# LTC3725

## Single-Switch Forward Controller and Gate Driver

## FEATURES

- **High Speed Gate Driver for Forward Converter**
- **On-Chip Rectifier and Self-Starting Architecture Eliminates Need for Separate Gate Drive Bias Supply**
- **Wide Input Voltage Supply Range: 9V and Up**
- **Linear Regulator Controller for Fast Start-Up**
- Precision UVLO with Adjustable Hysteresis
- Overcurrent Protection
- Volt-Second Limit Prevents Transformer Core Saturation
- Voltage Feedforward for Fast Transient Response
- Available in 10-Lead MSOP Package

## APPLICATIONS

- Isolated 48V Telecommunication Systems
- Internet Servers and Routers
- Distributed Power Step-Down Converters
- Automotive and Heavy Equipment

## DESCRIPTION

The LTC®3725 is a controller for a single-switch forward converter and includes an on-chip gate driver.

For secondary-side control, combine the LTC3725 with the LTC3706 PolyPhase® secondary-side synchronous forward controller to create a complete forward converter using a minimum of discrete parts. A proprietary scheme is used to multiplex gate drive signals across the isolation barrier through a tiny pulse transformer. The on-chip rectifier and the same pulse transformer provide gate drive bias power.

Alternatively, the LTC3725 can be used as a standalone voltage mode controller in a primary-side control architecture with optoisolator feedback. Voltage feedforward provides excellent line regulation and transient response.

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## TYPICAL APPLICATION

**36V-72V to 3.3V/30A Isolated Single-Switch Forward Converter**



L1: PULSE PA1294.910
T1: PULSE PA0815
T2: PULSE PA0297

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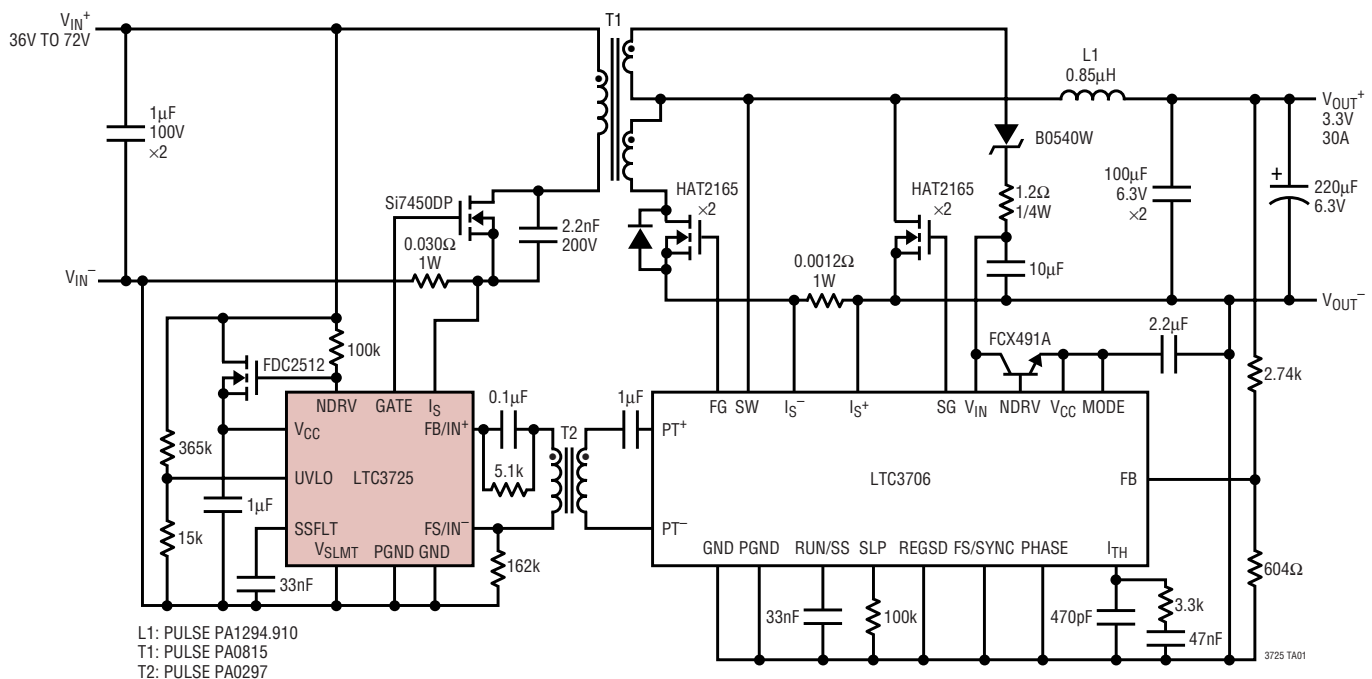
# ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Power Supply ($V_{CC}$) .................................. −0.3V to 15V
External NMOS Drive (NDRV) .................... −0.3V to 20V
NDRV to $V_{CC}$ ........................................................ − 0.3V to 5V
Soft-Start Fault, Feedback,
Frequency Set, Transformer
Inputs (SSFLT, FB/IN⁺, FS/IN⁻) .................. −0.3V to 15V
All Other Pins ($V_{SLMT}$, $I_S$, UVLO) ................. −0.3V to 5V
Peak Output Current <1µs (GATE) ........................... 2A
Operating Ambient Temperature Range .. −40°C to 85°C
Operating Junction Temperature (Note 2) ........... 125°C
Storage Temperature Range ................. −65°C to 150°C
Lead Temperature (Soldering, 10 sec).................. 300°C

# PACKAGE/ORDER INFORMATION

```
                    TOP VIEW
       UVLO   1  ┌───────────┐  10  I_S
       SSFLT  2  ┤           ├   9  V_SLMT
       NDRV   3  ┤     11    ├   8  V_CC
       FB/IN⁺ 4  ┤           ├   7  GATE
       FS/IN⁻ 5  └───────────┘   6  PGND
```

MSE PACKAGE
10-LEAD PLASTIC MSOP
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 45°C/W, $\theta_{JC}$ = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

| ORDER PART NUMBER | MSE PART MARKING |
|---|---|
| LTC3725EMSE | LTBSV |
| LTC3725IMSE | LTBSW |

**Order Options**  Tape and Reel: Add #TR
Lead Free: Add #PBF   Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 12V, GND = PGND = 0V, $T_A$ = 25°C, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$V_{CC}$ Supply, Linear Regulator and Trickle Charger Shunt Regulator** | | | | | | | |
| $V_{CCOP}$ | Operating Voltage Range | | | 7 | 12 | 15 | V |
| $V_{CCLR}$ | Output Voltage | Linear Regulator in Operation | | | 8 | | V |
| $I_{NDRV}$ | Current into NDRV Pin | Linear Regulator in Operation | | 0.1 | | 1 | mA |
| $t_{r(VCC)}$ | Rise Time of $V_{CC}$ | Linear Regulator Charging (0.5V to 7.5V) | | | 45 | | µs |
| $I_{NDRVTO}$ | Linear Regulator Time Out Current Threshold | Primary-Side Operation | | | 0.27 | | mA |
| $I_{CC}$ | Supply Current | $V_{UVLO}$ = 1.5V, Linear Regulator in Operation (Note 3) | | | 1.4 | 2.1 | mA |
| $I_{CCM}$ | Maximum Supply Current | $V_{UVLO}$ = 1.5V,  Trickle Charger in Operation, $V_{CC}$ = 13.2V (Note 3) | | | 1.7 | 2.5 | mA |
| $V_{CCSR}$ | Maximum Supply Voltage | Trickle Charger Shunt Regulator | | | 14.25 | 15 | V |
| $I_{CCSR}$ | Minimum Current into NDRV/$V_{CC}$ | Trickle Charger Shunt Regulator, $V_{CC}$ = 15V (Note 3) | | 10 | | | mA |
| **Internal Undervoltage** | | | | | | | |
| $V_{CCUV}$ | Internal Undervoltage Threshold | $V_{CC}$ Rising | | | 5.3 | | V |
| | | $V_{CC}$ Falling | | | 4.7 | | V |
| **Gate Drive Undervoltage** | | | | | | | |
| $V_{GDUV}$ | Gate Drive Undervoltage Threshold | $V_{CC}$ Rising (Linear Regulator) | ● | 7.2 | 7.4 | 7.7 | V |
| | | $V_{CC}$ Rising (Trickle Charger) | ● | 13.1 | 13.4 | 14 | V |
| | | $V_{CC}$ Falling | ● | 6.8 | 7.0 | 7.2 | V |
| **Undervoltage Lockout (UVLO)** | | | | | | | |
| $V_{UVLOR}$ | Undervoltage Lockout Threshold Rising | Rising | ● | 1.220 | 1.242 | 1.280 | V |
| $V_{UVLOF}$ | Undervoltage Lockout Threshold Falling | Falling | ● | 1.205 | 1.226 | 1.265 | V |

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# ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{CC} = 12V$, GND = PGND = 0V, $T_A = 25°C$, unless otherwise noted.

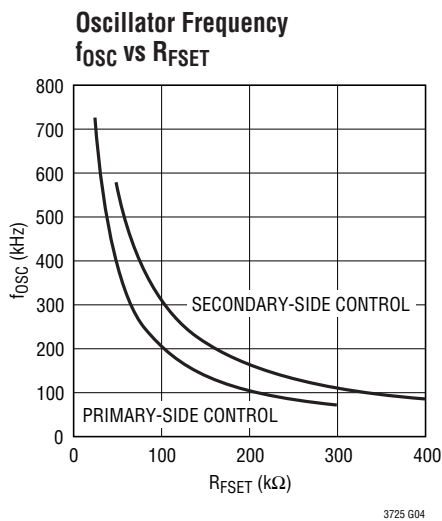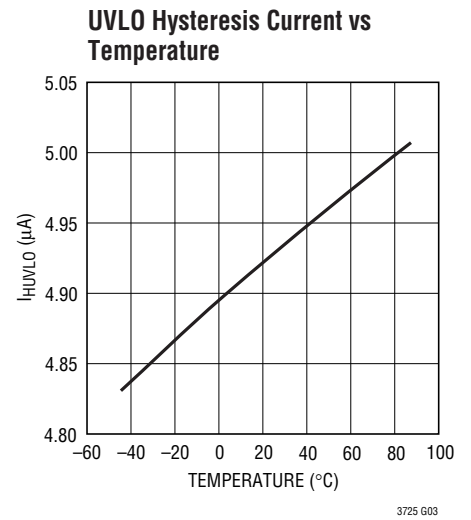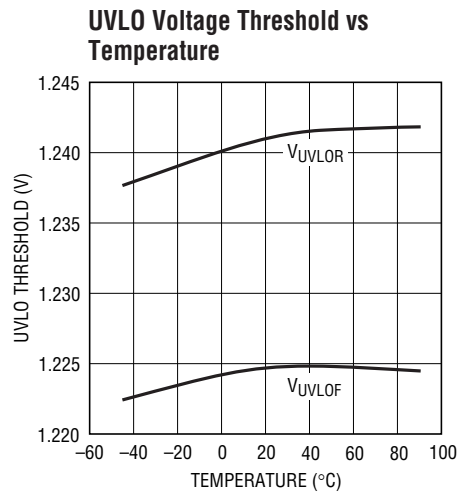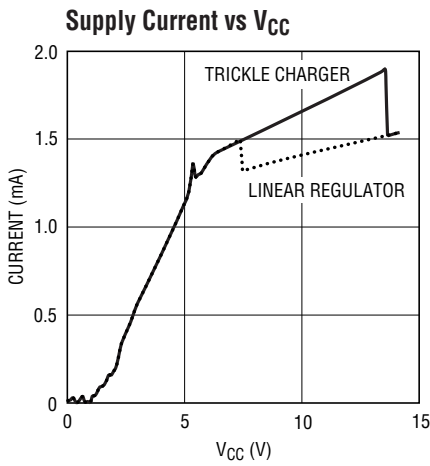| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{HUVLO}$ | Hysteresis Current | $V_{UVLO} = 1V$ | ● | 4.2 | 4.9 | 5.6 | µA |
| $V_{UVLOOP}$ | Voltage Feedforward Operating Range | Primary-Side Control | | $V_{UVLOF(MIN)}$ | 3.75 | | V |
| **Gate Driver (GATE)** | | | | | | | |
| $R_{OS}$ | Output Pull-Down Resistance | $I_{OUT} = 100mA$ | | | 1.9 | | Ω |
| $V_{OH}$ | High Output Voltage | $I_{OUT} = -100mA$ | | | 11 | | V |
| $I_{PU}$ | Peak Pull-Up Current | | | | 1.7 | | A |
| $t_r$ | Output Rise Time | 10% to 90%, $C_{OUT} = 4.7nF$ | | | 40 | | ns |
| $t_f$ | Output Fall Time | 10% to 90%, $C_{OUT} = 4.7nF$ | | | 70 | | ns |
| **Rectifier** | | | | | | | |
| $I_{RECT}$ | Maximum Rectifier DC Output Current | | | | | 25 | mA |
| **Oscillator** | | | | | | | |
| $f_{OSC(P)}$ | Oscillator Frequency | Primary-Side Control, $R_{FS(P)} = 100kΩ$ | | | 200 | | kHz |
| | | Primary-Side Control, $R_{FS(P)} = 25kΩ$ | | | 700 | | kHz |
| | | Primary-Side Control, $R_{FS(P)} = 300kΩ$ | | | 70 | | kHz |
| $\Delta f_{RFS(P)}$ | Oscillator Resistor Set Accuracy | Primary-Side Control $25k < R_{FSET} < 300k$ | | | ±15 | | % |
| $f_{OSC(S)}$ | Oscillator Frequency | Secondary-Side Control (During Start-Up), $R_{FS(S)} = 100kΩ$ | | | 300 | | kHz |
| **Soft-Start/Fault (SSFLT)** | | | | | | | |
| $I_{SS(C)}$ | Soft-Start Charge Current | Primary-Side Control, $V_{SSFLT} = 2V$ | | | -5.2 | | µA |
| | | Secondary-Side Control, $V_{UVLO} = 1.3V$, $V_{SSFLT} = 2V$ | | | -4 | | µA |
| | | Secondary-Side Control, $V_{UVLO} = 3.75V$, $V_{SSFLT} = 2V$ | | | -1.6 | | µA |
| $V_{LRTO}$ | Linear Regulator Time Out-Threshold | | | | 3.9 | | V |
| $V_{FLTH}$ | Fault Output High | $V_{CC} = 8V$ | | | 6.7 | | V |
| $I_{SS(D)}$ | Soft-Start Discharge Current | Timing Out After Fault, $V_{SSFLT} = 2V$ | | | 1 | | µA |
| **Current Sense Input ($I_S$)** | | | | | | | |
| $V_{IS(MAX)}$ | Overcurrent Threshold | | | | 300 | | mV |
| **Volt Second Limit ($V_{SLMT}$)** | | | | | | | |
| $V_{VSL(MAX)}$ | Volt-Second Limit Threshold | | | | 1.26 | | V |
| $I_{VSLMT(MAX)}$ | Maximum Volt-Second Limit Resistor Current | | | | 0.25 | | mA |
| **Optoisolator Bias Current** | | | | | | | |
| $V_{OPTO}$ | Open Circuit Optoisolator Voltage | Primary-Side Control $I_{FB} = 0V$ | | | 3.3 | | V |
| $I_{OPTO}$ | Optoisolator Bias Current | Primary-Side Control $V_{FB} = 2.5V$ | | | 0.5 | | mA |
| | | Primary-Side Control $V_{FB} = 0V$ | | | 1.6 | | mA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Operating junction temperature $T_J$ (in °C) is calculated from the ambient temperature $T_A$ and the average power dissipation PD (in watts) by the formula: $T_J = T_A + \theta_{JA} \cdot PD$. Refer to the Applications Information section for details.

**Note 3:** $I_{CC}$ is the sum of current into NDRV and $V_{CC}$.

**Note 4:** The LTC3725EMSE is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3725IMSE is guaranteed and tested over the –40°C to 85°C operating temperature range.

# TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current vs $V_{CC}$**



3725 G01

**UVLO Voltage Threshold vs Temperature**



3725 G02

**UVLO Hysteresis Current vs Temperature**



3725 G03

**Oscillator Frequency $f_{OSC}$ vs $R_{FSET}$**



3725 G04

**Oscillator Frequency vs Temperature**



3725 G05

**Shunt Regulator Current $I_{CC}$ vs $V_{CC}$**



3725 G06

**Shunt Regulator Current vs Temperature**



3725 G07

**$V_{GDUV}$ vs Temperature**



3725 G08

**Optoisolator Bias $V_{FB/IN+}$ vs $I_{FB/IN+}$**
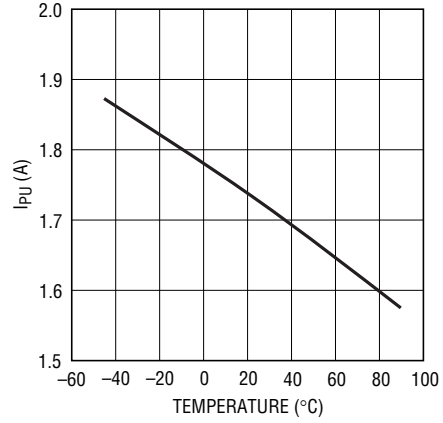


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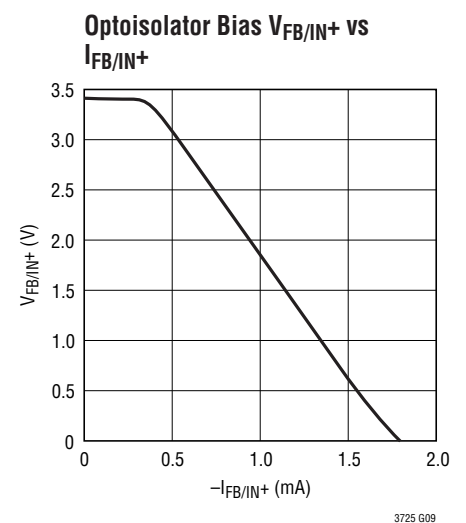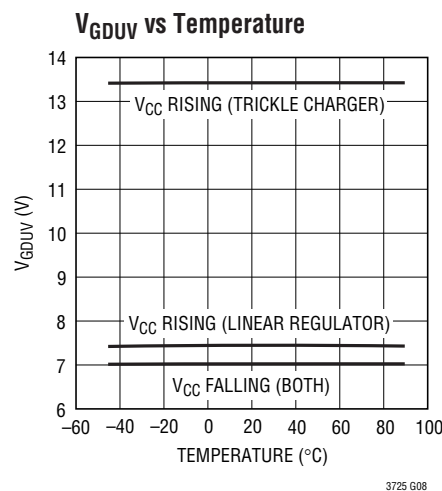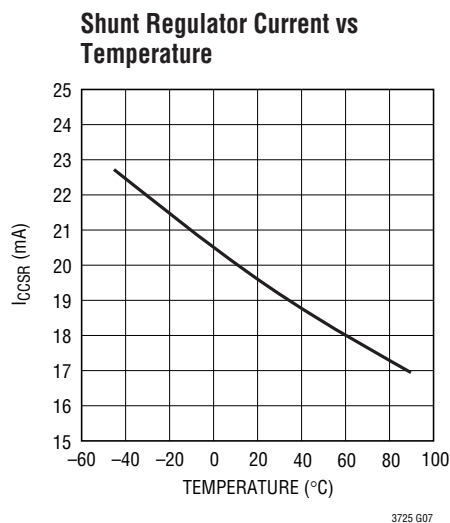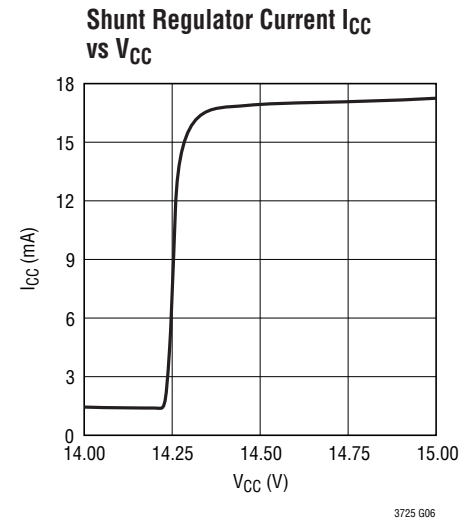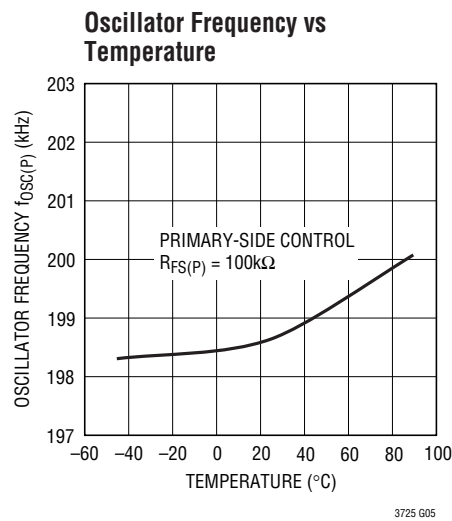
# TYPICAL PERFORMANCE CHARACTERISTICS

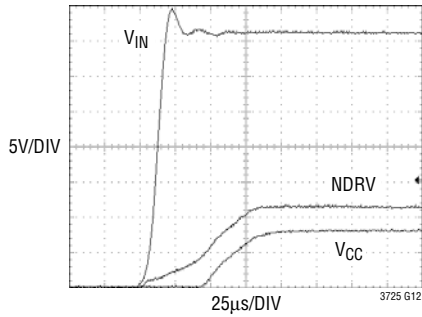**Gate Drive Pull-Down Resistance vs Temperature**
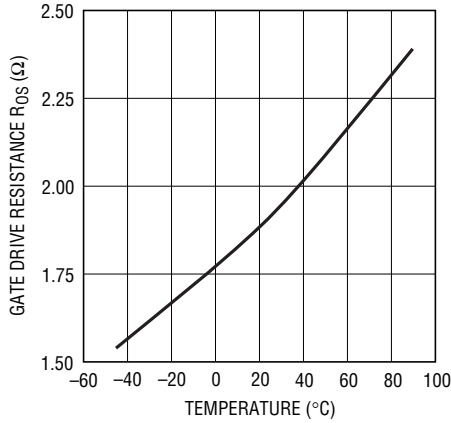

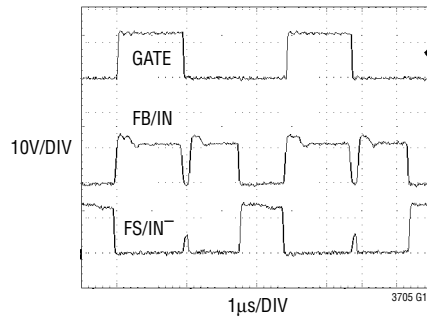
3725 G10

**Gate Drive Peak Pull-Up Current vs Temperature**
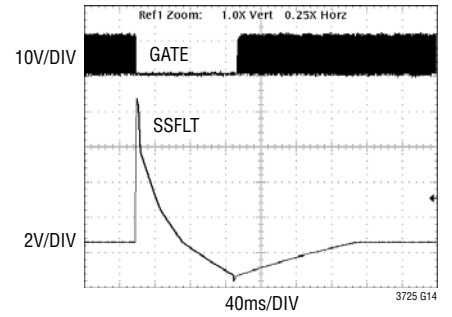


3725 G11

**Linear Regulator Start-Up**



3725 G12

**Gate Drive Encoding**



3705 G13

**Fault Operation**



3725 G14

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## PIN FUNCTIONS

**UVLO (Pin 1):** Undervoltage Lockout. Connect to a resistive voltage divider to monitor input voltage $V_{IN}$. Enables converter operation for $V_{UVLO} > 1.242V$. Hysteresis is a fixed 16mV hysteresis voltage with a 4.9μA hysteresis current that combines with the Thevenin resistance of the divider to set the total UVLO hysteresis voltage. This input also senses $V_{IN}$ for voltage feedforward. Finally, this pin can be used for external run/stop control.

**SSFLT (Pin 2):** Combination Soft-Start and Fault Indicator. A capacitor to GND sets the duty cycle ramp-up rate during start-up. To indicate a fault, the SSFLT pin is momentarily pulled up to within 1.3V of $V_{CC}$.

**NDRV (Pin 3):** Drive for the External NMOS Linear Regulator. Connect to the gate of the NMOS and connect a pull up resistor to the input voltage ($V_{IN}$). Optionally, to create a trickle charger omit the NMOS device and connect NDRV to $V_{CC}$.

**FB/IN+ (Pin 4):** This pin has several functions. One winding of a pulse transformer is connected to the FB/IN+ and FS/IN− pins. The other pulse transformer winding is connected to the LTC3706. The LTC3725 automatically detects when the LTC3706 applies a pulse-encoded signal to the FB/IN+ and FS/IN− pins and decodes duty cycle information for control of the primary-side gate drive (see Operation below). In secondary-side control, primary-side gate drive bias power is also extracted from the FB/IN+ and FS/IN− pins using an on-chip full-wave rectifier.

For primary-side control connect this pin to an optoisolator for feedback control of converter output voltage using an internal optoisolator biasing network.

**FS/IN− (Pin 5):** This pin has several functions. Place a resistor from this pin to GND to set the oscillator frequency. For secondary-side control with the LTC3706, connect one winding of the pulse transformer for operation as described for the FB/IN+ pin above.

**PGND (Pin 6):** Supply Return for the Bottom Gate Driver and the On-Chip Bridge Rectifier.

**GATE (Pin 7):** Gate Drive. Connect to the gate of the external MOSFET.

**$V_{CC}$ (Pin 8):** Main $V_{CC}$ Power for All Driver and Control Circuitry.

**$V_{SLMT}$ (Pin 9):** Volt-Second Limit. Form an R-C integrator by connecting a resistor from $V_{IN}$ to $V_{SLMT}$ and a capacitor from $V_{SLMT}$ to ground. The gate drive is turned off when the voltage on the $V_{SLMT}$ pin exceeds 1.26V.

**$I_S$ (Pin 10):** Input to the Overcurrent Comparator. Connect to the positive terminal of a current-sense resistor in series with the source of the ground-referenced bottom MOSFET.

**GND (Pin 11):** Signal Ground.

# BLOCK DIAGRAM
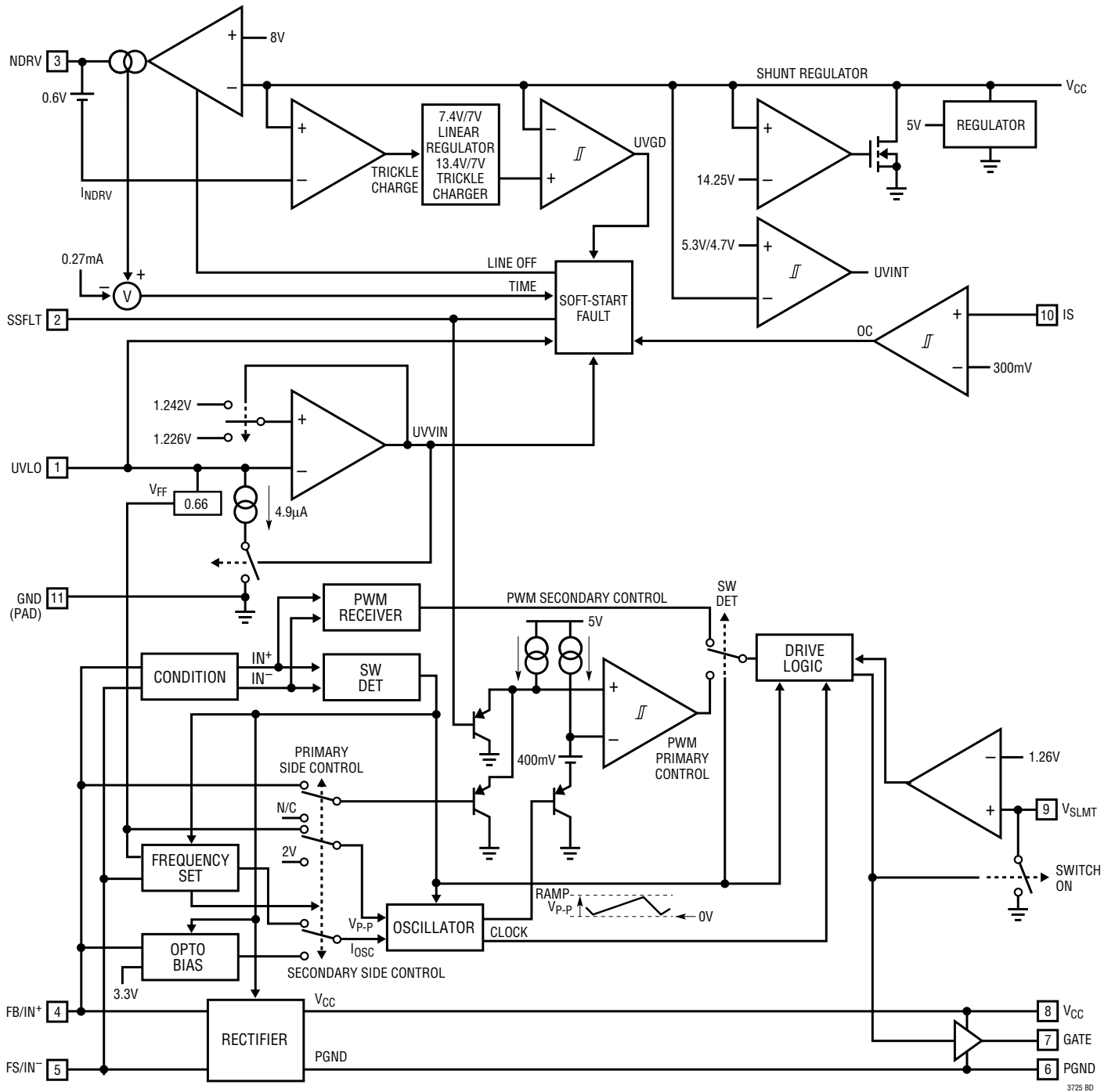
# OPERATION

## Mode Setting

The LTC3725 is a controller and gate driver designed for use in a single-switch forward converter. When used in conjunction with the LTC3706 PolyPhase secondary-side synchronous forward controller, it forms a complete forward converter with secondary-side regulation, galvanic isolation between input and output, and synchronous rectification. In this mode, upon start-up, the FB/IN$^+$ and FS/IN$^-$ pins are effectively shorted by one winding of the pulse transformer. The LTC3725 detects this short circuit to determine that it is in secondary-side control mode. Operation in this mode is confirmed when the LTC3706 begins switching the pulse transformer.

Alternately, the LTC3725 can be used as a standalone primary-side controller. In this case, the FB/IN$^+$ and FS/IN$^-$ pins operate independently. The FB/IN$^+$ pin is connected to the collector of an optoisolator to provide feedback and the FS/IN$^-$ pin is connected to the frequency set resistor.

## Gate Drive Encoding

In secondary-side control with the LTC3706, after a start-up sequence, the LTC3706 transmits multiplexed PWM information through a pulse transformer to the FB/IN$^+$ and FS/IN$^-$ inputs of the LTC3725. In the LTC3725, the PWM receiver extracts the duty cycle and uses it to control the gate driver.

Figure 1 shows that the LTC3706 drives the pulse transformer in a complementary fashion, with a duty cycle of approximately 75%. At the appropriate time during the positive half cycle, the LTC3706 applies a short (150ns) zero-voltage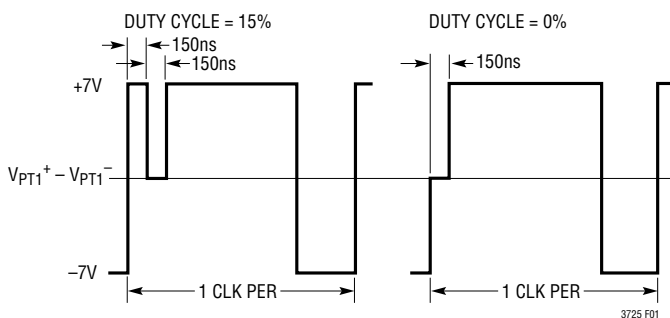 pulse across the pulse transformer, indicating the end of the "on" time. Although this scheme allows the transmission of 0% to 75% duty cycle, it is necessary to establish a minimum controllable "on" time of approximately 100ns. This ensures that 0% duty cycle can be reliably distinguished from 75% duty cycle.

## On-Chip Rectifier

Simultaneously with duty-cycle decoding, and through the same pulse transformer, the wave generated by the LTC3706 provides primary-side $V_{CC}$ gate drive bias power by way of the LTC3725's on-chip full-wave bridge rectifier. No auxiliary bias supply is necessary and forward converter design and circuitry are considerably simplified.

## External Series Pass Linear Regulator

The LTC3725 features an external series pass linear regulator that eliminates the long start-up time associated with the conventional trickle charger. The drain of an external NMOS is connected to the input voltage and the source is connected to $V_{CC}$. The gate of the NMOS is connected to NDRV. To power the gate, an external pull-up resistor is connected from the input voltage to NDRV. The NMOS must be a standard 3V threshold type (i.e. not logic level). An on-chip circuit manages the start up and operation of the linear regulator. It takes approximately 45μs for the linear regulator to charge $V_{CC}$ to its target value of 8V (unless limited by a slower rise of $V_{IN}$). The LTC3725 begins operating the gate drives when $V_{CC}$ reaches 7.4V. Often, the thermal rating of the NMOS prevents it from operating continuously, and the LTC3725 "times out" the linear regulator to prevent overheating. This is accomplished using the capacitor connected to the SSFLT pin as described subsequently.

## Trickle Charger Shunt Regulator

Alternately, a trickle charger can be implemented by eliminating the external NMOS and connecting NDRV to $V_{CC}$ and using the pull-up resistor to charge $V_{CC}$. To allow extra headroom for starting, the LTC3725 detects this mode and increases the threshold for starting the gate drives to 13.4V. An internal shunt regulator limits the voltage on the trickle charger to 15V.



**Figure 1. Gate Drive Multiplexing Scheme**

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# OPERATION

### Self-Starting Architecture

The LTC3725 is combined with the LTC3706 to form a complete self-starting DC isolated power supply. When power is first applied, and when $V_{CC}$ for the LTC3725 is above the appropriate threshold, the LTC3725 begins open-loop operation using its own internal oscillator. Power is supplied to the secondary by switching the gate driver with a gradually increasing duty cycle as controlled by the rate of rise of the voltage on the SSFLT pin. A peak detector power supply for the LTC3706 allows it to begin operation even for small duty cycles. Once adequate voltage is available for the LTC3706, it provides duty cycle information and gate drive bias power using the pulse transformer as shown in Figure 1. The LTC3725 detects the appearance of this signal and transfers control of the gate drivers to the LTC3706. Simultaneously, the LTC3725 also enables the on-chip rectifier and turns off the linear regulator.

Alternately, when the LTC3725 is used as a standalone primary-side controller, the gradually increasing duty cycle powers up a secondary-side reference and optoisolator and feedback is accomplished when the output of the optoisolator begins pulling down in the FB/IN⁺ pin.

### Soft-Start and Fault

These two functions are implemented using the SSFLT pin. (This pin is also used for linear regulator timeout as described in the following section.)

Initiating soft-start requires that: 1) the gate drive undervoltage (UVGD) goes low meaning that adequate voltage is available on the $V_{CC}$ pin (7.4V for the linear regulator or 13.4V for the trickle charger) and 2) the input undervoltage (UVV$_{IN}$) goes low meaning that the voltage on the UVLO pin has reached the 1.242V rising threshold.

During soft-start, the LTC3725 gradually charges the soft-start capacitor to ramp up the converter duty cycle. Soft-start is over when the voltage on the SSFLT pin reaches 2.8V. In normal operation, at some point before this, the LTC3725 makes a transition to controlling duty cycle using closed-loop regulation of the converter output voltage.

The SSFLT pin is also used to indicate a fault. The LTC3725 recognizes faults from four origins: 1) an overcurrent fault caused by the current sense voltage on the IS pin exceeding the 300mV overcurrent threshold, 2) an input undervoltage fault caused by the UVLO pin falling below the 1.226V falling threshold, 3) a gate drive undervoltage fault caused by the voltage on the $V_{CC}$ pin falling below the 7V threshold, or 4) loss of the gate drive encoding signal from the LTC3706.

Upon sensing a fault, the LTC3725 immediately turns off the gate drive and indicates a fault by quickly pulling the voltage on the SSFLT pin to within 1.3V of the voltage on the $V_{CC}$ pin. After indicating the fault, the LTC3725 quickly ramps down the voltage on the SSFLT pin to approximately 2.8V. Then, to allow complete discharge of the secondary-side circuit, the LTC3725 slowly ramps down the voltage on the SSFLT pin to about 200mV. The LTC3725 then attempts a restart.

### Linear Regulator Timeout

The thermal rating of the linear regulator's external NMOS often cannot allow it to indefinitely supply bias current to the primary-side gate drives. The LTC3725 has a linear regulator timeout mechanism that also uses the SSFLT capacitor.

As described in the prior section, soft-start is over once the voltage on the SSFLT pin reaches 2.8V. However, the SSFLT capacitor continues to charge and the linear regulator is turned off when the voltage on the SSFLT pin reaches 3.9V. The "Applications Information" section describes linear regulator timeout in more detail.

### Volt-Second Limit

The volt-second limit ensures that the power transformer core does not saturate for any combination of duty cycle and input voltage. The input of an R-C integrator is connected to $V_{IN}$ and its output is connected to the $V_{SLMT}$ pin. While the gate drive is "off," the LTC3725 grounds the $V_{SLMT}$ pin. When the gate drive is turned "on" the $V_{SLMT}$ pin is released and the capacitor is allowed to charge in proportion to $V_{IN}$. If the capacitor voltage on the $V_{SLMT}$ pin

# OPERATION

exceeds 1.26V the gate drive is immediately turned "off." Note that this is not considered a fault condition and the LTC3725 can run indefinitely with the switch duty cycle being determined by the volt-second limit circuit. The duty cycle is always limited to 75% to ensure that the power transformer flux always has time to reset before the start of the next cycle.

In an alternate application, the volt-second limit can be used for open-loop regulation of the output against changes in $V_{IN}$.

### Current Limit

Current limit for the LTC3725 is principally a safety feature to protect the converter and is not part of a control function. The current that flows in series through the transformer primary and the switch is sensed by a resistor connected between the source of the switch and GND. If the voltage across this resistor exceeds 300mV, the LTC3725 initiates a fault.

### Voltage Feedforward

The LTC3725 uses voltage feedforward to properly modulate the duty cycle as a function of the input voltage. For secondary-side control with the LTC3706, voltage feedforward is used during start-up only. The duty cycle during start up is determined by comparison of the voltage on the SSFLT pin to a 75% duty cycle triangle wave with an amplitude of 2V. To implement voltage feedforward, the charging current for the soft-start capacitor is reduced in proportion to the input voltage. As a result, the initial rate of rise of the converter output voltage is held approximately constant regardless of the input voltage. At some point during start-up, the LTC3706 begins to switch the pulse transformer and take over the soft-start.

For operation with standalone primary-side control and optoisolator feedback, voltage feedforward is used during both start-up and normal operation. The duty cycle is determined by using a 75% duty cycle triangle wave with an amplitude equal to 66% of the voltage on the UVLO pin which is, in turn, proportional to $V_{IN}$. The charging current for the soft-start capacitor is a constant 5.2μA. During soft-start, the duty cycle is determined by comparing the voltage on the SSFLT pin to the triangle wave. Soft-start is concluded when the voltage on the SSFLT pin exceeds the voltage on the FB/IN$^+$ pin. After the conclusion of soft-start, the duty cycle is determined by comparison of the voltage on the FB/IN$^+$ pin to the triangle wave.

### Optoisolator Bias

When the LTC3725 is used in standalone primary-side mode, feedback is provided by an optoisolator connected to the FB/IN$^+$ pin. The LTC3725 has a built optoisolator bias circuit which eliminates the need for external components.

LINEAR TECHNOLOGY

# APPLICATIONS INFORMATION

### UVLO

The UVLO pin is connected to a resistive voltage divider connected to $V_{IN}$ as shown in Figure 2. The voltage threshold on the UVLO pin for $V_{IN}$ rising is 1.242V. To introduce hysteresis, the LTC3725 draws 4.9μA from the UVLO pin when $V_{IN}$ is rising. The hysteresis is therefore user adjustable and depends on the value of R1. The UVLO threshold for $V_{IN}$ rising is:

$$V_{IN(UVLO, RISING)} = (1.242V)\frac{R1+R2}{R2} + R1(4.9\mu A)$$

The LTC3725 also has 16mV of voltage hysteresis on the UVLO pin so that the UVLO threshold for $V_{IN}$ falling is:

$$V_{IN(UVLO, FALLING)} = (1.226V)\frac{R1+R2}{R2}$$

To implement external Run/Stop control, connect a small NMOS to the UVLO pin as shown in Figure 2. Turning the NMOS on grounds the UVLO pin and prevents the LTC3725 from running.
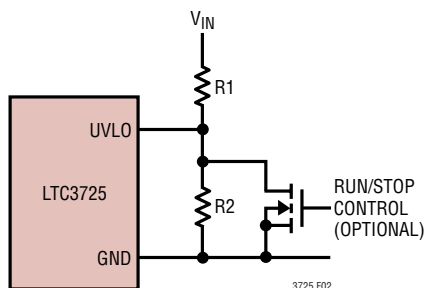


**Figure 2. Resistive Voltage Divider for UVLO and Optional Run/Stop Control**

### Linear Regulator

The linear regulator eliminates the long start-up times associated with a conventional trickle charger by using an external NMOS to quickly charge the capacitor connected to the $V_{CC}$ pin.

Note that a trickle charger usually requires a large capacitor to provide holdup for the $V_{CC}$ pin while the converter attempts to start. The linear regulator in the LTC3725 can both charge the capacitor connected to the $V_{CC}$ pin and provide primary-side gate-drive bias current. Therefore, with the linear regulator, the capacitor need only be large enough to cope with the ripple current from driving the gate of the primary FET and holdup need not be considered.

The external NMOS for the linear regulator should be a standard 3V threshold type (i.e. not a logic level threshold). The rate of charge of $V_{CC}$ from 0V to 8V is controlled by the LTC3725 to be approximately 45μs regardless of the size of the capacitor connected to the $V_{CC}$ pin. The charging current for this capacitor is approximately:

$$I_C = \frac{8V}{45\mu s}C$$

The safe operating area (SOA) for the external NMOS should be chosen so that capacitor charging does not damage the NMOS. Excessive values of capacitor are unnecessary and should be avoided.

### Start-Up Considerations

When used in a self-starting converter with the LTC3706, the LTC3725 initially begins the soft-start of the converter in an open-loop fashion. After bias is obtained on the secondary side, the LTC3706 assumes control and completes the soft-start interval. In order to ensure that control is properly transferred from the LTC3725 (primary-side) to the LTC3706 (secondary-side), it is necessary to limit the rate of rise on the primary-side soft-start ramp so that the LTC3706 has adequate time to wake up and assume control before the output voltage gets too high. This condition is satisfied for many applications if the following relationship is maintained:

$$C_{SS,SEC} \leq C_{SS\_PRI}$$

# APPLICATIONS INFORMATION

However, care should be taken to ensure that soft-start transfer from primary-side to secondary-side is completed well before the output voltage reaches its target value. A good design goal is to have the transfer completed when the output voltage is less than one-half of its target value. Note that the fastest output voltage rise time during primary-side soft-start mode occurs with minimum load current.

The open-loop start-up frequency on the LTC3725 is set by placing a resistor $R_{FS(S)}$ from the FS/IN$^-$ pin to GND. Although the exact start-up frequency on the primary side is not critical, it is generally a good practice to set it approximately equal to the operating frequency on the secondary side.

In this mode the start-up frequency of the LTC3725 is approximately:

$$f_{PRI} = \frac{34 \cdot 10^9}{R_{FS(S)} + 10,000}$$

In the event that the LTC3706 fails to start up properly and assume control of switching, there are several fail-safe mechanisms to help avoid overvoltage conditions. First, the LTC3725 implements a volt-second clamp that may be used to keep the primary-side duty cycle at a level that does not produce an excessive output voltage. Second, the timeout of the linear regulator (described in the following section) means that, unless the LTC3706 starts and supports the LTC3725 gate drive through the pulse transformer and on-chip rectifier, the LTC3725 eventually suffers a gate drive undervoltage fault. Finally, the LTC3706 has an independent overvoltage detection circuit that crowbars the output of the DC/DC converter using the synchronous secondary-side MOSFET switch.

In the event that a short-circuit is applied to the output of the converter prior to start-up, the LTC3706 generally does not receive enough bias voltage to operate. In this case, the LTC3725 detects a FAULT for one of two reasons: 1) since the LTC3706 never sends pulse encoding to the

LTC3725, the linear regulator times out resulting in a gate drive undervoltage fault, or 2) the primary-side overcurrent circuit is tripped because of current buildup in the output inductor. In either case, the LTC3725 initiates a shutdown followed by a soft-start retry.

**Linear Regulator Timeout**

After start-up, the LTC3725 times out the linear regulator to prevent overheating of the external NMOS. The timeout interval is set by further charging the soft-start capacitor $C_{SSFLT}$ from the end-of-soft-start voltage of approximately 2.8V to the timeout threshold of 3.9V. Linear regulator timeout behaves differently depending on mode.

In primary-side standalone mode, the LTC3725 generally requires that an auxiliary gate drive bias supply take over from the linear regulator. (See the subsequent section for more detail on the auxiliary supply.) During linear regulator timeout, the rate of rise of the soft-start capacitor voltage depends on the current into the NDRV pin as controlled by the pull-up resistor $R_{PULLUP}$, the value of $V_{IN}$ and the value of $V_{NDRV}$.

$$I_{NDRV} = \frac{V_{IN} - V_{NDRV}}{R_{PULLUP}}$$

The value of $V_{NDRV}$ is $V_{CC} = 8V$ plus the value of the gate-to-source voltage ($V_{NDRV} - V_{CC}$) of the external NMOS in the linear regulator. The gate-to-source voltage depends on the actual device but is approximately the threshold voltage of the external NMOS.

For $I_{NDRV} > 0.27$mA, the capacitor on the SSFLT pin is charged in proportion to ($I_{NDRV} - 0.27$mA) until the linear regulator times out. Thus, since $V_{NDRV}$ is very nearly constant, the timeout interval for the linear regulator is inversely proportional to the input voltage and a higher input voltage produces a shorter timeout.

$$t_{TIMEOUT} = \frac{66C_{SSFLT}(3.9V - 2.8V)}{\left[\frac{V_{IN} - V_{NDRV}}{R_{PULLUP}} - 0.27mA\right]}$$

# APPLICATIONS INFORMATION

Since the power dissipation of the linear regulator is proportional to the input voltage, this strategy of making the timeout inversely proportional to the input voltage produces an approximately constant temperature excursion for the external NMOS of the linear regulator regardless of the input voltage.

In situations for which the continuous operation of the linear regulator does not exceed the thermal limitations of the external NMOS (i.e. converters with low $V_{IN}$ or with minimal gate drive bias requirements), the auxiliary supply can be omitted and the linear regulator allowed to operate continuously. If $I_{NDRV}$ is less than 0.27mA the linear regulator never times out and the voltage on the SSFLT pin stays at approximately 2.8V after start-up is completed. To accomplish this set:

$$R_{PULLUP} > \frac{V_{IN(MAX)} - V_{NDRV}}{0.27mA}$$

where $V_{IN(MAX)}$ is the maximum expected continuous input voltage. Note that once the linear regulator is turned off it locks out. Therefore when using this strategy, care should be taken to ensure that a transient higher than $V_{IN(MAX)}$ does not persist longer than $t_{TIMEOUT}$.

In secondary-side operation with the LTC3706, there is never any need for continuous operation of the linear regulator since gate drive bias power is provided by the LTC3706 through the pulse transformer and on-chip rectifier. The LTC3725 shuts down the linear regulator once the LTC3706 begins switching the pulse transformer. If the LTC3706 fails to start, the LTC3725 quickly times out the linear regulator once the voltage on the SSFLT pin reaches 2.8V.

**Fault Lockout**

The LTC3725 indicates a fault by pulling the SSFLT pin to within 1V of $V_{CC}$. The LTC3725 subsequently attempts a restart. Optionally, the user can prevent restart and "lock out" the converter by clamping the voltage on the SSFLT pin with a 4.3V zener diode. Once the converter has locked out it can only be restarted by the removal of the input voltage or by release of the zener diode clamp.

**Pulse Transformer**

The pulse transformer that connects the LTC3706 to the LTC3725 performs the dual functions of gate drive duty cycle encoding and gate drive bias supply for the LTC3725 by way of the on-chip full-wave rectifier. The designs of the LTC3725 and LTC3706 have been coordinated so that the transformer turn ratio is:

$$N_{LTC3725} = 2N_{LTC3706}$$

where $N_{LTC3725}$ is the number of turns in the winding connected to the FB/IN$^+$ and FS/IN$^-$ pins of the LTC3725 and $N_{LTC3706}$ is the number of turns in the winding connected to the PT$^+$ and PT$^-$ pins of the LTC3706. The winding connected to the LTC3706 must be able to withstand volt-seconds equal to:

$$(V - s)_{MAX} = \frac{V_{CC}}{2f}$$

where $V_{CC}$ is the maximum supply voltage for the LTC3706 and f is the operating frequency of the LTC3706.

# APPLICATIONS INFORMATION

**Auxiliary Supply**

When used with the LTC3706, the LTC3725 does not require an auxiliary supply to provide primary-side gate-drive bias current. After start-up, primary-side gate drive current is provided by the LTC3706 through a small pulse transformer and the LTC3725's on-chip rectifier.

However, when used as a standalone primary-side controller, the LTC3725 may require a conventional gate-drive bias supply as shown in Figure 3. The bias supply must be designed to keep the voltage on the $V_{CC}$ pin between the absolute maximum of 15V and the gate-drive undervoltage lockout of 7V.

The auxiliary supply is connected in parallel with $V_{CC}$. The linear regulator maintains $V_{CC}$ at 8V. If the auxiliary supply produces more than 8V, it turns off the external NMOS before the LTC3725 can time out the linear regulator. If the auxiliary supply produces less than 8V, the linear regulator times out and then the voltage on the $V_{CC}$ pin declines to the voltage produced by the auxiliary supply.

**Slave Mode Operation**

When the LTC3725 is paired with the LTC3706, multiple pairs can be used to form a PolyPhase converter. In PolyPhase operation, one LTC3725 becomes the "master" while the remainder become "slaves." The master controls start-up in the same manner as for the single-phase converter, while the slaves do not begin switching until receiving PWM information through their own pulse trans-former from their corresponding LTC3706. To synchronize operation, the SSFLT and $V_{CC}$ pins of the master are connected to the corresponding pins of all the slaves. The master is designated by connection of the frequency set resistor to the FS/IN⁻ pin while this resistor is omitted from the slaves. For the slaves the NDRV pin is connected to the $V_{CC}$ pin. See the following section on PolyPhase Applications for more detail.

**PolyPhase Applications**

Figure 4 shows the basic connections for using the LTC3725 and LTC3706 in PolyPhase applications. One of the phases is always identified as the "master," while all other phases are "slaves." For the LTC3725 (primary side), the master performs the open-loop start-up and supplies the initial $V_{CC}$ voltage for the master and all slaves. The LTC3725 slaves are put into that mode by omitting the resistor on FS/IN−. The LTC3725 slaves simply stand by and wait for PWM signals from their respective pulse transformers. Since the SSFLT pins of master and slave LTC3725s are interconnected, a FAULT (overcurrent, etc.) on any one of the phases will perform a shutdown/restart on all phases together.

For the LTC3706, the master performs soft-start and voltage-loop regulation by driving all slaves to the same current as the master using the $I_{TH}$ pins. Faults and shutdowns are communicated via the interconnection of the RUN/SS pins. The LTC3706 is put into slave mode by tying the FB pin to $V_{CC}$.
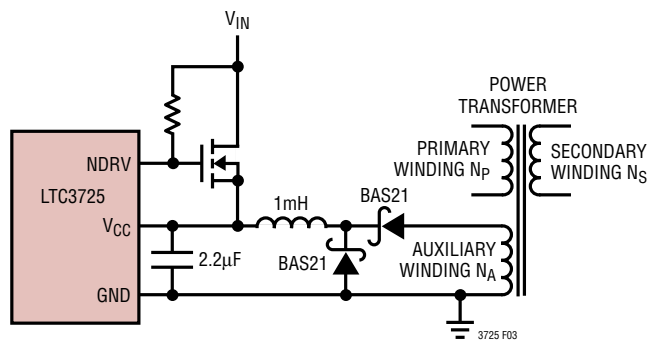


Figure. 3. Auxiliary Supply for Primary-Side Control
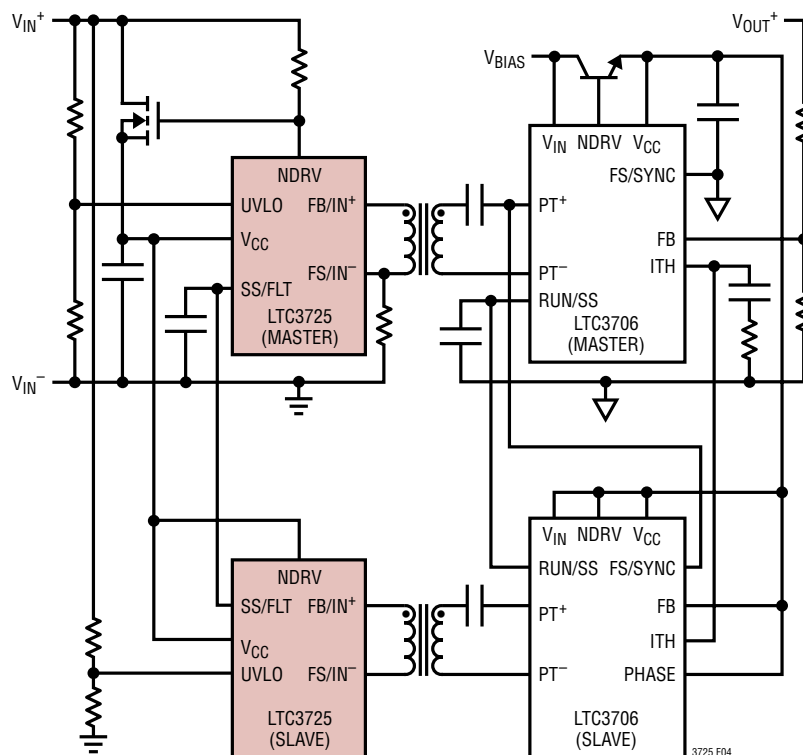
# APPLICATIONS INFORMATION



**Figure 4. Connections for PolyPhase**

## Standalone Primary-Side Operation

The LTC3725 can be used to implement a standalone forward converter using optoisolator feedback and a secondary-side voltage reference. Alternately the LTC3725 can be used to implement an open-loop forward converter using the $V_{SLMT}$ pin to regulate against changes in $V_{IN}$. In either case, the LTC3725 oscillator determines the frequency as found from:

$$f_{OSC} = \frac{21 \cdot 10^9}{R_{FS(P)} + 4200}$$

Note that polyphase operation is not possible in the standalone configuration.

## Grounding Considerations

The LT3725 is typically used in high current converter designs that involve substantial switching transients. Figure 5 illustrates these currents. The switch driver on the IC is designed to drive a large capacitance and, as such, generate significant transient currents. Careful consideration must be made regarding input and local power supply bypassing to avoid corrupting the ground references used by the UVLO and frequency set circuitry.

Typically, high current paths and transients from the input supply and any local drive supplies must be kept isolated from GND. By virtue of the topologies used in LT3725 applications, the large currents from the primary switch, as well as the switch drive transients, pass through the sense resistor to ground. This defines the ground connection of the sense resistor as the reference point for both GND and PGND.

# APPLICATIONS INFORMATION

Effective grounding can be achieved by considering the return current paths from the sense resistor to each respective bypass capacitor. Don't be tempted to run small traces to separate the grounds. A power ground plane is important as always in high power converters, but care must be taken to keep high current paths away from the GND reference. An effective approach is to use a 2-layer ground plane, reserving an entire layer for GND and an entire layer for PGND. The UVLO and frequency set resistors can then be directly connected to the GND plane.
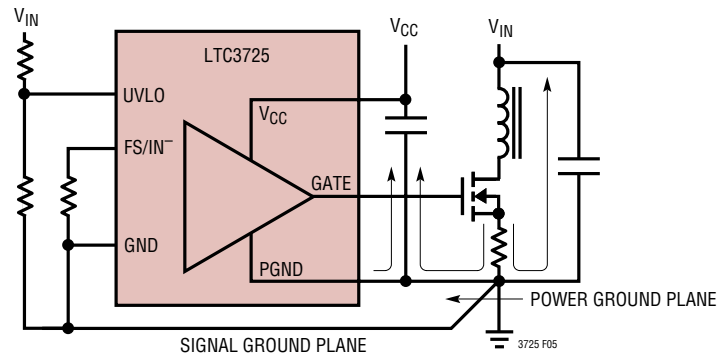


**Figure 5. High Current Transient Return Paths**

3725fa

# TYPICAL APPLICATIONS
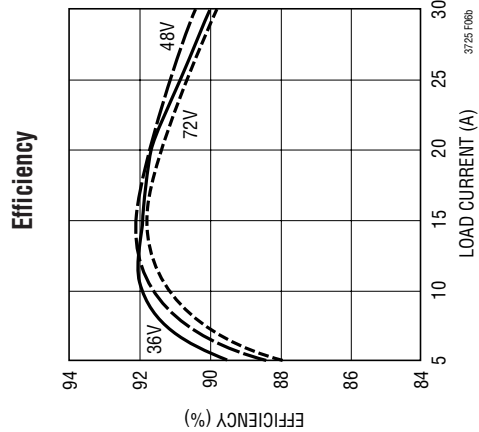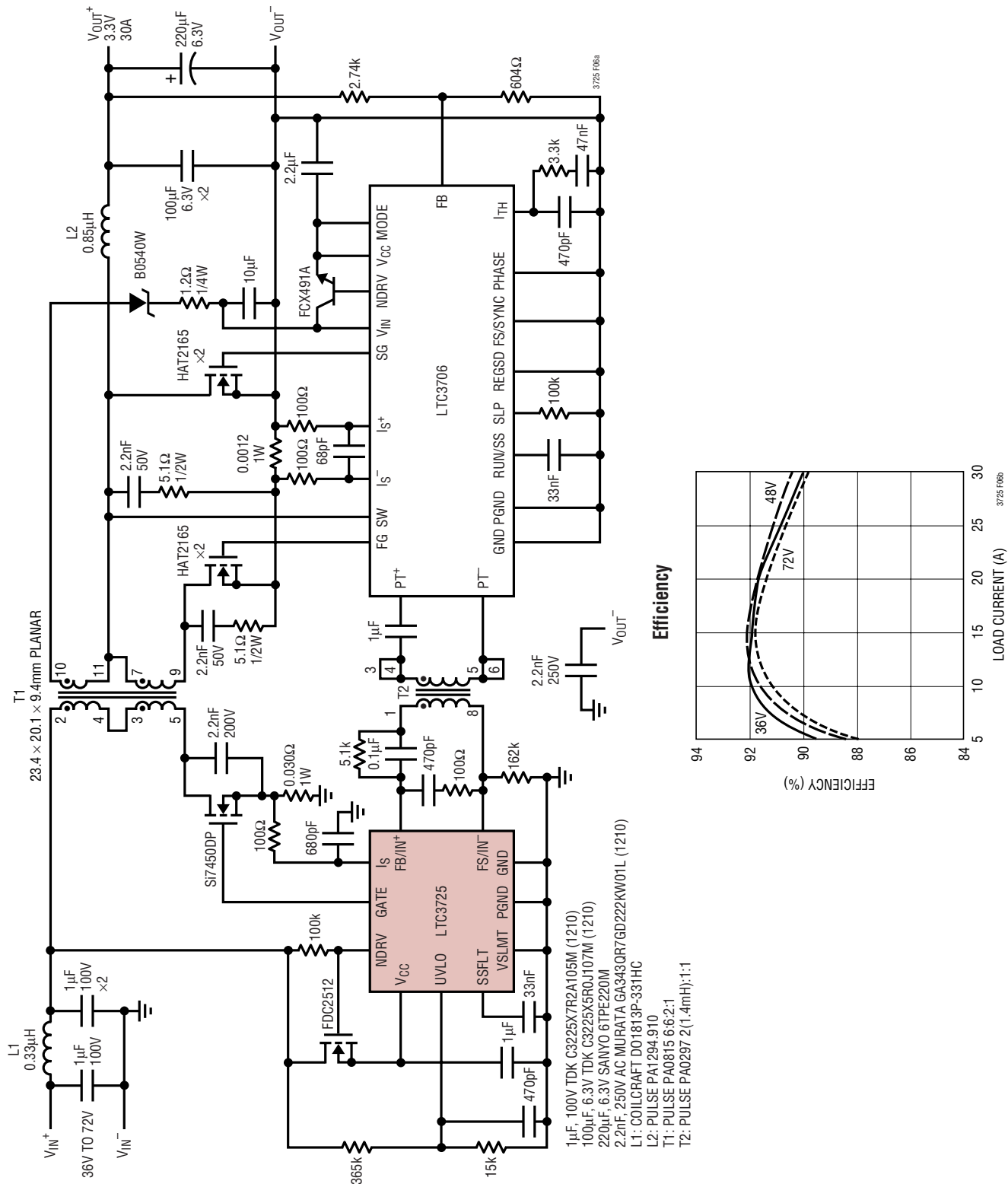


Figure 6. 36V–72V to 3.3V/30A Isolated Forward Converter Using LTC3706

1µF, 100V TDK C3225X7R2A105M (1210)
100µF, 6.3V TDK C3225X5R0J107M (1210)
220µF, 6.3V SANYO 6TPE220M
2.2nF, 250V AC MURATA GA343QR7GD222KW01L (1210)
L1: COILCRAFT DO1813P-331HC
L2: PULSE PA1294.910
T1: PULSE PA0815 6:6:2:1
T2: PULSE PA0297 2(1.4mH):1:1

Efficiency

# TYPICAL APPLICATIONS



10µF, 25V TDK C3225X7R1E106M (1210)
27µF, 100V SANYO MV-AX
1.5µF, 63V FILM WIMA MKS2
2.2nF, 250V AC MURATA GA343QR7GD222KW01L
L1: PULSE PE-53911
L2, L3: TDK SLF12575T-101M1R9
T1: PULSE PA0700 3T(16µH):11:11

**Figure 7. 12V$_{IN}$ to 48V/1.5A Isolated Forward Converter Using Optoisolator**

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# PACKAGE DESCRIPTION

**MSE Package**
**10-Lead Plastic MSOP**
(Reference LTC DWG # 05-08-1663)



BOTTOM VIEW OF
EXPOSED PAD OPTION

2.794 ± 0.102
(.110 ± .004)

0.889 ± 0.127
(.035 ± .005)

5.23
(.206)
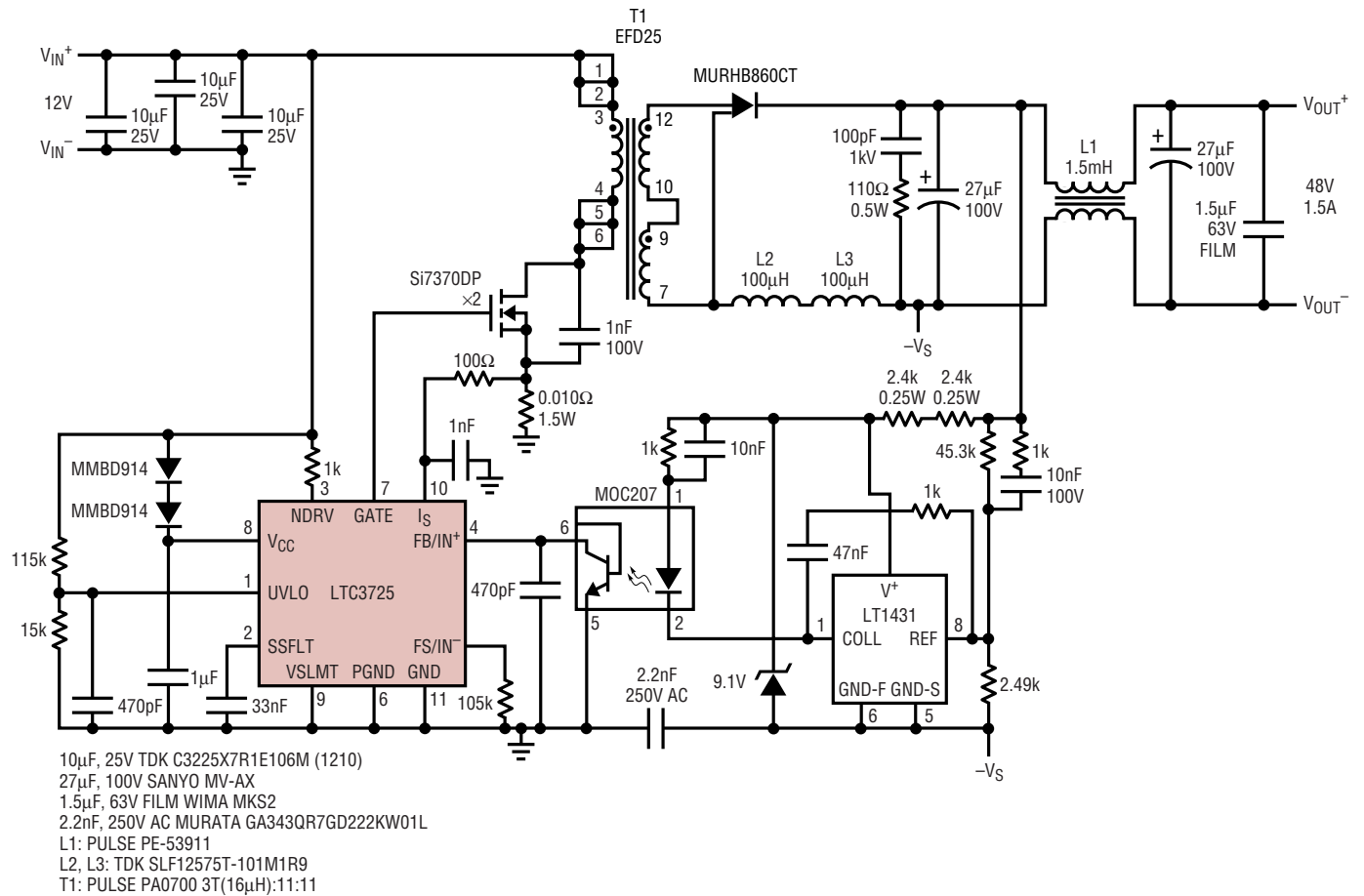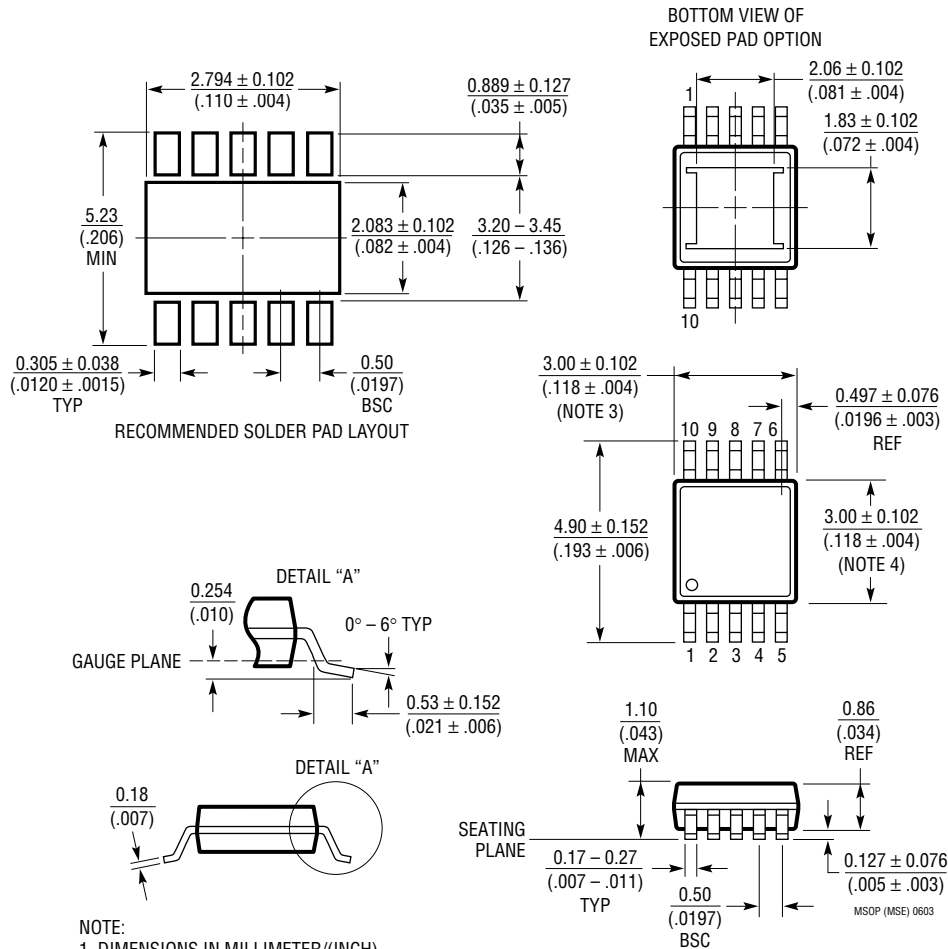MIN

2.083 ± 0.102
(.082 ± .004)

3.20 – 3.45
(.126 – .136)

0.305 ± 0.038
(.0120 ± .0015)
TYP

0.50
(.0197)
BSC

RECOMMENDED SOLDER PAD LAYOUT

2.06 ± 0.102
(.081 ± .004)

1.83 ± 0.102
(.072 ± .004)

1

10

3.00 ± 0.102
(.118 ± .004)
(NOTE 3)

0.497 ± 0.076
(.0196 ± .003)
REF

10 9 8 7 6

4.90 ± 0.152
(.193 ± .006)

3.00 ± 0.102
(.118 ± .004)
(NOTE 4)

1 2 3 4 5

DETAIL "A"

0.254
(.010)

0° – 6° TYP

GAUGE PLANE

0.53 ± 0.152
(.021 ± .006)

DETAIL "A"

0.18
(.007)

1.10
(.043)
MAX

0.86
(.034)
REF

SEATING
PLANE

0.17 – 0.27
(.007 – .011)
TYP

0.50
(.0197)
BSC

0.127 ± 0.076
(.005 ± .003)

MSOP (MSE) 0603

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

3725fa

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1693 | High Speed Single/Dual N-Channel MOSFET Drivers | CMOS Compatible Input, $V_{CC}$ Range: 4.5V to 12V |
| LTC1698 | Secondary Synchronous Rectifier Controller | Use with the LT1681, Optocoupler Driver, Pulse Transformer Synchronization |
| LT1950 | Single Switch Controller | Used for 20W to 500W Forward Converters |
| LTC3705 | 2-Switch Forward Controller and Gate Driver | 2-Switch Version of LTC3725 |
| LTC3706 | Polyphase Secondary-Side Synchronous Forward Controller | Fast Transient Response, Self-Starting Architecture, Current Mode Control |
| LT3710 | Secondary-Side Synchronous Post Regulator | For Regulated Auxiliary Output in Isolated DC/DC Converters |
| LTC3726 | Secondary-Side Synchronous Forward Controller | Similar to the LTC3706 |
| LT3781 | "Bootstrap" Start Dual Transistor Synchronous Forward Controller | 72V Operation, Synchronous Switch Output |
| LT3804 | Secondary Side Dual Output Controller with Opto Driver | Regulates Two Secondary Outputs, Optocoupler Feedback Driver and Second Output Synchronous Driver Controller |
| LTC3901 | Secondary-Side Synchronous Driver for Push-Pull and Full-Bridge Converter | Similar Function to LTC3900, Used in Full-Bridge and Push-Pull Converter |