Low Distortion, High Speed Rail-to-Rail Input/Output Amplifier

Known Good Die

AD8028-KGD-CHIP

FEATURES

High speed
190 MHz, –3 dB bandwidth (G = +1)
100 V/µs slew rate
Low distortion
120 dBc @ 1 MHz SFDR
80 dBc @ 5 MHz SFDR
Selectable input crossover threshold
Low noise
4.3 nV/√Hz
1.6 pA/√Hz
Low offset voltage: 900 µV max
Low power: 6.5 mA/amplifier supply current
Disable mode
Wide supply range: 2.7 V to 12 V
Known good die (KGD): these die are fully guaranteed to data sheet specifications

APPLICATIONS

Filters
ADC drivers
Level shifting
Buffering
Professional video
Low voltage instrumentation

GENERAL DESCRIPTION

The AD8028-KGD-CHIP[1] is a high speed amplifier with rail-to-rail input and output that operates on low supply voltages and is optimized for high performance and wide dynamic signal range. The AD8028-KGD-CHIP has low noise (4.3 nV/√Hz, 1.6 pA/√Hz) and low distortion (120 dBc at 1 MHz). In applications that use a fraction of or the entire input dynamic range and require low distortion, the AD8028-KGD-CHIP is an ideal choice.

Many rail-to-rail input amplifiers have an input stage that switches from one differential pair to another as the input signal crosses a threshold voltage, which causes distortion. The AD8028-KGD-CHIP has a unique feature that allows the user to select the input crossover threshold voltage through the SELECT pin. This feature controls the voltage at which the complementary transistor input pairs switch. The AD8028-KGD-CHIP also has intrinsically low crossover distortion. With its wide supply voltage range (2.7 V to 12 V) and wide bandwidth (190 MHz), the AD8028-KGD-CHIP amplifier is designed to work in a variety of applications where speed and performance are needed on low supply voltages. The AD8028-KGD-CHIP has a disable mode that is controlled via the SELECT pin.

The AD8028-KGD-CHIP is rated to work over the industrial temperature range of –40°C to +125°C.

Additional application and technical information can be found in the AD8028 data sheet.

[1]Protected by U.S. patent numbers 6,486,737B1; 6,518,842B1

Rev. B **Document Feedback**

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7/12—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V at T_A = 25°C, R_L = 1 kΩ to midsupply, G = 1, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Status[1]	Unit
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = 1, V_{OUT} = 0.2 V p-p	138	190		GBD	MHz
	G = 1, V_{OUT} = 2 V p-p	20	32		GBD	MHz
Bandwidth for 0.1 dB Flatness	G = 2, V_{OUT} = 0.2 V p-p		16			MHz
Slew Rate	G = +1, V_{OUT} = 2 V step/G = –1, V_{OUT} = 2 V step		90/100			V/µs
Settling Time to 0.1%	G = 2, V_{OUT} = 2 V step		35			ns
NOISE/DISTORTION PERFORMANCE						
Spurious-Free Dynamic Range (SFDR)	f_C = 1 MHz, V_{OUT} = 2 V p-p, RF = 24.9 Ω		120			dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p, RF = 24.9 Ω		80			dBc
Input Voltage Noise	f = 100 kHz		4.3			nV/√Hz
Input Current Noise	f = 100 kHz		1.6			pA/√Hz
Differential Gain Error	NTSC, G = 2, R_L = 150 Ω		0.1			%
Differential Phase Error	NTSC, G = 2, R_L = 150 Ω		0.2			Degrees
Crosstalk, Output to Output	G = 1, R_L = 100 Ω, V_{OUT} = 2 V p-p, V_S = ±5 V @ 1 MHz		–93			dB
DC PERFORMANCE						
Input Offset Voltage	SELECT = three-state or open, PNP active		200			µV
	SELECT = high NPN active		240			µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.50			µV/°C
Input Bias Current	V_{CM} = 0 V, NPN active		4	6	Tested	µA
	T_{MIN} to T_{MAX}		4			µA
	V_{CM} = 0 V, PNP active		–8	–11	Tested	µA
	TMIN to T_{MAX}		–8			µA
Input Offset Current			±0.1	±0.9	Tested	µA
Open-Loop Gain	V_{OUT} = ±2.5 V		110			dB
INPUT CHARACTERISTICS						
Input Impedance			6			MΩ
Input Capacitance			2			pF
Input Common-Mode Voltage Range			–5.2 to 5.2			V
Common-Mode Rejection Ratio	VCM = ±2.5 V		110			dB
SELECT PIN						
Crossover Low, Selection Input Voltage	Three-state < ±20 µA		–3.3 to +5			V
Crossover High, Selection Input Voltage			–3.9 to –3.3			V
Disable Input Voltage			–5 to –3.9			V
Disable Switching Speed	50% of input to <10% of final V_{OUT}		980			ns
Enable Switching Speed			45			ns
OUTPUT CHARACTERISTICS						
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = +6 V to –6 V, G = –1		40/45			ns
Output Voltage Swing		$-V_S + 0.20$	$+V_S - 0.06$, $-V_s + 0.06$	$+V_S$	Tested	V
Short-Circuit Output	Sinking and Sourcing		120			mA
Off Isolation	V_{IN} = 0.2 V p-p, f = 1 MHz, SELECT = low		–49			dB
Capacitive Load Drive	30% overshoot		20			pF
POWER SUPPLY						
Operating Range		2.7		12		V
Quiescent Current/Amplifier			6.5	8.5	Tested	mA
Quiescent Current (Disabled)	SELECT = low					
$+V_S$			0.8	3	Tested	mA
$–V_S$		–0.9	–0.6		Tested	mA
Power Supply Rejection Ratio	V_S ± 1 V		110			dB

[1] GBD is guaranteed by design.

V_S = 5 V at T_A = 25°C, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Status[1]	Unit
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	G = 1, V_{OUT} = 0.2 V p-p	131	185		GBD	MHz
	G = 1, V_{OUT} = 2 V p-p	18	28		GBD	MHz
Bandwidth for 0.1 dB Flatness	G = 2, V_{OUT} = 0.2 V p-p		12			MHz
Slew Rate	G = +1, V_{OUT} = 2 V step/G = −1, V_{OUT} = 2 V step		85/100			V/µs
Settling Time to 0.1%	G = 2, V_{OUT} = 2 V step		40			ns
NOISE/DISTORTION PERFORMANCE						
Spurious-Free Dynamic Range (SFDR)	f_C = 1 MHz, V_{OUT} = 2 V p-p, RF = 24.9 Ω		90			dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p, RF = 24.9 Ω		64			dBc
Input Voltage Noise	f = 100 kHz		4.3			nV/√Hz
Input Current Noise	f = 100 kHz		1.6			pA/√Hz
Differential Gain Error	NTSC, G = 2, R_L = 150 Ω		0.1			%
Differential Phase Error	NTSC, G = 2, R_L = 150 Ω		0.2			Degrees
Crosstalk, Output to Output	G = 1, R_L = 100 Ω, V_{OUT} = 2 V p-p, V_S = ±5 V @ 1 MHz		−92			dB
DC PERFORMANCE						
Input Offset Voltage	SELECT = three-state or open, PNP active		200	800	Tested	µV
	SELECT = high NPN active		240	900	Tested	µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		2			µV/°C
Input Bias Current	V_{CM} = 2.5 V, NPN active		4			µA
	T_{MIN} to T_{MAX}		4			µA
	V_{CM} = 2.5 V, PNP active		−8			µA
	T_{MIN} to T_{MAX}		−8			µA
Input Offset Current			±0.1			µA
Open-Loop Gain	V_{OUT} = 1 V to 4 V		105			dB
INPUT CHARACTERISTICS						
Input Impedance			6			MΩ
Input Capacitance			2			pF
Input Common-Mode Voltage Range			−0.2 to +5.2			V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 2.5 V		105			dB
SELECT PIN						
Crossover Low, Selection Input Voltage	Three-state < ±20 µA		1.7 to 5			V
Crossover High, Selection Input Voltage			1.1 to 1.7			V
Disable Input Voltage			0 to 1.1			V
Disable Switching Speed	50% of input to <10% of final V_{OUT}		1100			ns
Enable Switching Speed			50			ns
OUTPUT CHARACTERISTICS						
Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +6 V, G = −1		50/50			ns
Output Voltage Swing	R_L = 1 kΩ	−Vs + 0.12	+VS − 0.04, −Vs + 0.04	+Vs	Tested	V
Off Isolation	V_{IN} = 0.2 V p-p, f = 1 MHz, SELECT = low		−49			dB
Short-Circuit Current	Sinking and sourcing		105			mA
Capacitive Load Drive	30% overshoot		20			pF
POWER SUPPLY						
Operating Range		2.7		12	GBD	V
Quiescent Current/Amplifier			6			mA
Quiescent Current (Disabled)	SELECT = low		320			µA
Power Supply Rejection Ratio	V_S ± 1 V		105			dB

[1] GBD is guaranteed by design.

V_S = 3 V at T_A = 25°C, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Status[1]	Unit
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = 1, V_{OUT} = 0.2 V p-p	125	180		GBD	MHz
	G = 1, V_{OUT} = 2 V p-p	19	29		GBD	MHz
Bandwidth for 0.1 dB Flatness	G = 2, V_{OUT} = 0.2 V p-p		10			MHz
Slew Rate	G = +1, V_{OUT} = 2 V step/G = –1, V_{OUT} = 2 V step		73/100			V/µs
Settling Time to 0.1%	G = 2, V_{OUT} = 2 V step		48			ns
NOISE/DISTORTION PERFORMANCE						
Spurious-Free Dynamic Range (SFDR)	f_C = 1 MHz, V_{OUT} = 2 V p-p, R_F = 24.9 Ω		85			dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p, R_F = 24.9 Ω		64			dBc
Input Voltage Noise	f = 100 kHz		4.3			nV/√Hz
Input Current Noise	f = 100 kHz		1.6			pA/√Hz
Differential Gain Error	NTSC, G = 2, R_L = 150 Ω		0.15			%
Differential Phase Error	NTSC, G = 2, R_L = 150 Ω		0.20			Degrees
Crosstalk, Output to Output	G = 1, R_L = 100 Ω, V_{OUT} = 2 V p-p, V_S = 3 V @ 1 MHz		–89			dB
DC PERFORMANCE						
Input Offset Voltage	SELECT = three-state or open, PNP active		200			µV
	SELECT = high NPN active		240			µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		2			µV/°C
Input Bias Current	V_{CM} = 1.5 V, NPN active		4			µA
	T_{MIN} to T_{MAX}		4			µA
	V_{CM} = 1.5 V, PNP active		–8			µA
	T_{MIN} to T_{MAX}		–8			µA
Input Offset Current			±0.1			µA
Open-Loop Gain	V_{OUT} = 1 V to 2 V		100			dB
INPUT CHARACTERISTICS						
Input Impedance			6			MΩ
Input Capacitance			2			pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		–0.2 to +3.2			V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V		100			dB
SELECT PIN						
Crossover Low, Selection Input Voltage	Three-state < ±20 µA		1.7 to 3			V
Crossover High, Selection Input Voltage			1.1 to 1.7			V
Disable Input Voltage			0 to 1.1			V
Disable Switching Speed	50% of input to <10% of final V_{OUT}		1150			ns
Enable Switching Speed			50			ns
OUTPUT CHARACTERISTICS						
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = –1 V to +4 V, G = –1		55/55			ns
Output Voltage Swing	R_L = 1 kΩ	$–V_S$ + 0.09	$+V_S$ – 0.03, $–V_S$ + 0.03	$+V_S$	Tested	V
Short-Circuit Current	Sinking and sourcing		72			mA
Off Isolation	V_{IN} = 0.2 V p-p, f = 1 MHz, SELECT = low		–49			dB
Capacitive Load Drive	30% overshoot		20			pF
POWER SUPPLY						
Operating Range		2.7		12	GBD	V
Quiescent Current/Amplifier			6.0			mA
Quiescent Current (Disabled)	SELECT = low		300			µA
Power Supply Rejection Ratio	V_S ± 1 V		100			dB

[1] GBD is guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Common-Mode Input Voltage	$\pm V_S \pm 0.5$ V
Differential Input Voltage	±1.8 V
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

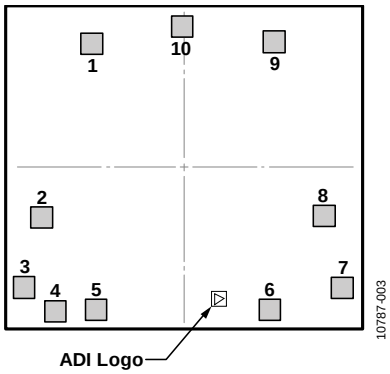

Figure 1.Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	X-Axis	Y-Axis	Mnemonic	Description
1	−326	+491	V_{OUTA}	Output A.
2	−547	−212	−IN A	Inverting Input A.
3	−590	−346	+IN A	Noninverting Input A.
4	−592	−490	$-V_S$	Negative Supply.
5	−286	−492	Disable Control/Select A	Disable Control/Select Mode A.
6	+325	−489	Disable Control/Select B	Disable Control/Select Mode B.
7	+593	−490	+IN B	Noninverting Input B.
8	+596	−350	−IN B	Inverting Input B
9	+324	+491	V_{OUTB}	Output B.
10	+86	+492	$+V_S$	Positive Supply.

OUTLINE DIMENSIONS

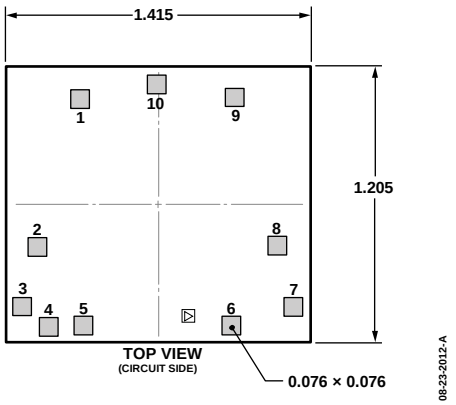

Figure 2. 10-Pad Bare Die [CHIP]
(C-10-3)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Typical Die Specifications

Parameter	Value	Unit
Chip Size	1420 × 1290	µm
Scribe Line Width	75	µm
Die Size	55.7 × 47.4	Mil
Thickness	305	µm
Bond Pads (Min Size)	76 × 76	µm
Bond Pad Composition	1% Copper Doped Aluminum	%
Backside	Si	Not Applicable
Passivation	Doped oxide/SiN	Not Applicable
ESD	HBM 2000	V

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Ablestik 84-1LMIS R4
Bonding Method	1 mil gold

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8028-KGD-CHIP	–40°C to +125°C	10-Pad Bare Die	C-10-3