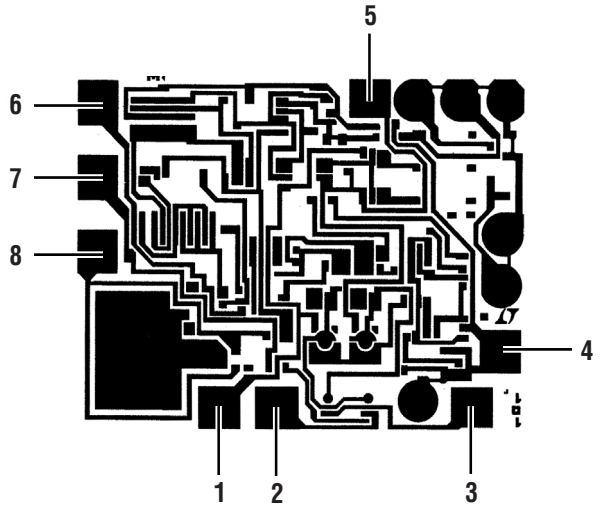
DICE/DWF SPECIFICATION

RH101A
Operational Amplifier



80 × 59 mils

Backside (substrate) is an alloyed gold layer. May be connected to V^- or no connection.

DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH101A RH101A	RH101A DICE RH101A DWF

PAD FUNCTION

1. BAL/COMP
2. –IN
3. +IN
4. V^-
5. BAL
6. OUT
7. V^+
8. COMP

DICE ELECTRICAL TEST LIMITS

T_A = 25°C. V_S = ±20V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	T_A = 25°C MIN	MAX	UNITS
Pre-Irradiation (Note 1)					
V_{OS}	Input Offset Voltage	$R_S \leq 50k$		2	mV
I_{OS}	Input Offset Current			10	nA
I_B	Input Bias Current	V_{CM} = 0V		75	nA
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k$	50		V/mV
CMRR	Common Mode Rejection Ratio	$R_S \leq 50k$	80		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 50k$	80		dB
	Input Voltage Range	V_S = ±20V	±15		V
V_{OUT}	Output Voltage Swing	V_S = ±15V, $R_L \geq 10k$ V_S = ±15V, $R_L \geq 2k$	±12 ±10		V V
I_S	Supply Current	V_S = ±20V		3	mA

DICE ELECTRICAL TEST LIMITS

T_A = 25°C. V_S = ±20V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	10Krad(SI) MIN	10Krad(SI) MAX	20Krad(SI) MIN	20Krad(SI) MAX	50Krad(SI) MIN	50Krad(SI) MAX	100Krad(SI) MIN	100Krad(SI) MAX	200Krad(SI) MIN	200Krad(SI) MAX	UNITS
Post-Irradiation (Note 4)													
V_{OS}	Input Offset Voltage	$R_S \leq 50k$		2		2		2		2		3	mV
I_{OS}	Input Offset Current			10		10		10		10		20	nA
I_B	Input Bias Current			75		75		100		200		400	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±15V, $R_S \leq 50k$	80		80		80		80		80		dB
PSRR	Power Supply Rejection Ratio	V_{CM} = ±5V to ±20V, $R_S \leq 50k$	80		80		80		80		80		dB
A_{VOL}	Large Signal Voltage Gain	R_L = ±2k, V_O = ±10V, V_S = ±15V	50		50		50		50		25		V/mV
V_{OUT}	Maximumm Output Voltage Swing	V_S = ±15V, $R_L \geq 10k$ V_S = ±15V, $R_L \geq 2k$	±12 ±10		±12 ±10		±12 ±10		±12 ±10		±12 ±10		V V
I_S	Supply Current	V_S = ±20V	3		3		3		3		3		mA

Note 1: Unless otherwise noted, all measurements are made with unity gain compensation (C1 = 30pF); these specifications apply for $\pm5V \leq V_S \leq 20V$.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 3: Refer to LTC standard product data sheet for all other applicable information.

Note 4: The post-irradiation table is for lot qualification based on sample lot assembly and testing only. Contact LTC marketing for more detail.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-0101

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