REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with N.O.R. 5962-R003-93.	92-11-25	M. A. FRYE
B	Drawing updated to reflect current requirements. Redrawn. - ro	06-12-11	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
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REV																			
SHEET																			

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B				
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10				

PMIC N/A

PREPARED BY
RICK C. OFFICER

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
CHARLES E. BESORE

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
91-08-16

MICROCIRCUIT, LINEAR, HIGH SPEED, PRECISION, JFET, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
B	A	**67268**	**5962-89976**

SHEET 1 OF 10

DSCC FORM 2233
APR 97

5962-E097-07

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89976	01	G	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LT1055A	High speed precision JFET operational amplifier
02	LT1056A	High speed precision JFET operational amplifier
03	LT1055	High speed precision JFET operational amplifier
04	LT1056	High speed precision JFET operational amplifier

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
G	MACY1-X8	8	Can

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_S) ..... ±20 V dc
Differential input voltage (V_{ID}) ..... ± 40 V dc
Input voltage (V_{IN}) ..... ±20 V dc
Output short circuit duration ..... Indefinite
Power dissipation (P_D) ..... 500 mW
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Junction temperature (T_J) ..... +150°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 150°C/W

1.4 Recommended operating conditions.

Supply voltage (V_S) ..... ±15 V dc
Common mode voltage (V_{CM}) ..... 0 V
Operating ambient temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_S = \pm 15$ V, $V_{CM} = 0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input voltage range	V_{IN}		1	01	-11.0	11.0	V
			2,3		-10.5	10.5	
Input offset voltage	V_{IO}	1/	4	01	-150	150	µV
			2,3		-500	500	
			4	02	-180	180	
			2,3		-550	550	
			4	03	-400	400	
			2,3		-1200	1200	
			4	04	-450	450	
			2,3		-1250	1250	
Average temperature coefficient of input offset voltage	$\Delta V_{IO} / \Delta T$	2/ 3/	2,3	01,02	-4.0	4.0	µV/°C
				03,04	-8.0	8.0	
Input offset current	I_{IO}	1/	1	01	-10	10	pA
			2		-1.2	1.2	nA
			1	02	-10	10	pA
			2		-1.5	1.5	nA
			1	03	-20	20	pA
			2		-1.8	1.8	nA
			1	04	-20	20	pA
			2		-2.4	2.4	nA
Input bias current	I_{IB}	1/	1	01	-50	50	pA
			2		-2.5	2.5	nA
			1	02	-50	50	pA
			2		-3.0	3.0	nA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_S = \pm15$ V, $V_{CM} = 0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input bias current	I_{IB}	1/	1	03	-50	50	pA
			2		-4.0	4.0	nA
			1	04	-50	50	pA
			2		-5.0	5.0	nA
		V_{CM} = +10 V	1	01,02		100	pA
				03,04		150	
Common mode rejection ratio	CMRR	$V_{CM} = \pm11$ V	1	01,02	86		dB
		$V_{CM} = \pm10.5$ V	2,3		85		
		$V_{CM} = \pm11$ V	1	03,04	83		
		$V_{CM} = \pm10.5$ V	2,3		82		
Power supply rejection ratio	PSRR	$V_S = \pm10$ V to ±18 V	1	01,02	90		dB
		$V_S = \pm10$ V to ±17 V	2,3		88		
		$V_S = \pm10$ V to ±18 V	1	03,04	88		
		$V_S = \pm10$ V to ±17 V	2,3		86		
Supply current	I_S		1	01		4.0	mA
			2,3			14.0	
			1	02		6.5	
			2,3			14.0	
			1	03		4.0	
			2,3			14.0	
			1	04		7.0	
			2,3			14.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_S = \pm 15$ V, $V_{CM} = 0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Large signal voltage gain 4/	A_{VOL}	$R_L = 2$ kΩ, $V_O = \pm 10$ V	4	01	150		V/mV
		$R_L = 1$ kΩ, $V_O = \pm 10$ V			130		
		$R_L = 2$ kΩ, $V_O = \pm 10$ V	5,6		40		
		$R_L = 2$ kΩ, $V_O = \pm 10$ V	4	02	150		
		$R_L = 1$ kΩ, $V_O = \pm 10$ V			130		
		$R_L = 2$ kΩ, $V_O = \pm 10$ V	5,6		40		
		$R_L = 2$ kΩ, $V_O = \pm 10$ V	4	03	120		
		$R_L = 1$ kΩ, $V_O = \pm 10$ V			100		
		$R_L = 2$ kΩ, $V_O = \pm 10$ V	5,6		35		
		$R_L = 2$ kΩ, $V_O = \pm 10$ V	4	04	120		
		$R_L = 1$ kΩ, $V_O = \pm 10$ V			100		
		$R_L = 2$ kΩ, $V_O = \pm 10$ V	5,6		35		
Output voltage swing	V_{OUT}	$R_L = 2$ kΩ	4,5,6	All	-12	12	V
Input noise current density 2/ 4/ 5/	I_N	$f_O = 10$ Hz	7	All		4.0	fA / $\sqrt{Hz}$
		$f_O = 1$ kHz				4.0	
Input noise voltage density 2/ 6/	E_N	$f_O = 10$ Hz	7	01,02		65	nV / $\sqrt{Hz}$
		$f_O = 1$ kHz				20	
		$f_O = 10$ Hz		03,04		60	
		$f_O = 1$ kHz				22	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_S = \pm 15$ V, $V_{CM} = 0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Slew rate 2/	SR	R_L = 2 kΩ minimum, C_L = 100 pF, A_V = +5, $V_{IN} = \pm 2$ V, measured at -7 V and +7 V	7,8b	01	10.0		V/µs
			8a		5.0		
			7,8b	02	12.0		
			8a		6.0		
			7,8b	03	7.5		
			8a		3.5		
			7,8b	04	9.0		
			8a		4.0		

1/ Offset voltage is measured under two different conditions. The first, approximately 0.5 seconds after application of power. The second, at T_A = +25°C only, with the chip heated to approximately 38°C for devices 01 and 03, and 45°C for devices 02 and 04, to account for chip temperature rise when the device is fully warmed up.
I_{IO} and I_{IB} are measured fully warmed up also.

2/ If not tested, shall be guaranteed to the limits specified in table I herein.

3/ Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100 kΩ potentiometer between the balance terminals and the wiper tied to V_{S+}.

4/ f_O symbolizes output frequency and V_O symbolizes output voltage.

5/ Current noise is calculated using the formula: $I_N = (2 \times q \times I_{IB}) \times 1/2$ where $q = 1.6 \times 10^{-19}$ coulomb.
The noise of source resistors up to 1 GΩ swamps the contribution of current noise.

6/ Input noise voltage density at f_O = 10 Hz is sample tested on every lot to a sample size series number of 15.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Device types	01, 02, 03, and 04
Case outline	G
Terminal number	Terminal symbol
1	BALANCE
2	INPUT-
3	INPUT+
4	V_{S-}
5	BALANCE
6	OUT
7	V_{S+}
8	NC

NC = No connection

FIGURE 1. Terminal connections.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 7
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7, 8a, 8b
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-12-11

Approved sources of supply for SMD 5962-89976 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8997601GA	3/	LT1055AMH/883
5962-8997602GA	3/	LT1056AMH/883
5962-8997603GA	3/	LT1055MH/883
5962-8997604GA	3/	LT1056MH/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply. The last known supplier is listed below.

Vendor CAGE number	Vendor name and address
64155	Linear Technology Corporation 720 Sycamore Drive Milpitas, CA 95035