ANALOG DEVICES

Dual/Quad Low Power, High Speed JFET Operational Amplifiers

AD8682/AD8684

FEATURES

Low supply current: 250 μA/amp maximum
High slew rate: 9 V/μs
Bandwidth: 3.5 MHz typical
Low offset voltage: 1 mV maximum @ 25°C
Low input bias current: 20 pA maximum @ 25°C
CMRR: 90 dB typical
Fast settling time
Unity-gain stable

APPLICATIONS

Portable telecommunications
Low power industrial and instrumentation
Loop filters
Active and precision filters
Integrators
Strain gauge amplifiers
Portable medical instrumentation
Supply current monitoring

PIN CONFIGURATIONS

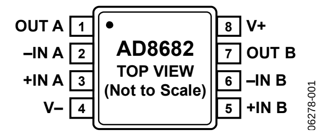

Figure 1. 8-Lead SOIC_N and 8-Lead MSOP

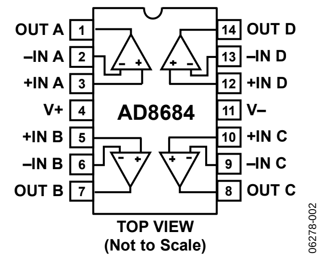

Figure 2. 14-Lead SOIC_N and 14-Lead TSSOP

GENERAL DESCRIPTION

The AD8682 and AD8684 are dual and quad low power, precision (1 mV) JFET amplifiers featuring excellent speed at low supply currents. The slew rate is typically 9 V/μs with a supply current under 250 μA per amplifier. These unity-gain stable amplifiers have a typical gain bandwidth of 3.5 MHz. The JFET input stage ensures bias current is typically a few picoamps and below 125 pA maximum over the full temperature operating range.

The devices are ideal for portable, low power applications, especially with high source impedance. The devices are unity-gain stable and can drive higher capacity loads (G = 1, noninverting), as an example of their excellent dynamic response over a wide range of conditions, delivering dc precision performance at low quiescent currents.

Rev. B

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7/07—Rev. 0 to Rev. A

Change to Figure 21 ... 8
Change to Figure 31 ... 9

10/06—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = ±15.0 V, T_A = 25°C, V_{CM} = 0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.35	1	mV
AD8682		+25°C ≤ T_A ≤ +85°C			2.5	mV
		−40°C ≤ T_A ≤ +25°C			3	mV
AD8684		+25°C ≤ T_A ≤ +85°C			3.5	mV
		−40°C ≤ T_A ≤ +25°C			4	mV
Input Bias Current	I_B			6	20	pA
		−40°C ≤ T_A ≤ +85°C			125	pA
Input Offset Current	I_{OS}				20	pA
		−40°C ≤ T_A ≤ +85°C			100	pA
Input Voltage Range			−11		+15	V
Common-Mode Rejection Ratio	CMRR	−11 V ≤ V_{CM} ≤ +15 V, −40°C ≤ T_A ≤ +85°C	70	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20			V/mV
		R_L = 10 kΩ, −40°C ≤ T_A ≤ +85°C	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ	13.5	13.9		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ		−13.9	−13.5	V
Short-Circuit Limit	I_{SC}	Source	3	10		mA
		Sink		−12	−8	mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, −40°C ≤ T_A ≤ +85°C	92	114		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, −40°C ≤ T_A ≤ +85°C		210	250	µA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/µs
Full-Power Bandwidth	BW_P	1% distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			3.5		MHz
Phase Margin	$Ø_M$			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n			0.01		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage[1]	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

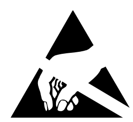
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP [RM-8]	210	45	°C/W
8-Lead SOIC_N [R-8]	158	43	°C/W
14-Lead TSSOP [RU-14]	180	35	°C/W
14-Lead SOIC_N [R-14]	120	36	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

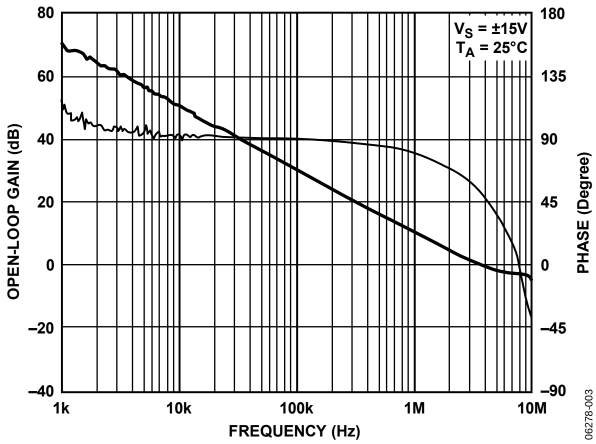


Figure 3. AD8682 Open-Loop Gain and Phase vs. Frequency

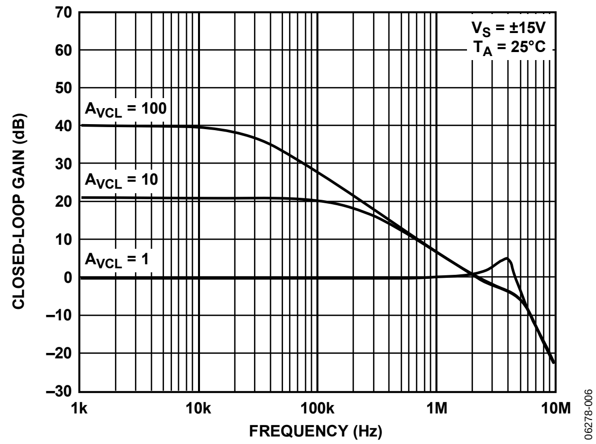


Figure 6. AD8682 Closed-Loop Gain vs. Frequency

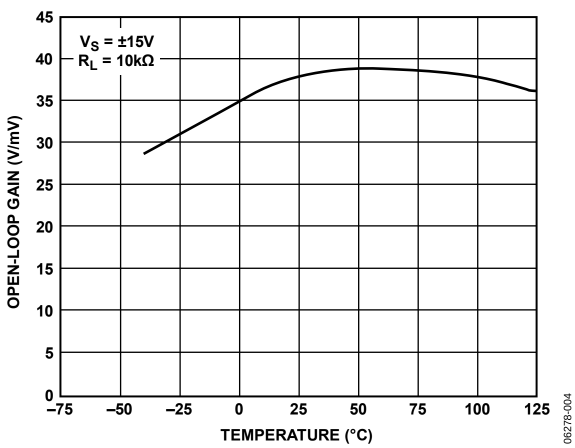


Figure 4. AD8682 Open-Loop Gain vs. Temperature

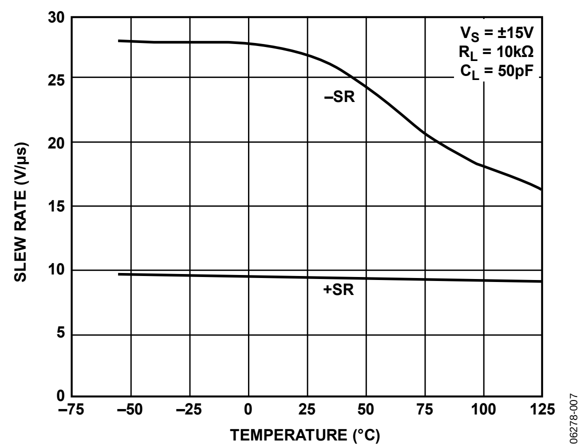


Figure 7. Slew Rate vs. Temperature

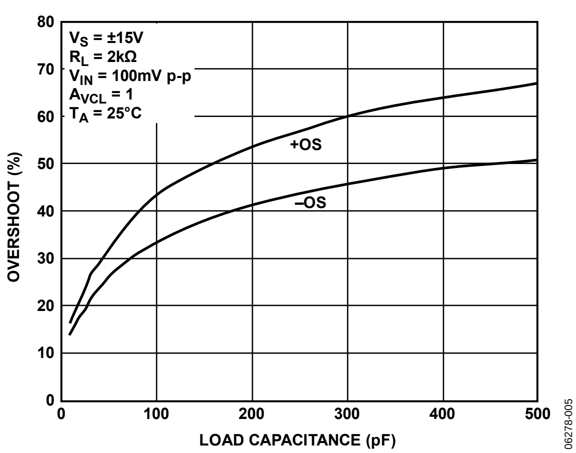


Figure 5. Small Signal Overshoot vs. Load Capacitance

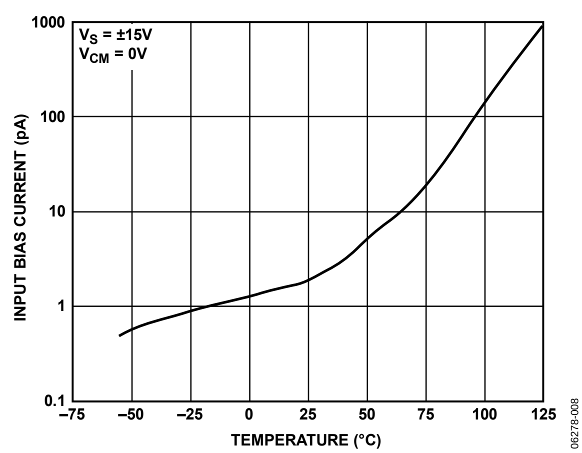


Figure 8. AD8682 Input Bias Current vs. Temperature

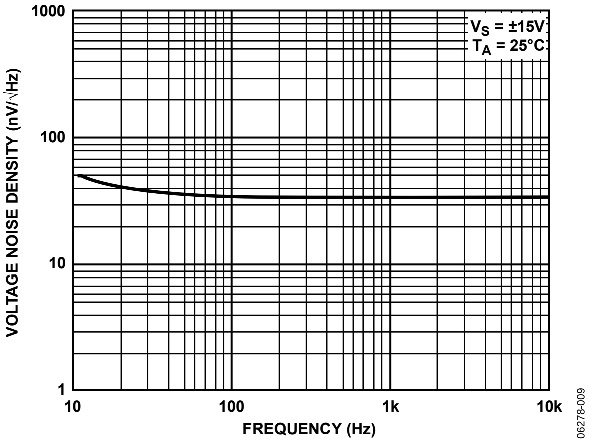


Figure 9. Voltage Noise Density vs. Frequency

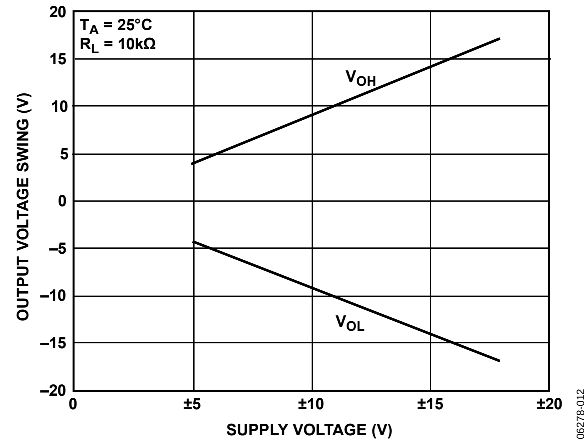


Figure 12. Output Voltage Swing vs. Supply Voltage

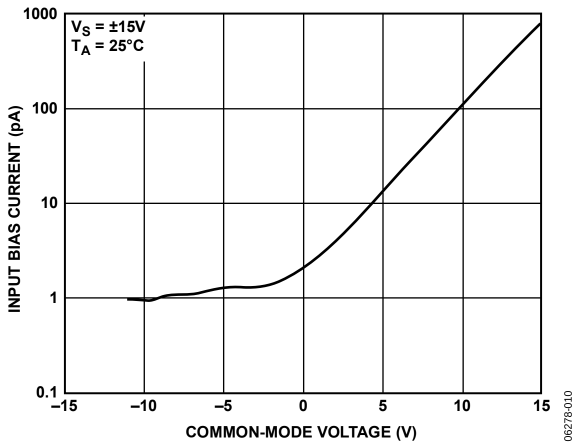


Figure 10. Input Bias Current vs. Common-Mode Voltage

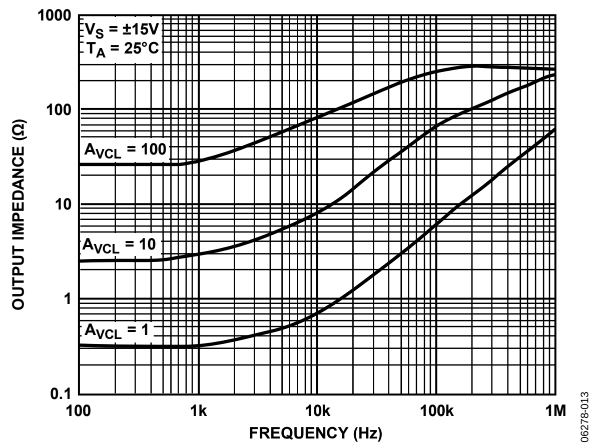


Figure 13. Closed-Loop Output Impedance vs. Frequency

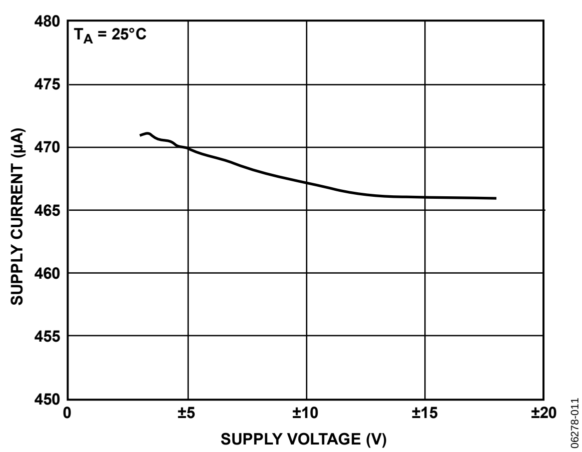


Figure 11. AD8682 Supply Current vs. Supply Voltage

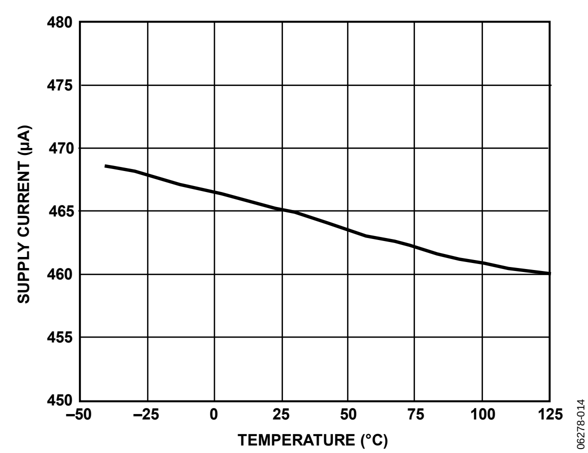


Figure 14. AD8682 Supply Current vs. Temperature

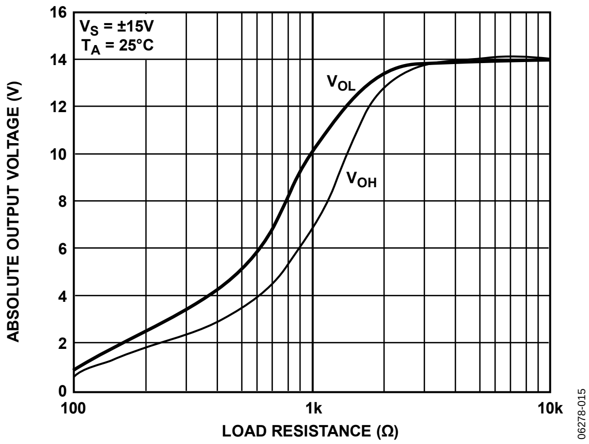


Figure 15. Absolute Output Voltage vs. Load Resistance

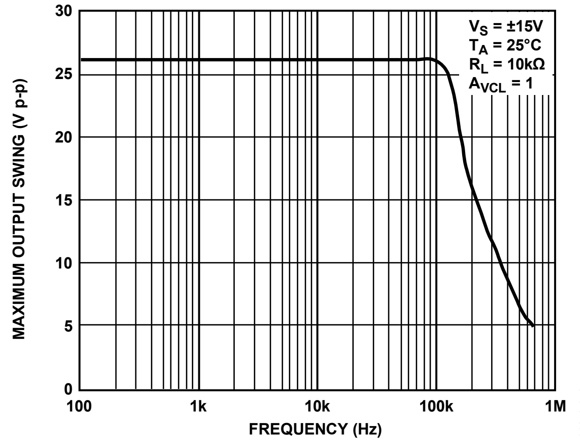


Figure 18. Maximum Output Swing vs. Frequency

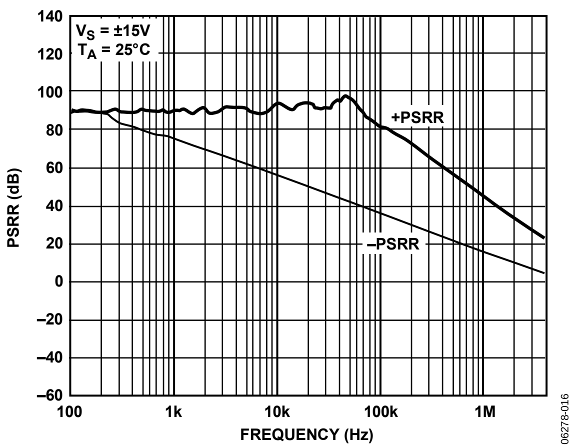


Figure 16. AD8682 PSRR vs. Frequency

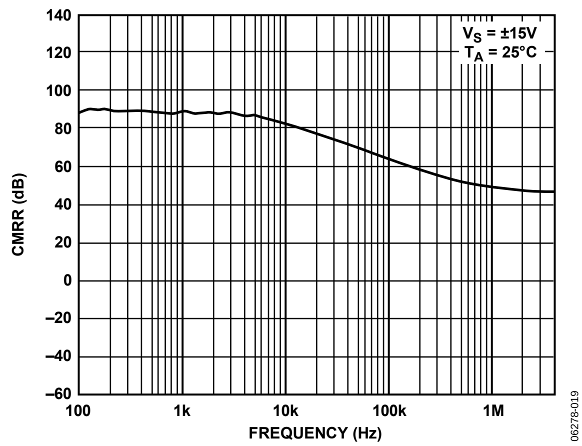


Figure 19. AD8682 CMRR vs. Frequency

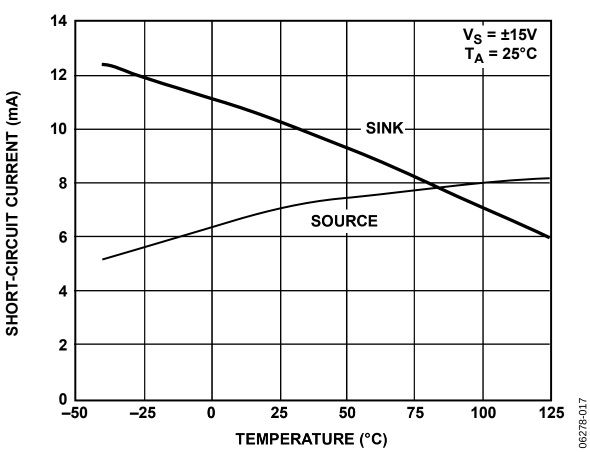


Figure 17. AD8682 Short-Circuit Current vs. Temperature

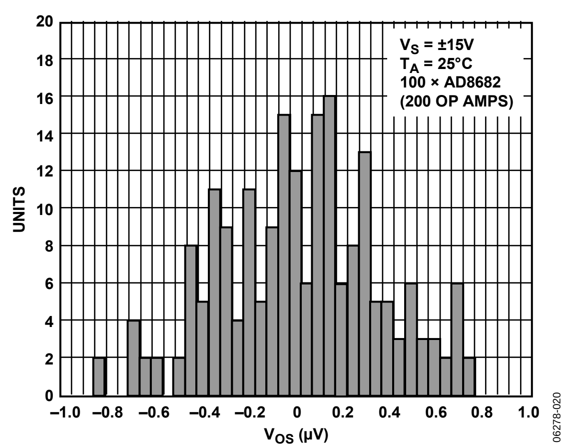


Figure 20. AD8682 VOS Distribution

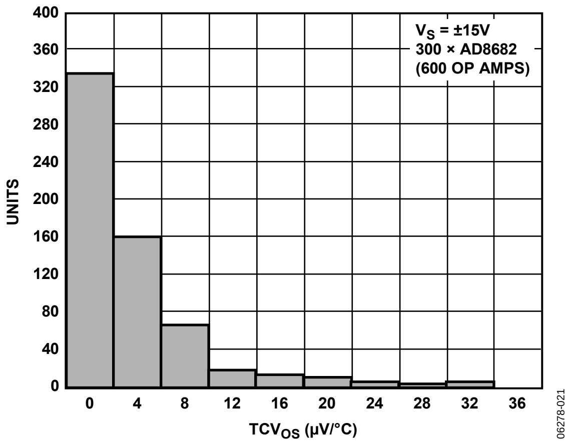


Figure 21. AD8682 TCVOS Distribution SOIC_N Package

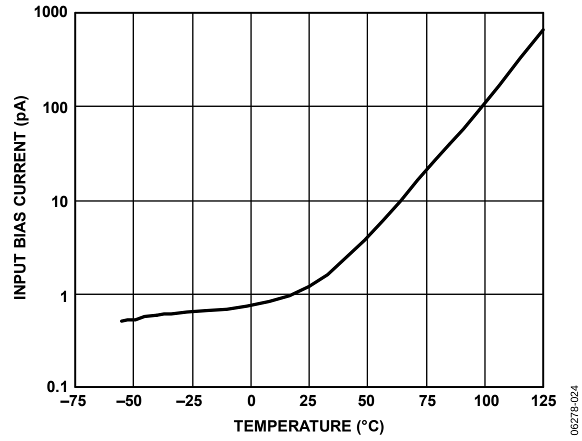


Figure 24. AD8684 Input Bias Current vs. Temperature

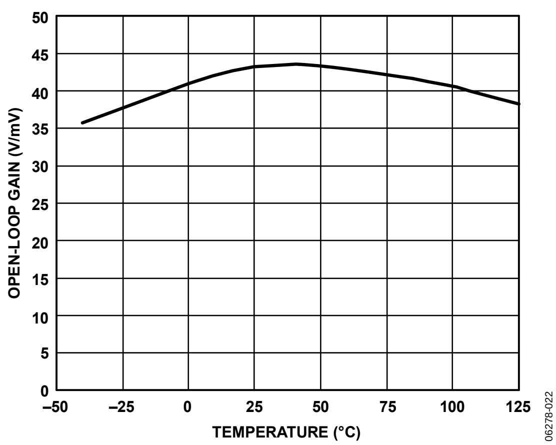


Figure 22. AD8684 Open-Loop Gain vs. Temperature

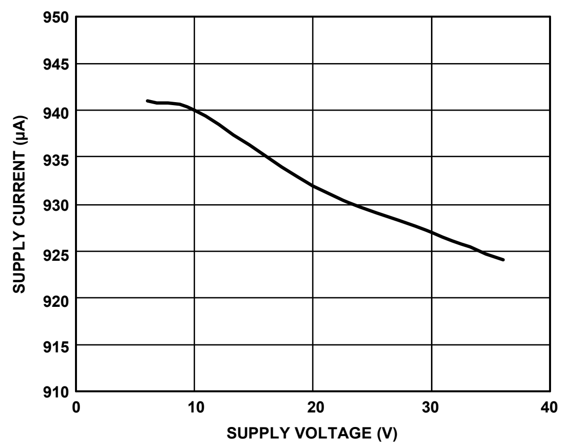


Figure 25. AD8684 Relative Supply Current vs. Supply Voltage

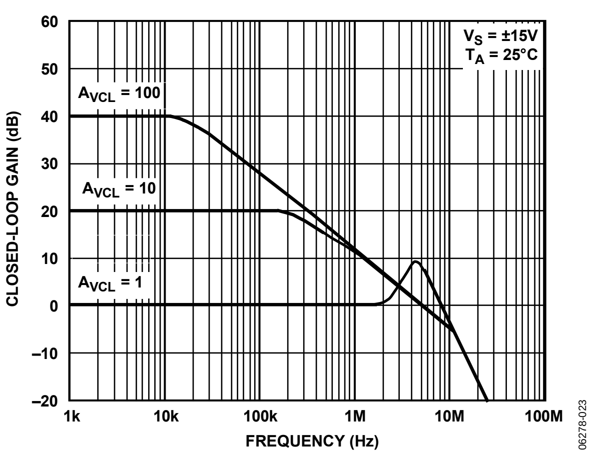


Figure 23. AD8684 Closed-Loop Gain vs. Frequency

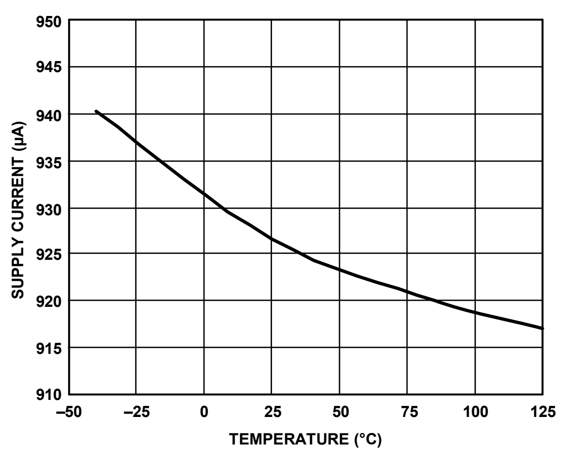


Figure 26. AD8684 Supply Current vs. Temperature

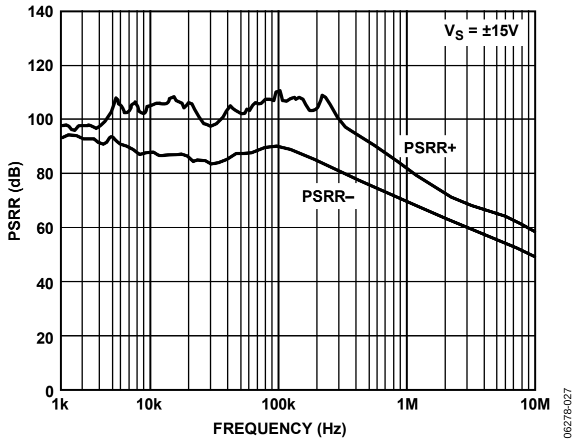


Figure 27. AD8684 PSRR vs. Frequency

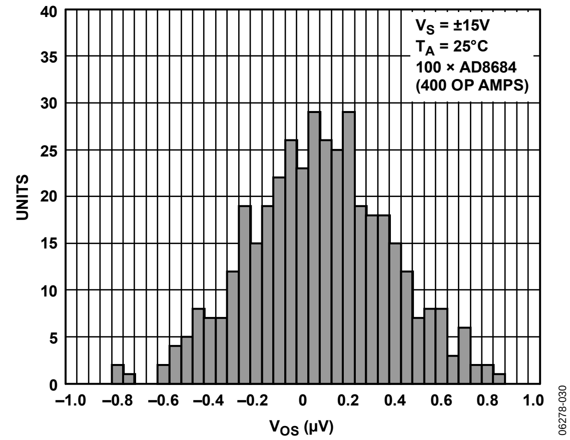


Figure 30. AD8684 VOS Distribution Package

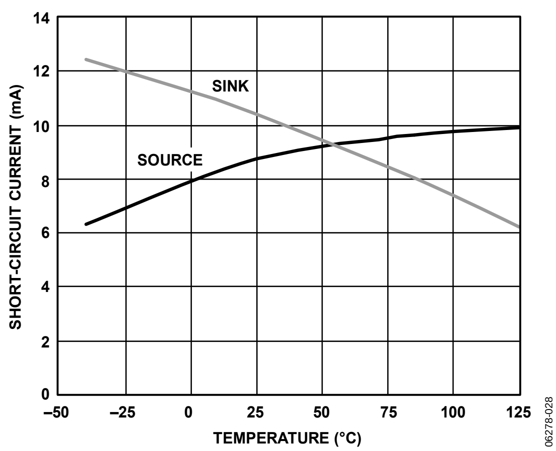


Figure 28. AD8684 Short-Circuit Current vs. Temperature

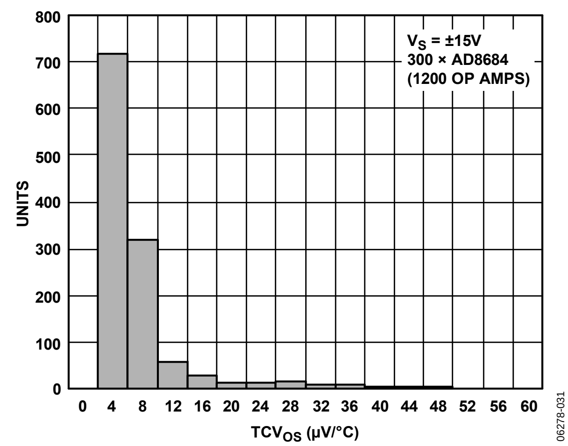


Figure 31. AD8684 TCVOS Distribution Package

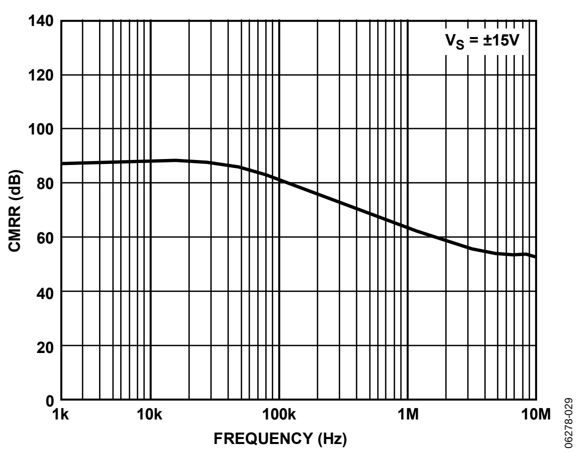


Figure 29. AD8684 CMRR vs. Frequency

APPLICATIONS INFORMATION

The AD8682 and AD8684 are dual and quad JFET op amps that are optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery-powered or low power applications that require above average performance. Applications benefiting from this performance combination include telecommunications, geophysical exploration, portable medical equipment, and navigational instrumentation.

HIGH-SIDE SIGNAL CONDITIONING

There are many applications requiring the sensing of signals near the positive rail. The AD8682 and the AD8684 were tested and are guaranteed over a common-mode range (-11 V ≤ V_{CM} ≤ $+15$ V) that includes the positive supply.

The AD8682/AD8684 are commonly used in the sensing of power supply currents and in current sensing applications, such as the partial circuit shown in Figure 32. In this circuit, the voltage drop across a low value resistor, such as the 0.1 Ω shown here, is amplified and compared to 7.5 V. The output can then be used for current limiting.

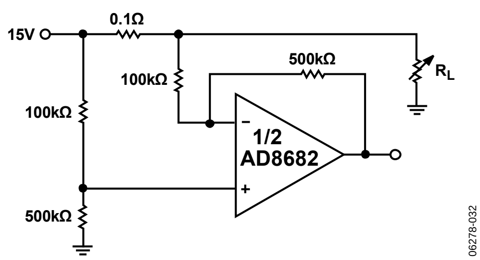


Figure 32. High-Side Signal Conditioning

PHASE INVERSION

Most JFET input amplifiers invert the phase of the input signal if either input exceeds the input common-mode range. For the AD8682/AD8684, a negative signal in excess of 11 V causes phase inversion. This is caused by saturation of the input stage leading to the forward-biasing of a gate-drain diode. Phase reversal in AD8682/AD8684 can be prevented by using Schottky diodes to clamp the input terminals to each other and to the supplies. In the simple buffer circuit below, D1 protects the op amp against phase reversal. R1, D2, and D3 limit the input current when the input exceeds the supply rail. The resistor should be selected to limit the amount of input current below the absolute maximum rating.

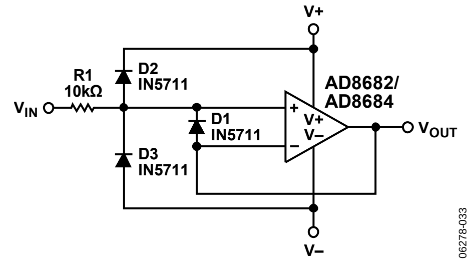


Figure 33. Phase Reversal Solution Circuit

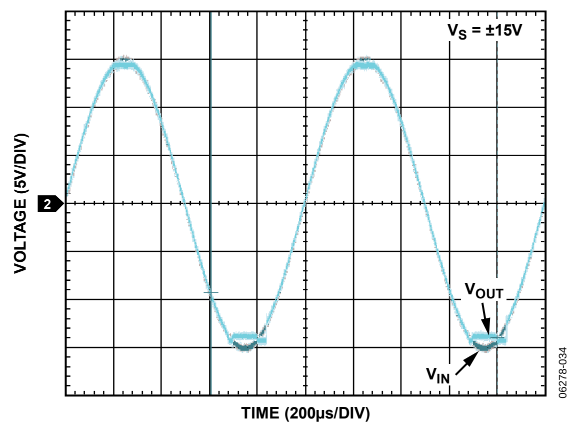


Figure 34. No Phase Reversal

ACTIVE FILTERS

The wide bandwidth and high slew rates of the AD8682/AD8684 make either one an excellent choice for many filter applications.

There are many active filter configurations, but the four most popular configurations are: Butterworth, elliptic, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic, as shown in Table 4.

Table 4.

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good		Maximum flat	
Chebyshev	Good	Moderate	Nonlinear	Equal ripple	
Elliptic	Best	Poor		Equal ripple	Equal ripple
Bessel (Thompson)	Poor	Best	Linear		

PROGRAMMABLE STATE VARIABLE FILTER

The circuit shown in Figure 35 can be used to accurately program the Q factor; the cutoff frequency (f_C); and the gain of a two-pole state variable filter. The AD8684 has been used in this design because of its high bandwidth, low power, and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are used in voltage mode; therefore, many values are dependent on the accuracy of the DAC only and not on the absolute values of the DAC resistive ladders. As a result, this makes the circuit unusually accurate for a programmable filter.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation × R1 determines the amount of signal current that charges the integrating capacitor, C1.

This cutoff frequency can be expressed as

$$f_C = \frac{1}{2\pi R1C1}\left(\frac{D1}{256}\right)$$

where $D1$ is the digital code for the DAC.

DAC 3 is used to set the gain. The gain equation is

$$Gain = \frac{R4}{R5}\left(\frac{D3}{256}\right)$$

DAC 2 is used to set the Q of the circuit. Adjusting this DAC controls the amount of feedback from the band-pass node to the input summing node. Note that the digital value of the DAC is in the numerator; therefore, zero code is not a valid operating point.

$$Q = \frac{R2}{R3}\left(\frac{256}{D2}\right)$$

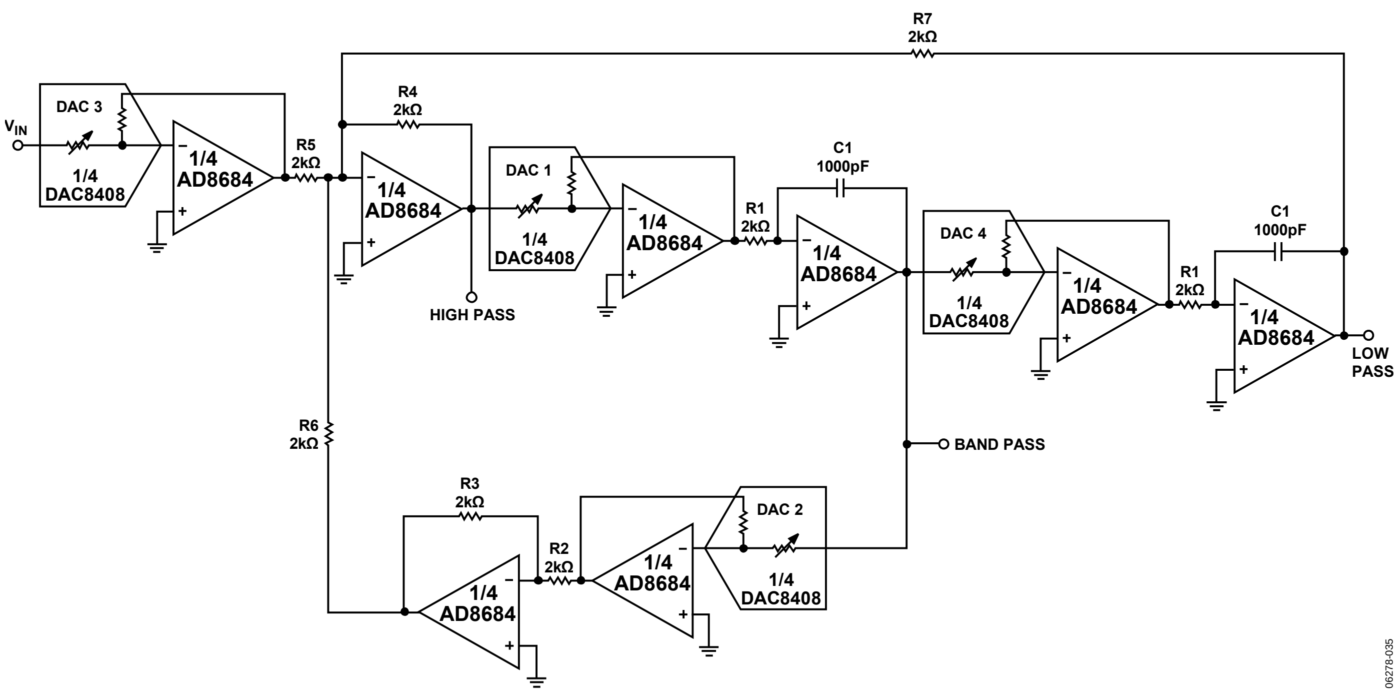


Figure 35. Programmable State Variable Filter

OUTLINE DIMENSIONS

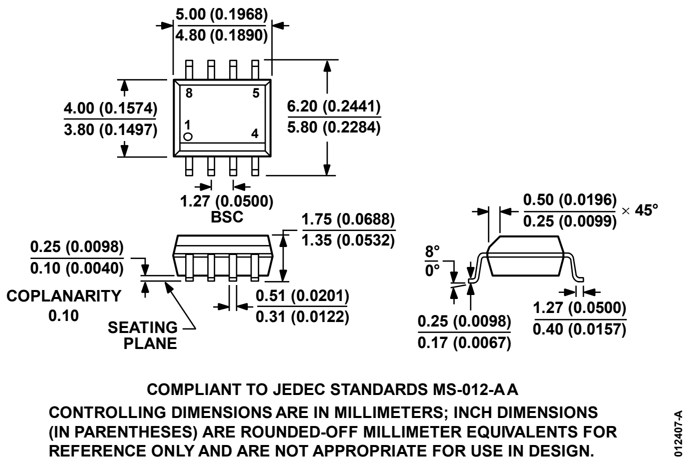


Figure 36. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

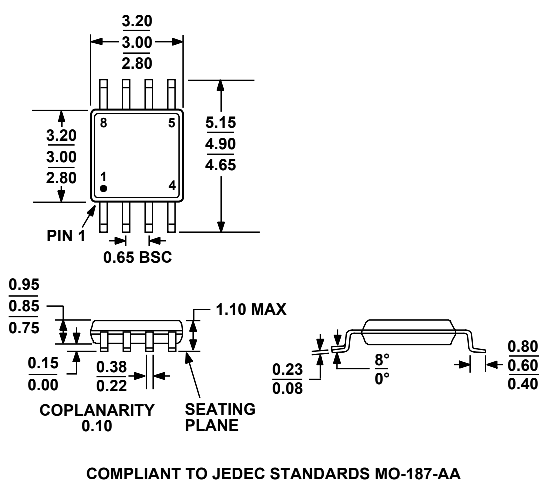


Figure 37. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

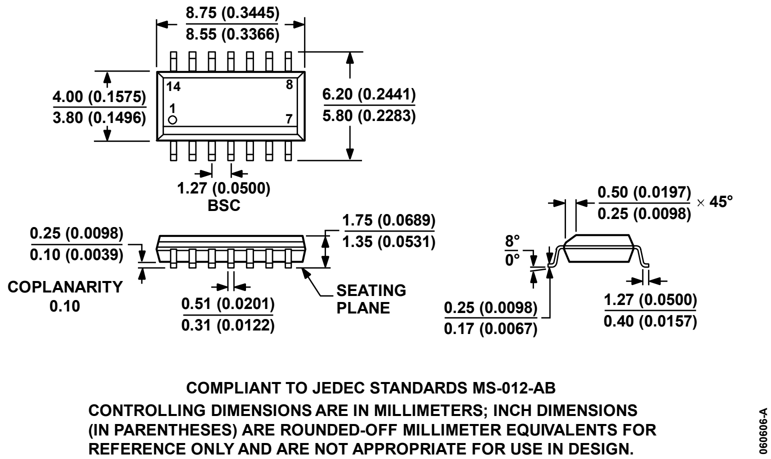


Figure 38. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

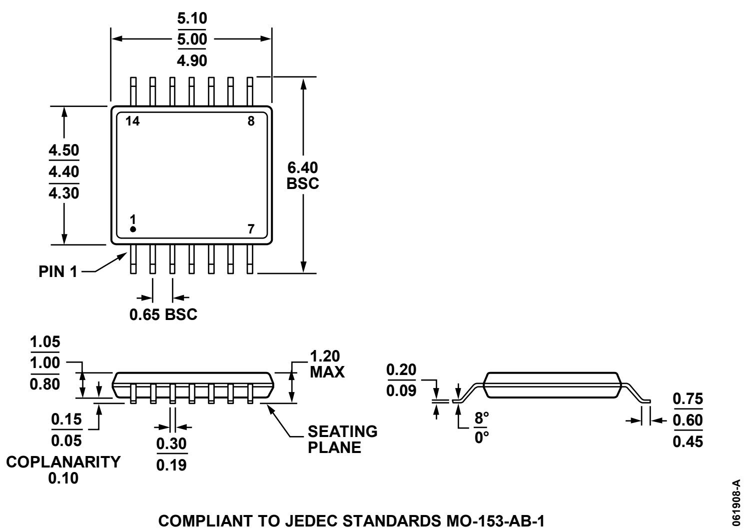


Figure 39. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8682ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8682ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8682ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8682ARMZ-R2[1]	−40°C to +85°C	8-Lead MSOP	RM-8	A1K
AD8682ARMZ-REEL[1]	−40°C to +85°C	8-Lead MSOP	RM-8	A1K
AD8684ARZ[1]	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8684ARZ-REEL[1]	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8684ARZ-REEL7[1]	−40°C to +85°C	14-Lead SOIC_N	R-14	
AD8684ARUZ[1]	−40°C to +85°C	14-Lead TSSOP	RU-14	
AD8684ARUZ-REEL[1]	−40°C to +85°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

ANALOG DEVICES

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