ANALOG DEVICES

Precision JFET-Input Operational Amplifiers

OP-15/OP-16/OP-17

FEATURES (All Devices)

- **Significant Performance Advantages over LF155, 156 and 157 Devices.**
- **Low Input Offset Voltage .... 500μV Max**
- **Low Input Offset Voltage Drift .... 2.0μV/° C**
- **Minimum Slew Rate Guaranteed on All Models**
- **Temperature-Compensated Input Bias Currents**
- **Guaranteed Input Bias Current @ 125° C**
- **Bias Current Specified WARMED UP Over Temperature**
- **Internal Compensation**
- **Low Input Noise Current .... 0.01pA/√Hz**
- **High Common-Mode Rejection Ratio 100dB**
- **Models With MIL-STD-883 Processing Available**
- **125° C Temperature Tested DICE**

OP-15

- **156 Speed With 155 Dissipation .... (80mW Typ)**
- **Wide Bandwidth 6MHz**
- **High Slew Rate 13V/μs**
- **Fast Settling to ±0.1% 1200ns**
- **Available in Die Form**

OP-16

- **Higher Slew Rate 25V/μs**
- **Faster Settling to ±0.1% 900ns**
- **Wider Bandwidth 8MHz**
- **Available in Die Form**

OP-17

- **Highest Slew Rate 60V/μs**
- **Fastest Settling to ±0.1% 600ns**
- **Highest Gain Bandwidth Product (A_{VCL} = 5 Min) 30MHz**
- **Available in Die Form**

GENERAL DESCRIPTION

The PMI JFET-input series of devices offer clear advantages over industry-generic devices and are superior in both cost and performance to many dielectrically-isolated and hybrid op amps. All devices offer offset voltages as low as 0.5mV with TCV_{OS} guaranteed to 5μV/°C. A unique input bias cancellation circuit reduces the I_B by a factor of 10 over conventional designs. In addition, PMI specifies I_B and I_{OS} with the devices warmed up and operating at 25°C ambient.

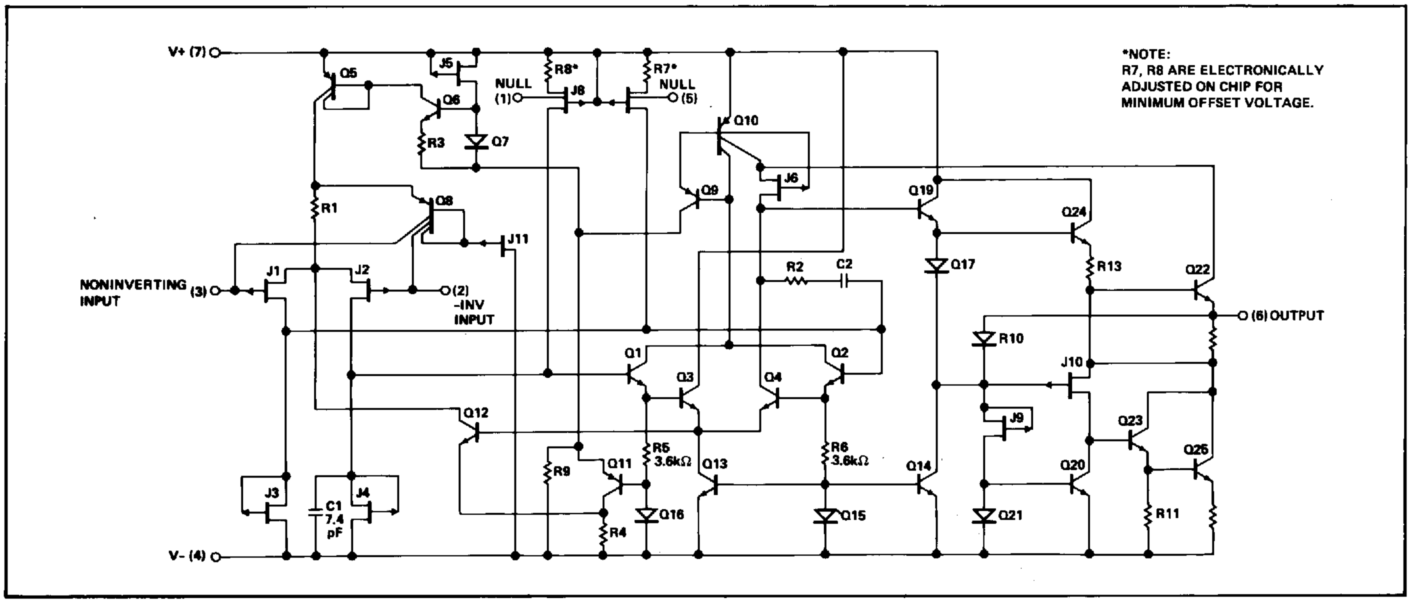
These devices were designed to provide real precision performance along with high speed. Although they can be nulled, the design objective was to provide low offset-voltage without nulling. Systems generally become more cost effective as the number of trim circuits is decreased. PMI achieves this performance by use of an improved Bipolar compatible JFET process coupled with on-chip, zener-zap offset trimming.

The OP-15 provides an excellent combination of high speed and low input offset voltage. In addition, the OP-15 offers the speed of the 156A op amp with the power dissipation of a 155A. The combination of a low input offset voltage of 500μV, slew rate of 13V/μs, and settling time of 1200ns to 0.1% makes the OP-15 an op amp of both precision and speed. The additional features of low supply current coupled with an input bias current of 9nA at 125° C ambient (not junction) temperature makes the OP-15 ideal for a wide range of applications.

The OP-16 features a slew rate of 25V/μs and a settling time of 900ns to 0.1% which represents a significant improvement in speed over the 156. Also, the OP-16 has all the DC features of the OP-15.

The OP-17 has a slew rate of 60V/μs and is the best choice for applications requiring high closed-loop gain with high speed. See the OP-42 data sheet for unity gain applications and the OP-215 data sheet for a dual configuration of the OP-15.

SIMPLIFIED SCHEMATIC


V+ (7)
V- (4)
NONINVERTING INPUT (3)
(2) -INV INPUT
NULL (1)
NULL (5)
(6) OUTPUT
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q19 Q20 Q21 Q22 Q23 Q24 Q25
J1 J2 J3 J4 J5 J6 J8 J9 J10 J11
R1 R2 R3 R4 R5 3.6kΩ R6 3.6kΩ R7* R8* R9 R10 R11 R13
C1 7.4 pF
C2

*NOTE: R7, R8 ARE ELECTRONICALLY ADJUSTED ON CHIP FOR MINIMUM OFFSET VOLTAGE.

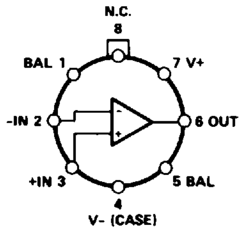
ORDERING INFORMATION [†]

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	SO 8-PIN	OPERATING TEMPERATURE RANGE
0.5	OP15AJ*	OP15AZ*	–	–	MIL
	OP16AJ*	–	–	–	
	OP17AJ*	OP17AZ*	–	–	
0.5	OP15EJ	OP15EZ	–	–	COM
	OP16EJ	OP16EZ	–	–	
	OP17EJ	OP17EZ	–	–	
1.0	OP15BJ/883	OP15BZ/883	–	–	MIL
	OP16BJ/883	OP16BZ/883	–	–	
	OP17BJ*	OP17BZ	–	–	
1.0	OP15FJ	OP15FZ	OP15FP	–	COM
	OP16FJ	OP16FZ	OP16FP	–	
	–	–	OP17FP	–	
3.0	–	OP17CZ/883	–	–	MIL
	OP17CJ/883C	–	–	–	
3.0	OP15GJ	OP15GZ	OP15GP	OP15GS	XIND
	OP16GJ	OP16GZ	OP16GP	OP16GS	
	OP17GJ	OP17GZ	OP17GP	OP17GS	

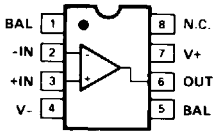
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

PIN CONNECTIONS

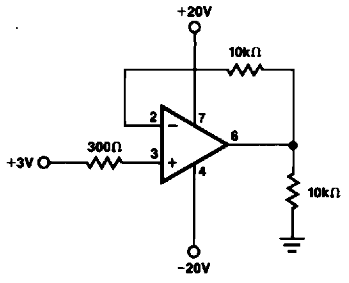


TO-99
(J-Suffix)



8-PIN CERDIP
(Z-Suffix)
8-PIN PLASTIC DIP
(P-Suffix)
8-PIN SO
(S-Suffix)

BURN-IN CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- All Devices Except C, G (Packaged) & GR Grades ..... ±22V
- C, G (Packaged) & GR Grades ..... ±18V

Operating Temperature
- A, B, & C Grades ..... −55°C to +125°C
- E & F Grades ..... 0°C to +70°C
- G Grade ..... −40°C to +85°C

Maximum Junction Temperature ..... +150°C

DICE Junction Temperature (T_j) ..... −65°C to +150°C

Differential Input Voltage
- All Devices Except C, G (Packaged) & GR Grades ..... ±40V
- C, G (Packaged) & GR Grades ..... ±30V

Input Voltage (Note 2)
- All Devices Except C, G (Packaged) & GR Grades ..... ±20V
- C, G (Packaged) & GR Grades ..... ±16V

Input Voltage
- OP-15A, OP-15B, OP-15E, OP-15F ..... ±20V
- OP-15G ..... ±16V
- OP-16A, OP-16B, OP-16E, OP-16F ..... ±20V
- OP-16C, OP-16G ..... ±16V
- OP-17A, OP-17B, OP-17E, OP-17F ..... ±20V
- OP-17C, OP-17G ..... ±16V

Output Short-Circuit Duration ..... Indefinite

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power-supply voltage.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15A/E OP-16A/E OP-17A/E MIN	 TYP	 MAX	OP-15B/F OP-16B/F OP-17B/F MIN	 TYP	 MAX	OP-15G OP-16C/G OP-17C/G MIN	 TYP	 MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)	OP-15	—	3	10	—	6	20	—	12	50	pA
		Device Operating		—	5	22	—	10	40	—	20	100	
		$T_j = 25°C$ (Note 1)	OP-16/OP-17	—	3	10	—	6	20	—	12	50	
		Device Operating		—	5	25	—	10	50	—	20	125	
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)	OP-15	—	±15	±50	—	±30	±100	—	±60	±200	pA
		Device Operating		—	±18	±110	—	±40	±200	—	±80	±400	
		$T_j = 25°C$ (Note 1)	OP-16/OP-17	—	±15	±50	—	±30	±100	—	±60	±200	
		Device Operating		—	±20	±130	—	±40	±250	—	±80	±500	
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm10V$		100	240	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V
		$R_L = 2k\Omega$		±11	±12.7	—	±11	±12.7	—	±11	±12.7	—	
Supply Current	I_{SY}		OP-15	—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
			OP-16/OP-17	—	4.6	7.0	—	4.6	7.0	—	4.8	8.0	
Slew Rate	SR	$A_{VCL} = +1$ (Note 3)	OP-15	10	13	—	7.5	11	—	5	9	—	V/µs
			OP-16	18	25	—	12	21	—	9	17	—	
		$A_{VCL} = +5$ (Note 3)	OP-17	45	60	—	35	50	—	25	40	—	
Gain Bandwidth Product	GBW	(Note 3)	OP-15	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
			OP-16	6.0	8.0	—	5.5	7.6	—	5.0	7.2	—	
			OP-17	20	30	—	15	28	—	11	26	—	
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	—	14	—	—	13	—	—	12	—	MHz
			OP-16	—	19	—	—	18	—	—	17	—	
		$A_{VCL} = +5$	OP-17	—	11	—	—	10	—	—	9	—	
Settling Time	t_S	to 0.01%	OP-15	—	4.5	—	—	4.5	—	—	4.7	—	µs
		to 0.05% (Note 2)		—	1.5	—	—	1.5	—	—	1.6	—	
		to 0.10%		—	1.2	—	—	1.2	—	—	1.3	—	
		to 0.01%	OP-16	—	3.8	—	—	3.8	—	—	4.0	—	
		to 0.05% (Note 2)		—	1.2	—	—	1.2	—	—	1.3	—	
		to 0.10%		—	0.9	—	—	0.9	—	—	1.0	—	
		to 0.01%	OP-17	—	1.5	—	—	1.5	—	—	1.6	—	
		to 0.05% (Note 4)		—	0.7	—	—	0.7	—	—	0.8	—	
		to 0.10%		—	0.6	—	—	0.6	—	—	0.7	—	
Input Voltage Range	IVR			±10.5	—	—	±10.5	—	—	±10.3	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10.5V$		86	100	—	86	100	—	—	—	—	dB
		$V_{CM} = \pm10.3V$		—	—	—	—	—	—	82	96	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm10V$ to $\pm18V$		—	10	51	—	10	51	—	—	—	µV/V
		$V_S = \pm10V$ to $\pm15V$		—	—	—	—	—	—	—	10	80	
Input Noise Voltage Density	e_n	$f_O = 100Hz$		—	20	—	—	20	—	—	20	—	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$		—	15	—	—	15	—	—	15	—	
Input Noise Current Density	i_n	$f_O = 100Hz$		—	0.01	—	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
		$f_O = 1000Hz$		—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}			—	3	—	—	3	—	—	3	—	pF

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.
4. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

				OP-15A OP-16A OP-17A			OP-15B OP-16B OP-17B			OP-16C OP-17C			
PARAMETER	**SYMBOL**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV
Average Input Offset Voltage Drift		(Note 2)											
Without External Trim	TCV_{OS}			—	2	5	—	3	10	—	4	15	μV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$		—	2	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_j = 125°C$	OP-15	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		$T_A = 125°C$ Device Operating		—	0.8	7.0	—	1.2	11	—	1.5	17	
		$T_j = 125°C$	OP-16/OP-17	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	
		$T_A = 125°C$ Device Operating		—	1.0	8.5	—	1.3	14.5	—	1.7	22	
Input Bias Current (Note 1)	I_B	$T_j = 125°C$	OP-15	—	±1.2	±5.0	—	±1.5	±7.5	—	±1.8	±10	nA
		$T_A = 125°C$ Device Operating		—	±1.7	±9.0	—	±2.2	±14	—	±2.7	±19	
		$T_j = 125°C$	OP-16/OP-17	—	±1.2	±5.0	—	±1.5	±7.5	—	±1.8	±10	
		$T_A = 125°C$ Device Operating		—	±2.0	±11	—	±2.5	±18	—	±3.0	±25	
Input Voltage Range	IVR			±10.4	—	—	±10.4	—	—	±10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$		85	97	—	85	97	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$		—	—	—	—	—	—	80	93	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	15	57	—	15	57	—	—	—	μV/V
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	23	100	
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$		35	120	—	30	110	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $0°C \leq T_A \leq 70°C$ for E and F, $-40 \leq T_A \leq +85°C$ for G grade, unless otherwise noted.

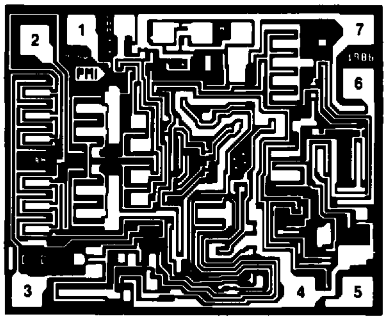
PARAMETER	SYMBOL	CONDITIONS		OP-15E OP-16E OP-17E			OP-15F OP-16F OP-17F			OP-15G OP-16G OP-17G			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 2)		
Without External Trim	TCV_{OS}			—	2	5	—	3	10	—	4	30	μV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$		—	2	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_j = 70°C$	OP-15	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = 70°C$ Device Operating		—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	
		$T_j = 70°C$	OP-16/OP-17	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	
		$T_A = 70°C$ Device Operating		—	0.07	0.70	—	0.10	1.1	—	0.15	1.7	
Input Bias Current (Note 1)	I_B	$T_j = 70°C$	OP-15	—	±0.10	±0.40	—	±0.12	±0.60	—	±0.14	±0.80	nA
		$T_A = 70°C$ Device Operating		—	±0.13	±0.75	—	±0.16	±1.1	—	±0.19	±1.5	
		$T_j = 70°C$	OP-16/OP-17	—	±0.10	±0.40	—	±0.12	±0.60	—	±0.14	±0.80	
		$T_A = 70°C$ Device Operating		—	±0.15	±0.90	—	±0.20	±1.4	—	±0.25	±2.0	
Input Voltage Range	IVR			±10.4	—	—	±10.4	—	—	±10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10.4V$		85	98	—	85	98	—	—	—	—	dB
		$V_{CM} = \pm10.25V$		—	—	—	—	—	—	80	94	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm10V$ to $\pm18V$		—	13	57	—	13	57	—	—	—	μV/V
		$V_S = \pm10V$ to $\pm15V$		—	—	—	—	—	—	—	20	100	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm10V$		65	200	—	50	180	—	35	160	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

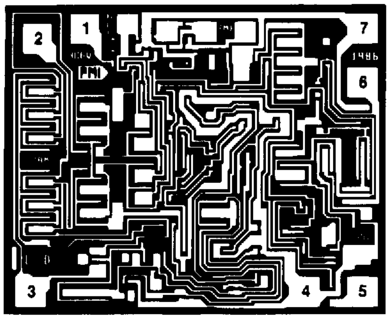
OP-15



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils (1.73 × 1.42mm, 2.46 sq. mm)

1. **BALANCE**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **V−**
5. **BALANCE**
6. **OUTPUT**
7. **V+**

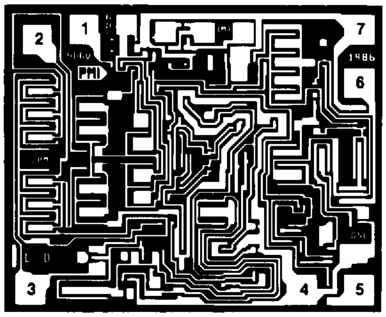
OP-16



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils (1.73 × 1.42mm, 2.46 sq. mm)

1. **BALANCE**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **V−**
5. **BALANCE**
6. **OUTPUT**
7. **V+**

OP-17



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils (1.73 × 1.42mm, 2.46 sq. mm)

1. **BALANCE**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **V−**
5. **BALANCE**
6. **OUTPUT**
7. **V+**

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-15/16/17N, OP-15/16/17G and OP-15/16/17GR devices; $T_A = 125°C$ for OP-15/16/17NT and OP-15/16/17GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15NT OP-16NT OP-17NT LIMIT	OP-15N OP-16N OP-17N LIMIT	OP-15GT OP-16GT OP-17GT LIMIT	OP-15G OP-16G OP-17G LIMIT	OP-15GR OP-16GR OP-17GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	0.9	0.5	2.0	1.0	3.0	mV MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 2k\Omega$	35	100	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.4	±10.5	±10.4	±10.5	±10.3	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	86	85	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$ $V_S = \pm 10V$ to $\pm 15V$	57 —	51 —	57 —	51 —	— 80	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 —	±12 ±11	±12 —	±12 ±11	±12 ±11	V MIN
Supply Current	I_{SY}	OP-15 OP-16, OP-17	— —	4 7	— —	4 7	5 8	mA MAX
Input Bias Current	I_B	OP-15 OP-16, OP-17	±9 ±11	— —	±14 ±18	— —	— —	nA MAX
Input Offset Current	I_{OS}	OP-15 OP-16, OP-17	7.0 8.5	— —	11.0 14.5	— —	— —	nA MAX

NOTES:

For 25° C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

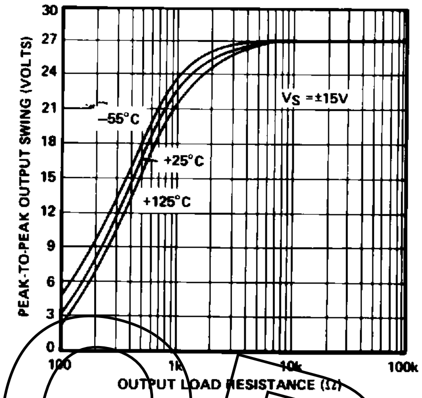
PARAMETER	SYMBOL	CONDITIONS		OP-15NT OP-16NT OP-17NT TYPICAL	OP-15N OP-16N OP-17N TYPICAL	OP-15GT OP-16GT OP-17GT TYPICAL	OP-15G OP-16G OP-17G TYPICAL	OP-15GR OP-16GR OP-17GR TYPICAL	UNITS
Average Input Offset Drift Unnulled	TCV_{OS}			2	2	3	3	4	μV/°C
Average Input Offset Drift Nulled	TCV_{OSn}	$R_P = 100k\Omega$		2	2	3	3	4	μV/°C
Input Offset Current	I_{OS}			3	3	3	3	3	pA
Input Bias Current	I_B			±15	±15	±15	±15	±15	pA
Slew Rate	SR	$A_{VCL} = +1$	OP-15	13	13	11	11	9	V/μs
			OP-16	25	25	21	21	17	
		$A_{VCL} = +5$	OP-17	60	60	50	50	40	
Settling Time (see settling time test circuits)	t_S	to 0.01%	OP-15	4.5	4.5	4.5	4.5	4.7	μs
		to 0.05%		1.5	1.5	1.5	1.5	1.6	
		to 0.10%		1.2	1.2	1.2	1.2	1.3	
		to 0.01%	OP-16	3.8	3.8	3.8	3.8	4.0	
		to 0.05%		1.2	1.2	1.2	1.2	1.3	
		to 0.10%		0.9	0.9	0.9	0.9	1.0	
		to 0.01%	OP-17	1.5	1.5	1.5	1.5	1.6	
		to 0.05%		0.7	0.7	0.7	0.7	0.8	
		to 0.10%		0.6	0.6	0.6	0.6	0.7	
Gain Bandwidth Product	GBW		OP-15	6.0	6.0	5.7	5.7	5.4	MHz
			OP-16	8.0	8.0	7.6	7.6	7.2	
			OP-17	30	30	28	28	26	
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	14	14	13	13	12	MHz
			OP-16	19	19	18	18	17	
		$A_{VCL} = +5$	OP-17	11	11	10	10	9	
Input Noise Voltage Density	e_n	f = 100Hz		20	20	20	20	20	$nV/\sqrt{Hz}$
		f = 1000Hz		15	15	15	15	15	
Input Noise Current Density	i_n	f = 100Hz		0.01	0.01	0.01	0.01	0.01	$pA/\sqrt{Hz}$
		f = 1000Hz		0.01	0.01	0.01	0.01	0.01	
Input Capacitance	C_{IN}			3	3	3	3	3	pF

NOTES:

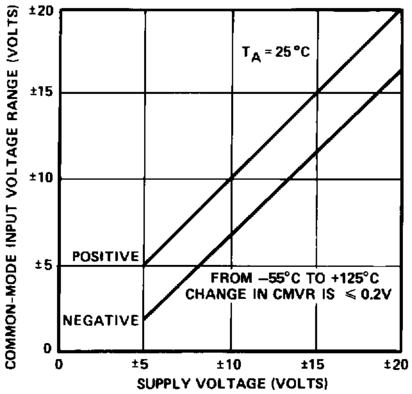
For 25° C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)

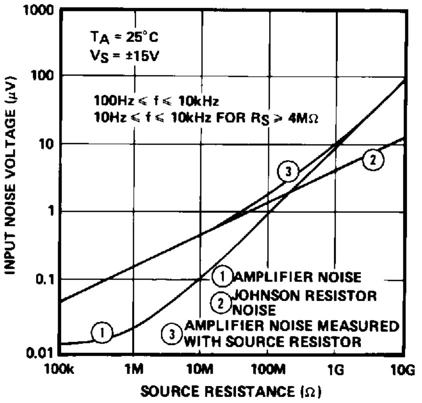
MAXIMUM OUTPUT SWING vs LOAD RESISTANCE



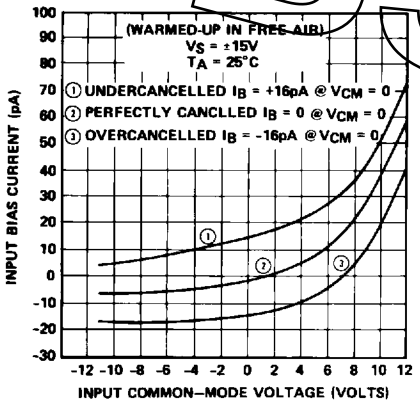
COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



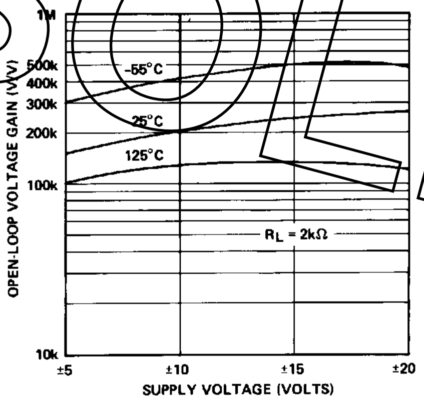
VOLTAGE NOISE vs SOURCE RESISTANCE



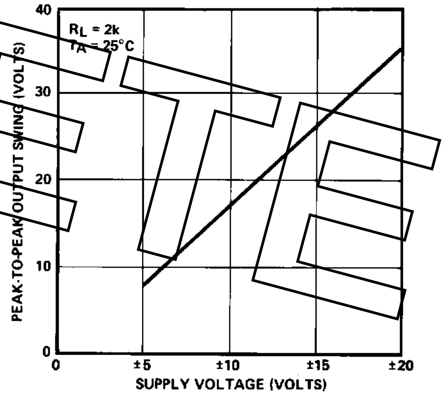
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



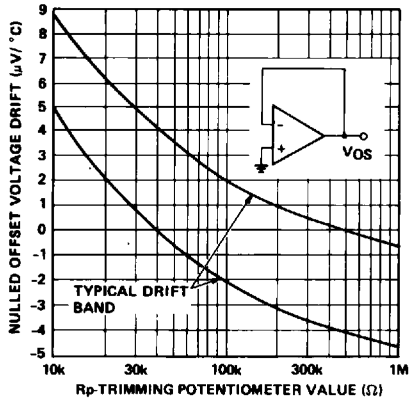
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



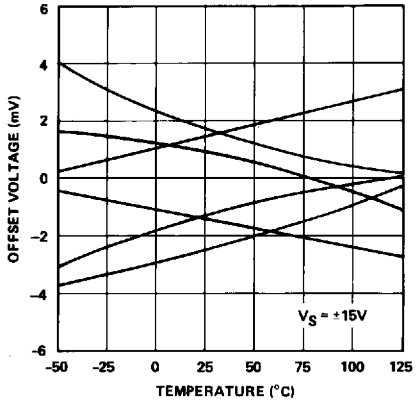
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



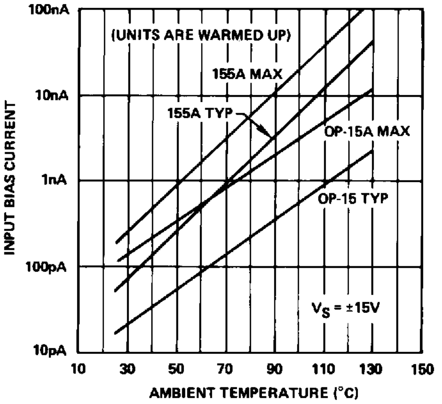
NULLED OFFSET VOLTAGE DRIFT vs POTENTIOMETER SIZE



OFFSET VOLTAGE DRIFT vs TEMPERATURE OF REPRESENTATIVE UNITS

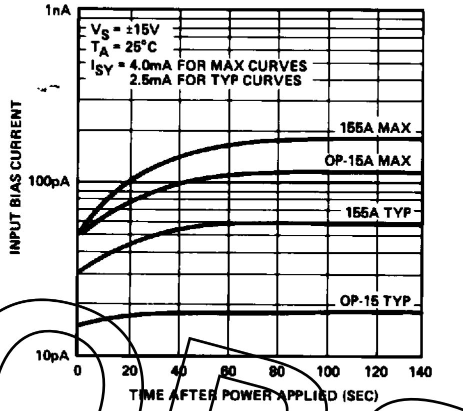


INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)

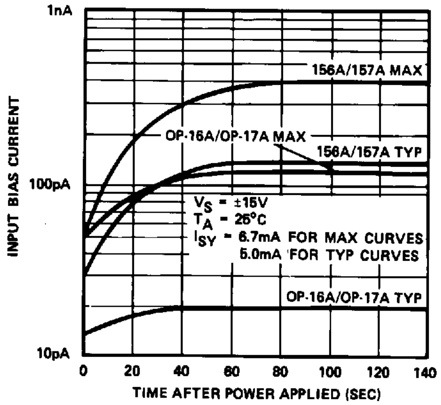


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)

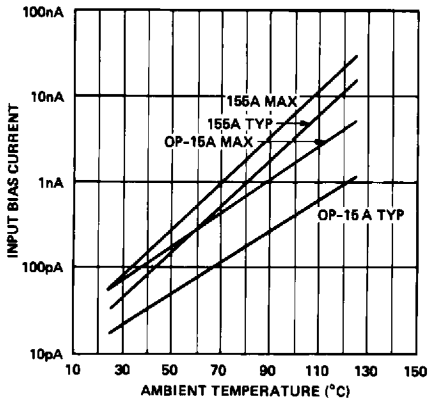
BIAS CURRENT vs TIME IN FREE AIR (OP-15)



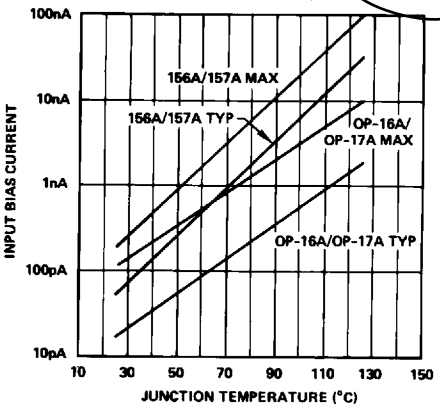
BIAS CURRENT vs TIME IN FREE AIR (OP-16/OP-17)



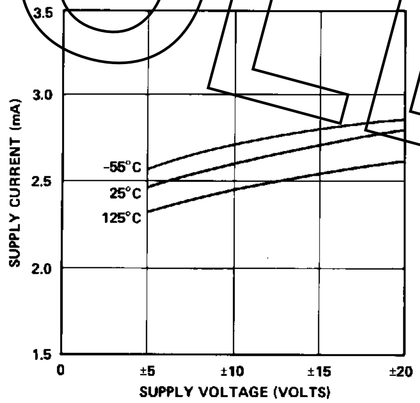
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR) (OP-15)



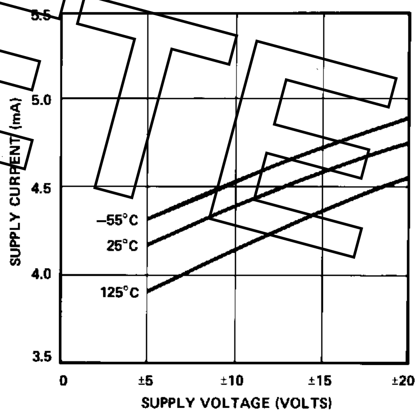
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR) (OP-16/OP-17)



SUPPLY CURRENT vs SUPPLY VOLTAGE (OP-15)

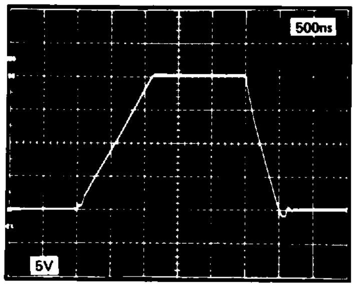


SUPPLY CURRENT vs SUPPLY VOLTAGE (OP-16/OP-17)

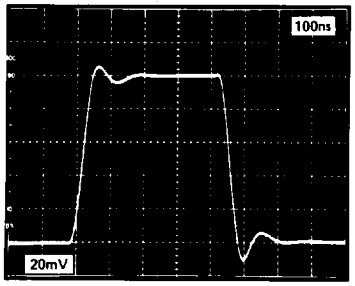


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)

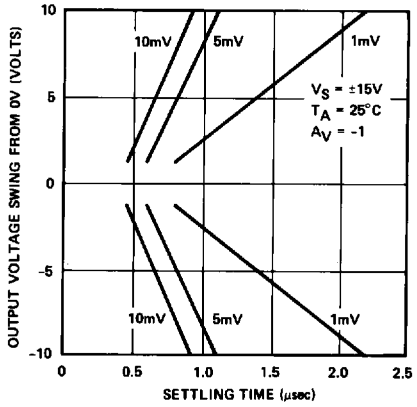
LARGE-SIGNAL TRANSIENT RESPONSE



SMALL-SIGNAL TRANSIENT RESPONSE

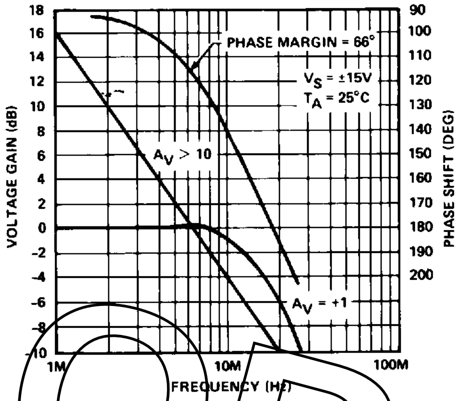


SETTLING TIME

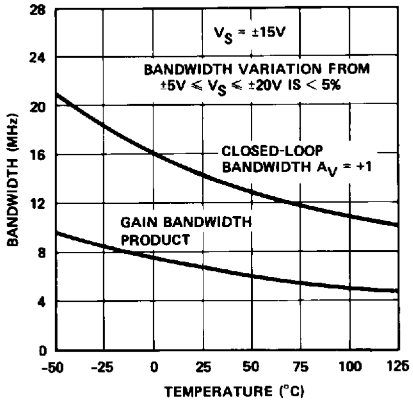


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)

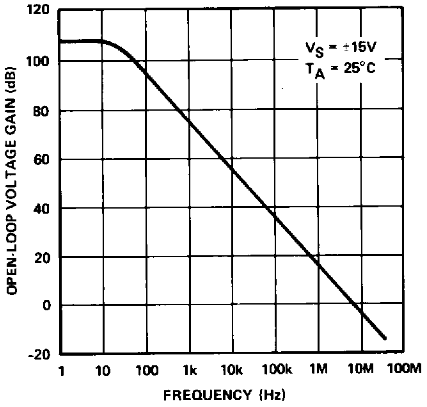
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



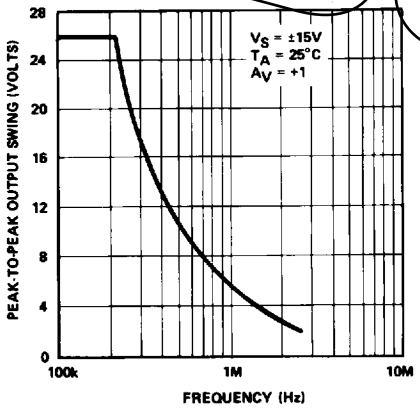
BANDWIDTH vs TEMPERATURE



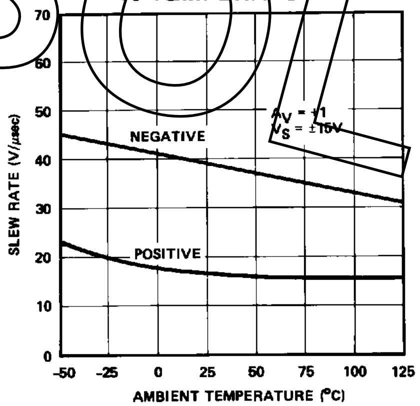
OPEN-LOOP GAIN vs FREQUENCY



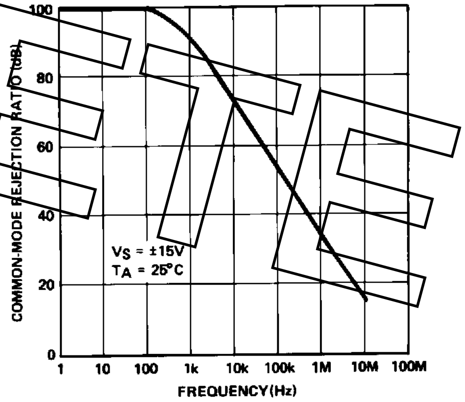
MAXIMUM OUTPUT SWING vs FREQUENCY



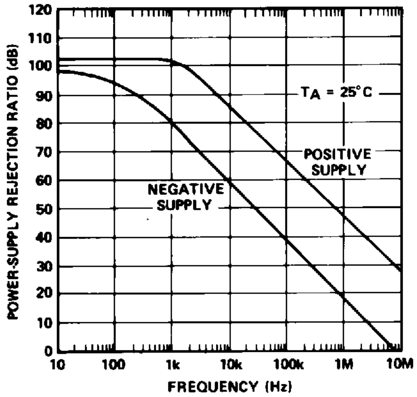
SLEW RATE vs TEMPERATURE



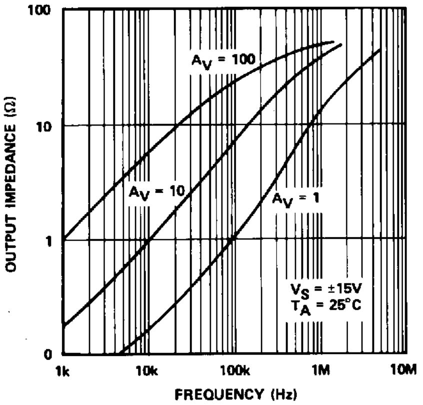
COMMON-MODE REJECTION RATIO vs FREQUENCY



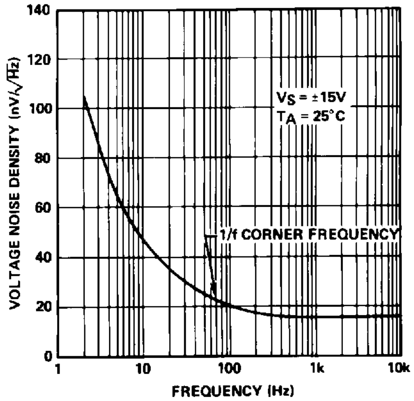
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

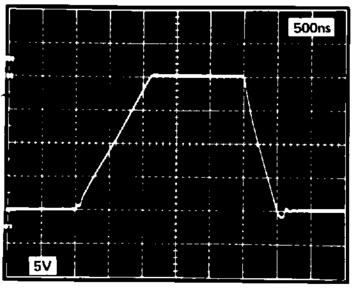


VOLTAGE NOISE DENSITY vs FREQUENCY

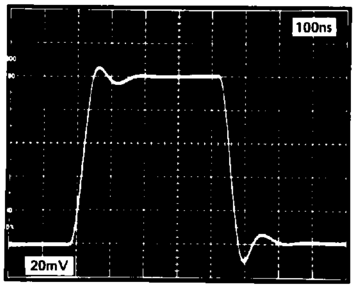


TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

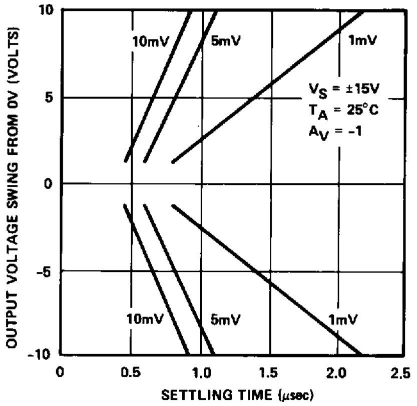
LARGE-SIGNAL TRANSIENT RESPONSE



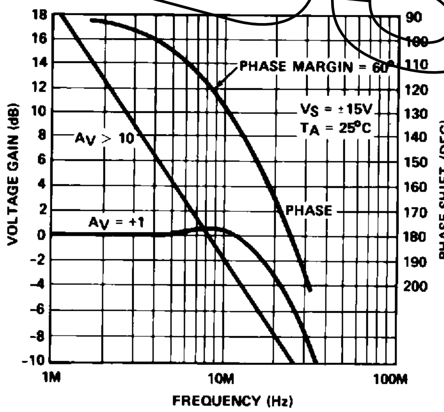
SMALL-SIGNAL TRANSIENT RESPONSE



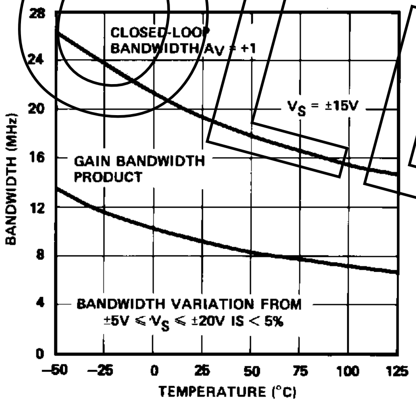
SETTLING TIME



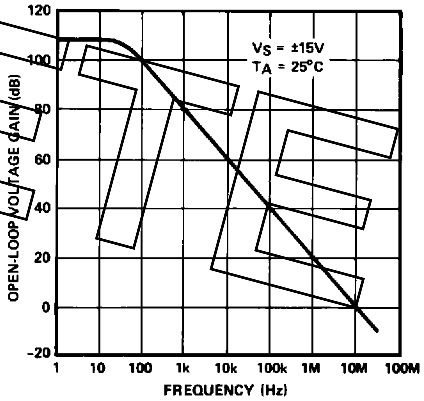
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



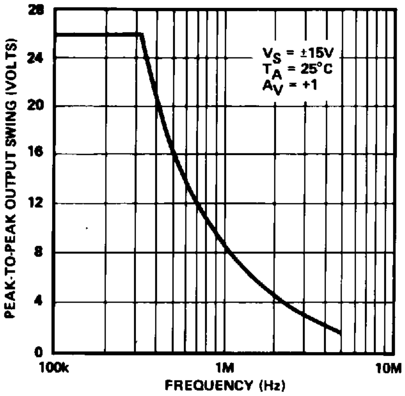
BANDWIDTH vs TEMPERATURE



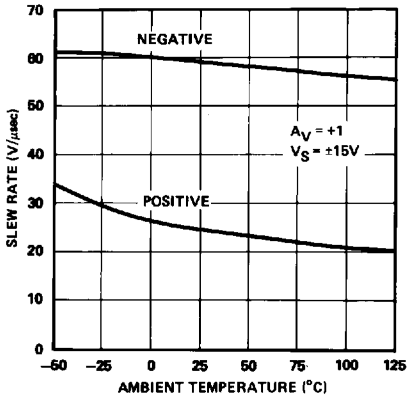
OPEN-LOOP GAIN vs FREQUENCY



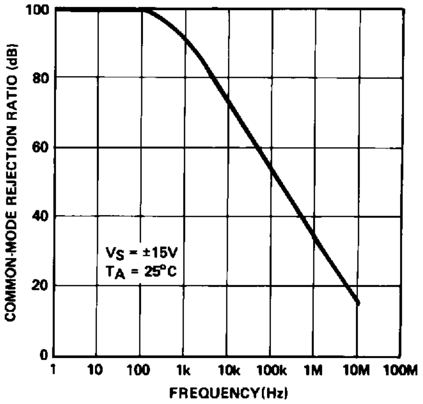
MAXIMUM OUTPUT SWING vs FREQUENCY



SLEW RATE vs TEMPERATURE

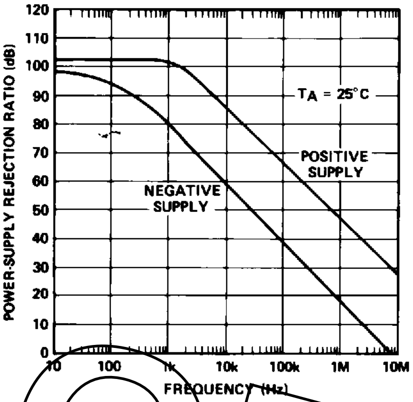


COMMON-MODE REJECTION RATIO vs FREQUENCY

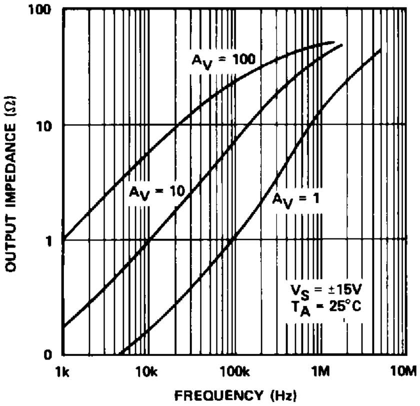


TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

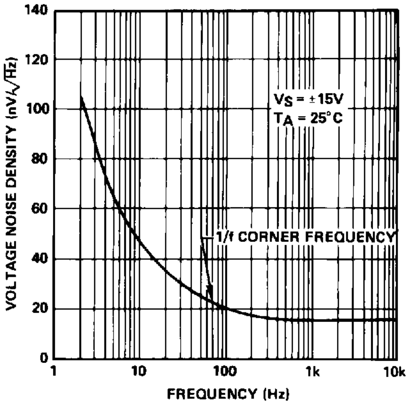
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

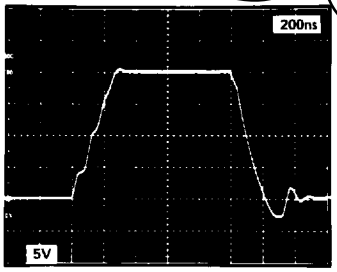


VOLTAGE NOISE DENSITY vs FREQUENCY

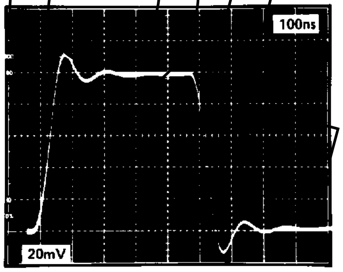


TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)

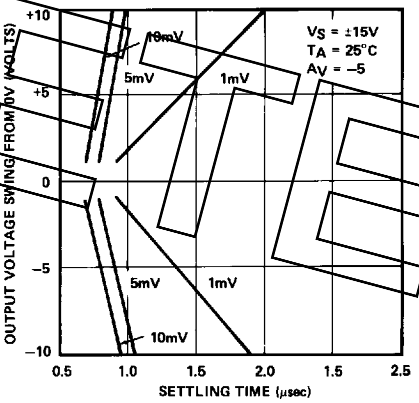
LARGE-SIGNAL TRANSIENT RESPONSE



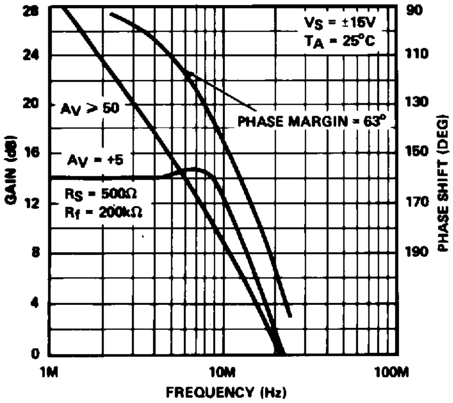
SMALL-SIGNAL TRANSIENT RESPONSE



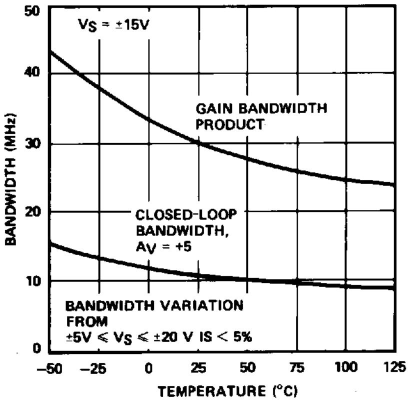
SETTLING TIME



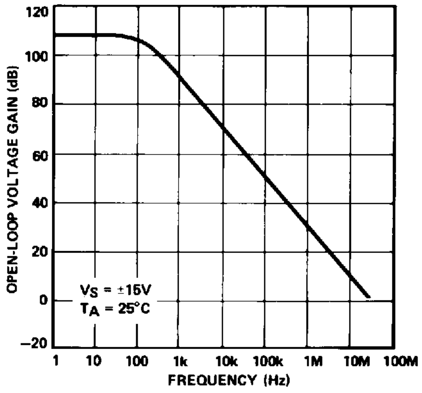
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



BANDWIDTH vs TEMPERATURE

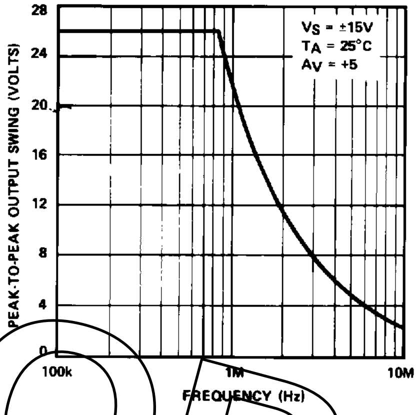


OPEN-LOOP FREQUENCY RESPONSE

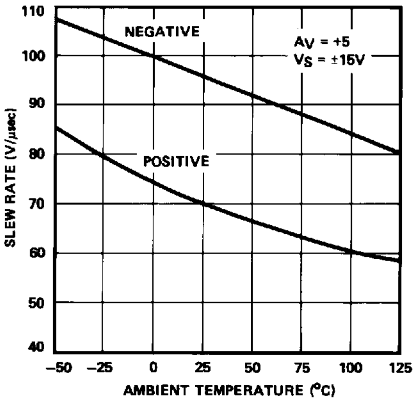


TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)

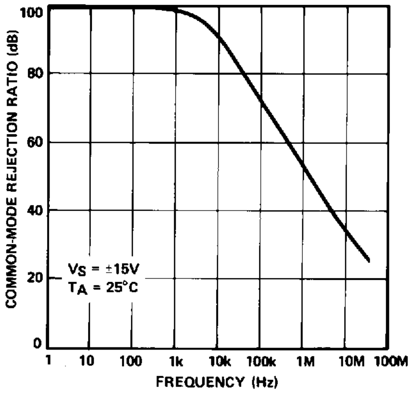
MAXIMUM OUTPUT SWING vs FREQUENCY



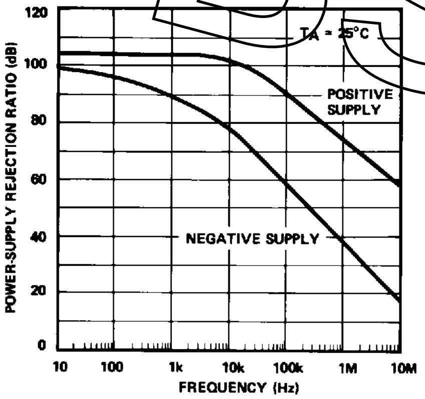
SLEW RATE vs TEMPERATURE



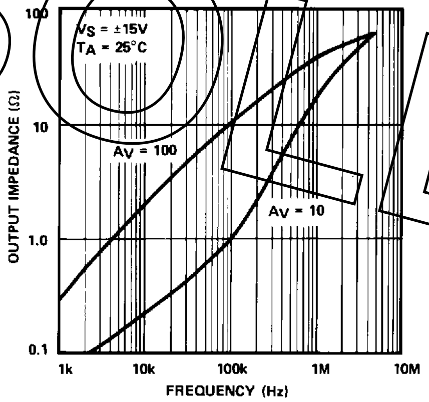
COMMON-MODE REJECTION RATIO vs FREQUENCY



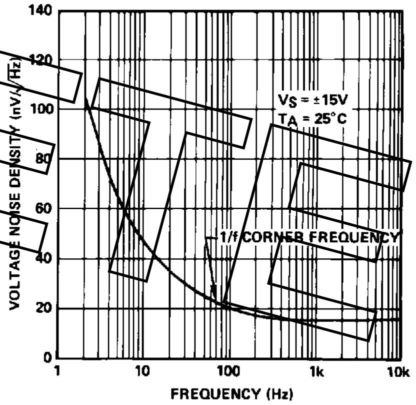
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

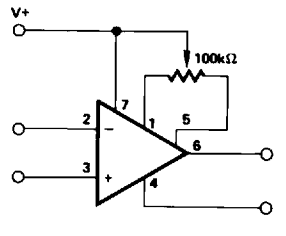


VOLTAGE NOISE vs FREQUENCY



BASIC CONNECTIONS

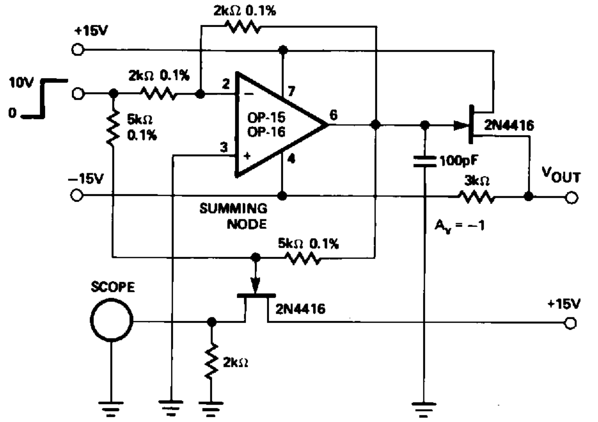
INPUT OFFSET VOLTAGE NULLING



V+
100kΩ
7
1
5
2
–
6
3
+
4

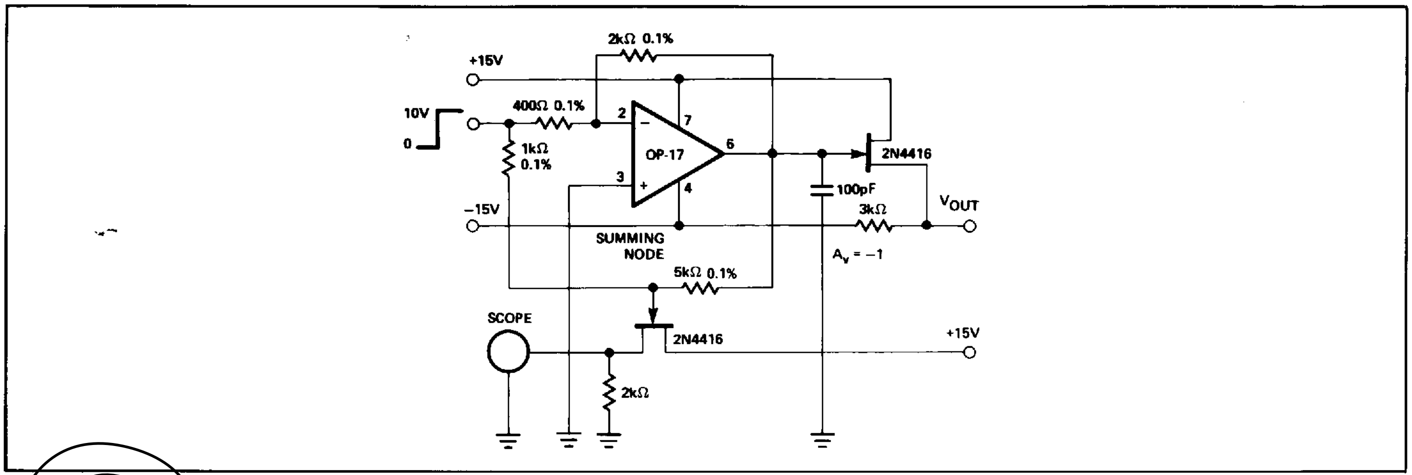
NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

SETTLING-TIME TEST CIRCUIT — OP-15/OP-16



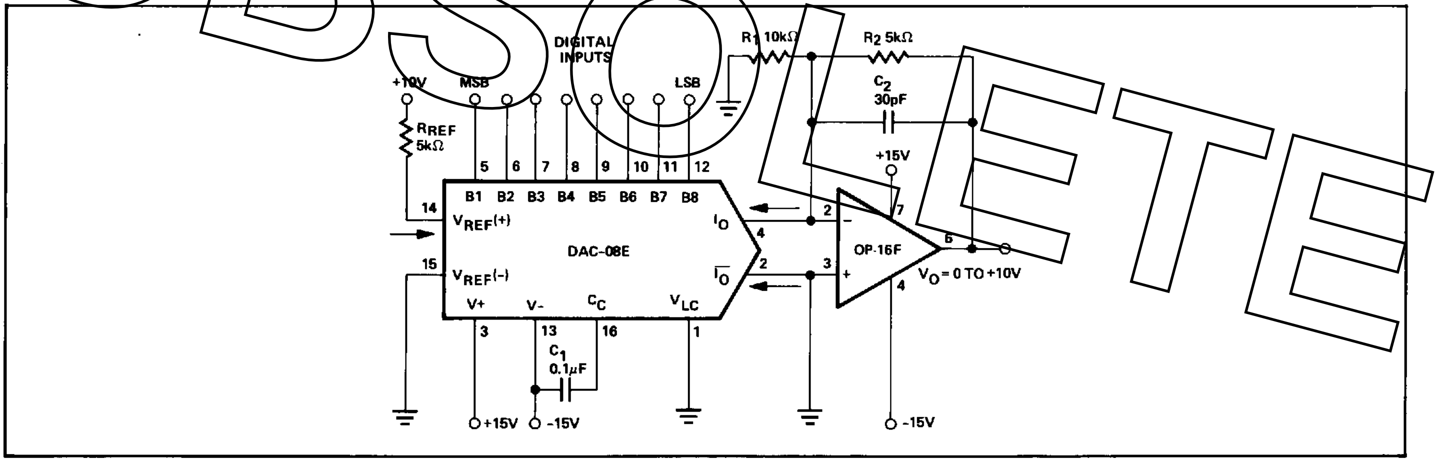
2kΩ 0.1%
+15V
10V
0
2kΩ 0.1%
2
–
7
5kΩ 0.1%
OP-15
OP-16
6
2N4416
3
+
4
100pF
–15V
3kΩ
VOUT
SUMMING NODE
Av = –1
5kΩ 0.1%
SCOPE
2N4416
+15V
2kΩ

SETTLING-TIME TEST CIRCUIT — OP-17


2kΩ 0.1%
+15V
10V
0
400Ω 0.1%
1kΩ
0.1%
2
7
OP-17
6
3
4
2N4416
100pF
3kΩ
VOUT
–15V
SUMMING
NODE
Av = –1
5kΩ 0.1%
SCOPE
2N4416
+15V
2kΩ

TYPICAL APPLICATIONS

CURRENT-TO-VOLTAGE AMPLIFIER OUTPUT


DIGITAL
INPUTS
+10V
MSB
LSB
RREF
5kΩ
5
6
7
8
9
10
11
12
B1 B2 B3 B4 B5 B6 B7 B8
14
VREF(+)
15
VREF(–)
DAC-08E
IO
ĪO
V+
V-
CC
VLC
3
13
16
1
C1
0.1µF
+15V
-15V
R1 10kΩ
R2 5kΩ
C2
30pF
+15V
4
2
2
7
OP-16F
6
3
4
VO = 0 TO +10V
-15V

APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time-constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback pole time constant.