RS9113 Module Family

Datasheet

Version 3.5

January 2018

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Overview:

The RS9113 module family is based on Redpine Signals' RS9113 ultra-low-power Convergence SoC. These modules offer dual-band 1x1 802.11n, dual-mode Bluetooth 4.0 and ZigBee® 802.15.4 in a single device. They are high performance, long range and ultra-low power modules and include a proprietary multi-threaded MAC processor called ThreadArch®, digital and analog peripheral interfaces, baseband digital signal processor, calibration OTP memory, dual-band RF transceiver, dual-band high-power amplifiers, baluns, diplexers, diversity switch and Quad-SPI flash.

The modules are offered with two software architectures – hosted and embedded. The hosted variant (n-Link®) realizes a host-based architecture where the necessary MAC and PHY layers are implemented in the device to support high-performance, long range WLAN, Bluetooth and ZigBee applications in a 32-bit host processor over SDIO or USB interfaces. The embedded variants (WiSeConnect® and Connect-io-n®) realize WLAN, Bluetooth and ZigBee protocols along with Wi-Fi Direct™([1]), WPA/WPA2-PSK, WPA/WPA2-Enterprise (EAP-TLS, EAP-FAST, EAP-TTLS, EAP-PEAP, EAP-LEAP)(1) and a feature-rich networking stack thus providing a fully-integrated solution for embedded low-end wireless applications. These modules can be connected to 8/16/32-bit host processors through SPI,UART, USB and USB-CDC interfaces.
The modules are available in two hardware footprints. One footprint type comes with an integrated antenna and an u.FL connector and the other footprint comes without an integrated antenna.

Applications:

- Smartphones, Tablets and e-Readers
- VoWi-Fi phones
- Smart meters and in-home displays
- Industrial automation and telemetry
- Medical devices
- Industrial monitoring and control
- Home and building automation
- Wireless Headset

Module Features:

WLAN:

- Compliant to single-spatial stream IEEE 802.11 a/b/g/n with dual band (2.4 and 5 GHz) support.
- Support for 20MHz and 40MHz (n-Link™ only) channel bandwidths.
- Transmit power up to +17dBm with integrated PA.
- Receive sensitivity of -97dBm.

Bluetooth:

- Compliant to dual-mode Bluetooth 4.0
- Transmit power up to 15dBm (class-1) with integrated PA.
- Receive sensitivity of -94 dBm.

ZigBee:

- Compliant to IEEE 802.15.4
- Transmit power up to 15 dBm with integrated PA.
- Receive sensitivity of -102 dBm.
- ZigBee Pro stack embedded.

n-Link®:

- Seamless integration with 32-bit processors over SDIO and USB.
- Host Drivers for Linux, Android and Windows[2]

WiSeConnect® and Connect-io-n®:

- WLAN, Bluetooth and ZigBee stacks embedded in the device.
- Supports Wi-Fi Direct™(1), Access point mode, WPA/WPA2-PSK, WPA/WPA2-Enterprise (EAP-TLS, EAP-FAST, EAP-TTLS, EAP-PEAP, EAP-LEAP)1
- Bluetooth profiles embedded.[3]
- ZigBee Pro stack embedded.
- TCP/IP stack (IPv4/IPv6), HTTP/HTTPS, DHCP, ICMP, SSL 3.0/TLS1.2, Websockets, IGMP, FTP Client, SNTP, DNS, mDNS, DNS-SD, SNMP[4] embedded in the device.
- SPI, UART, USB, USB-CDC host interfaces.

General:

- FCC, IC, ETSI/CE, TELEC Certified
- U.FL connector for external antenna connection.
- Dual external antenna for antenna diversity (n-Link™ only.
- Wireless firmware upgrade (for WiSeConnect™ and Connect-io-n™ only)
- Options for single supply of 3.0 to 3.6 V operation or multiple supplies for power saving[5].

[1]This feature is specific to WiSeConnect® Modules and not available in Connect-io-n® Modules.
[2]Drivers for Linux and Android available now. Contact Redpine Signals Sales (sales@redpinesignals.com) for availability of drivers Windows.
[3]Refer to the Features section for list of profiles supported.
[4]mDNS and DNS-SD supported in future software releases.
[5]USB Interface needs VBUS level of 5V for detection and enumeration.

- Operating temperature range: -40ºC to +85ºC

About this Document

This document describes the RS9113 module family specifications. The document covers the modules' hardware and software features, package descriptions, pin descriptions, interface specifications, electrical characteristics, performance specifications, reliability and certification information and ordering information.

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1 Overview

The RS9113 n-Link®, WiSeConnect® and Connect-io-n® modules are M2M Combo modules based on Redpine Signals' RS9113 ultra-low-power Convergence SoC.

They differ in terms of the features embedded in the module's firmware and their performance. The n-Link® modules are high-performance modules which realize a zero-host architecture for the data path. The necessary MAC and PHY layers are implemented in the device to support WLAN, Bluetooth and ZigBee applications and they interface with 32-bit host processors over SDIO or USB interfaces. The WiSeConnect® and Connect-io-n® modules offer WLAN, ZigBee and Bluetooth protocols along with Wi-Fi Direct™([6]), WPA/WPA2-PSK,WPA/WPA2-Enterprise (EAP-TLS, EAP-FAST, EAP-TTLS, EAP-PEAP, EAP-LEAP) (6) and a feature-rich networking stack embedded in the device, thus providing a fully-integrated solution for embedded wireless applications. These modules can be interfaced to 8/16/32-bit host processors through SPI, UART, USB and USB-CDC interfaces.

All three modules are offered with and without an integrated antenna. The module with the integrated antenna also offers a u.FL connector for connecting an external antenna with an option to select either one of them.

1.1 Block Diagram

The following figures are the block diagrams for the modules with and without the integrated antenna.

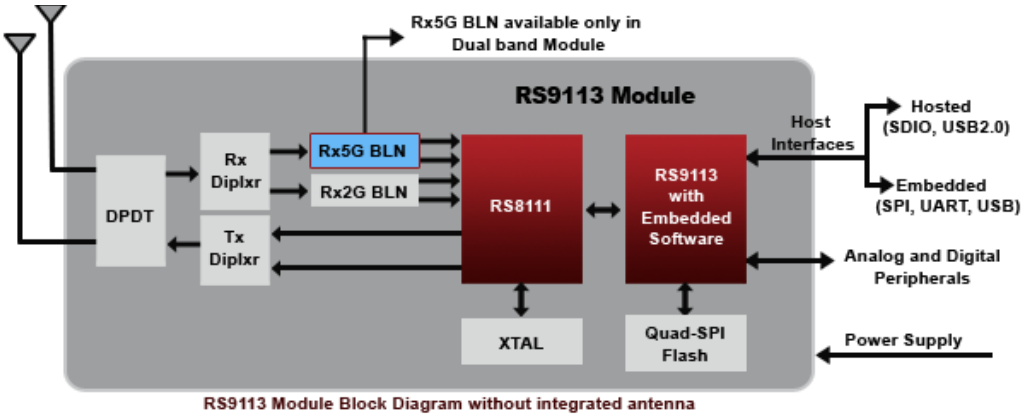

Figure 1: Block Diagram of RS9113 Module without Integrated Antenna

[6]This feature is specific to WiSeConnect® Modules.

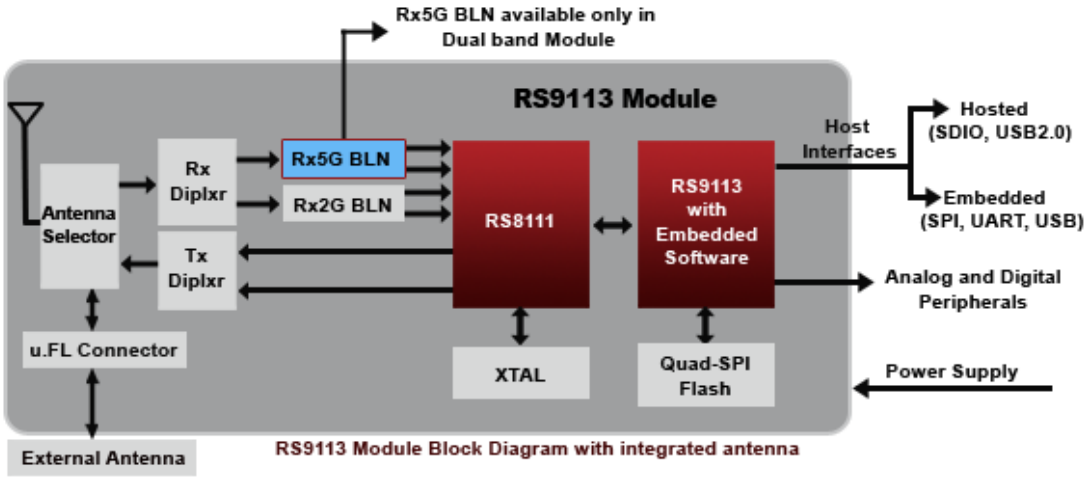

Figure 2: Block Diagram of RS9113 Module with Integrated Antenna

1.2 Product Naming and Variants

The figure below shows the naming convention of the RS9113 Family Modules.

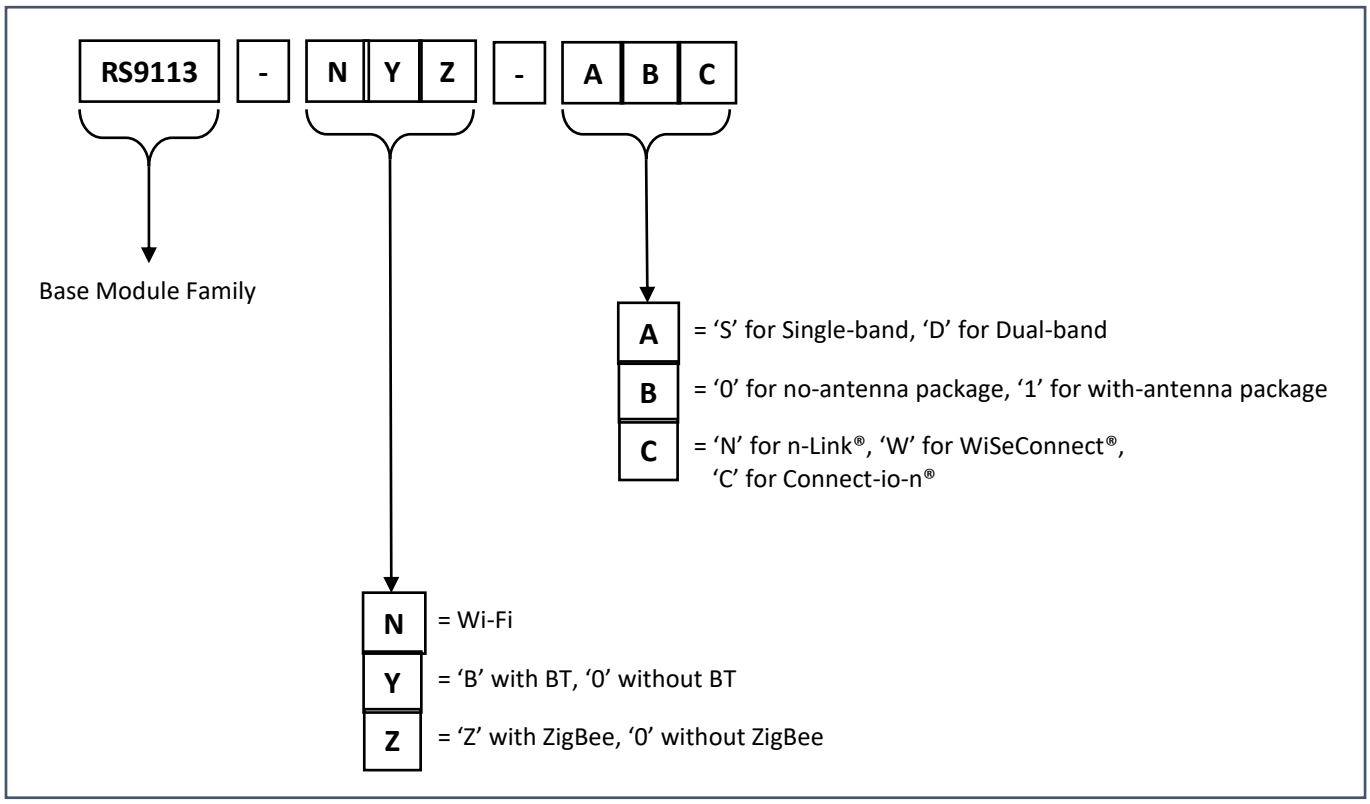

Figure 3: RS9113 Modules' Naming Convention

NOTE:

1) The possible combinations of ‘XYZ’ are ‘N00’, ‘NB0’, ‘N0Z’ and ‘NBZ’.
2) The modules and the accompanying software/firmware support a maximum of two wireless protocols simultaneously.

For the full list of available module variants, please see the section on Ordering Information.

2 Features

The table below lists the features supported by the n-Link®, WiSeConnect® and Connect-io-n® modules.

S.No.	Feature	n-Link®	WiSeConnect®	Connect-io-n®
1.	Wireless Protocols	IEEE 802.11a, 802.11b, 802.11g, 802.11n Bluetooth 4.0 (2.1+EDR, LE) ZigBee 802.15.4		
2.	Operational Modes Supported[7]	Wi-Fi Access Point with support for upto 32 clients	Wi-Fi Access Point with support for upto 8 clients and limited packet buffering	
		Wi-Fi Client		
		Wi-Fi Access Point + Client	NA	
		Wi-Fi Direct™		NA
		Wi-Fi Client + Bluetooth Classic (EDR v2.1) Wi-Fi Client + Bluetooth Low Energy Wi-Fi Client + ZigBee End Device	Wi-Fi Client + ZigBee End Device	Wi-Fi Client + Bluetooth Classic (EDR v2.1) Wi-Fi Client + Bluetooth Low Energy Wi-Fi Client + ZigBee End Device
		ZigBee Router[8] ZigBee Coordinator8		
3.	WLAN Bandwidth	20 and 40 MHz	20 MHz	
4.	WLAN Data Rates	802.11b: 1, 2, 5.5, 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n: MCS0 to MCS7 with and without Short GI		
5.	WLAN Operating Frequency Range	2412 MHz – 2484 MHz 4910 MHz – 5825 MHz		
6.	WLAN Modulation	OFDM with BPSK, QPSK, 16-QAM, and 64-QAM		

[7]For other co-existence modes not listed here, contact Redpine Signals Sales (sales@redpinesignals.com) for custom offerings.
[8]Supported in future software releases.

S.No.	Feature	n-Link®	WiSeConnect®	Connect-io-n®
		802.11b with CCK and DSSS		
7.	WLAN Transmit Power	17 dBm		
8.	WLAN Receive Sensitivity	-97 dBm		
9.	Bluetooth Data Rates	1, 2, 3 Mbps		
10.	Bluetooth Operating Frequency Range	2402 MHz - 2480 MHz		
11.	Bluetooth Channel Spacing	BR, EDR – 1 MHz LE – 2 MHz		
12.	Bluetooth Modulation	GFSK, DQPSK, 8DPSK		
13.	Bluetooth Transmit Power	15 dBm (Class-1)		
14.	Bluetooth Receive Sensitivity	-94 dBm		
15.	ZigBee Data Rate	250 kbps		
16.	ZigBee Operating Frequency Range	2405MHz - 2480 MHz		
17.	ZigBee Modulation	DSSS		
18.	ZigBee Transmit Power	15 dBm		
19.	ZigBee Receive Sensitivity	-102 dBm		
20.	Deep Sleep Current Consumption	< 10 µA in disconnected state < 30 µA in connected state		
21.	Host Interfaces	SDIO 2.0 USB 2.0/1.1	SPI UART USB 2.0/1.1 USB-CDC	
22.	SDIO Host Interface	Compatible with SDIO standard version 2.0 Maximum clock speed of 50MHz	NA	
23.	USB Host Interface	Supports 480 Mbps High Speed (HS) mode and 12 Mbps Full Speed (FS) modes.		
24.	SPI Host Interface	NA	Maximum clock speed of 80MHz	

S.No.	Feature	n-Link®	WiSeConnect®	Connect-io-n®
			Support for SPI Modes 0 (CPOL=0, CPHA=0) and 3 (CPOL=1, CPHA=1)	
25.	UART Host Interface	NA	Supported Baud Rates (bps): 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 Support for AT and Binary Commands for Configuration and Data Transfer Support for 8 bits encoding Support for 1stop bit Support for Auto Flow Control Support for Transparent Mode	
26.	Software Architecture	Architecture for Zero Host Load for Data path	Embedded Architecture which includes all network related features, including WLAN, Bluetooth, ZigBee stacks and a feature-rich TCP/IP stack embedded in the module. Option to bypass the TCP/IP stack and include only the Wireless protocol stacks.	
27.	Wireless Security Features	WPA/WPA2 Personal WPA/WPA2 Enterprise Security WPS (in the Host)	WPA/WPA2-Personal WPA/WPA2 Enterprise[9]: EAP-TLS EAP-FAST EAP-TTLS EAP-PEAP EAP-LEAP WPS (embedded in the device)	WPA/WPA2-Personal WPS (embedded in the device)
28.	Advanced Security Features[10]	PUF Based Security AES 128/256-bit		

[9]Supported only in Wi-Fi Client mode. For Enterprise Security methods not listed here, contact Redpine Signals Sales (sales@redpinesignals.com) for custom offerings.
[10]These features are not part of the standard firmware. Contact Redpine Signals Sales (sales@redpinesignals.com) for details.

S.No.	Feature	n-Link®	WiSeConnect®	Connect-io-n®
		RSA SHA, SHA256 ECDH		
29.	Application throughputs[11]	Upto 90 Mbps UDP Upto 70 Mbps TCP	With embedded TCP/IP Stack: Upto 25 Mbps UDP Upto 20 Mbps TCP With TCP/IP Stack in Host: Upto 40 Mbps UDP Upto 25 Mbps TCP	
30.	Operating Temperature Range	-40°C to +85°C		
31.	Supply Voltages and Options[12]	Option 1: Single 3.0 to 3.6V Supply Option 2[13]: A 3.0 to 3.6V Supply, a 1.8 to 3.6V Supply and a 1.9 to 3.6V Supply		
32.	WLAN Features	Dynamic selection of data rate depending on the channel statistics. Hardware accelerators for WEP 64/128-bit, TKIP, AES and WPS Support for WMM Support for AMPDU Aggregation/De-aggregation and AMSDU De-aggregation Support for IEEE 802.11d/e/I, 802.11j[14], 802.11w/k/v/r/h[14]		
33.	TCP/IP Features	NA	TCP/IP Stack with IPv4, IPv6 HTTP Server/Client Static and Dynamic Webpages with JSON Objects (for HTML Server) DHCP Server/Client for IPv4 and IPv6	

[11]The throughputs mentioned here have been recorded in an ideal environment on an x86 platform over USB. Throughputs observed in other environments might differ based on the host interface speeds (e.g., SPI/SDIO clock frequency, UART Baud Rate, etc.), host processor capabilities (CPU frequency, RAM, etc.), wireless medium, physical obstacles, distance, etc.
[12]USB Interface needs VBUS level of 5V for detection and enumeration.
[13]This option results in lower power consumption overall. Refer to the Module Integration Guide for details on the circuit.
[14]Except 802.11h, all other features to be supported in future software releases. 802.11h is supported in n-Link™ only. Contact Redpine Signals Sales (sales@redpinesignals.com) for DFS certification for different regulatory domains.

S.No.	Feature	n-Link®	WiSeConnect®	Connect-io-n®
			HTTPS Server/Client ICMP SSL 3.0/TLS 1.2 Websockets DNS Client IGMP FTP Client SNTP mDNS Client[15] DNS-SD Client[15] SNMP[15]	
34.	Bluetooth Features	Supports Classic mode piconet with seven active slaves[16]. Supports Low Energy mode with upto eight active slaves[17]. Supports scatternet with two slave roles or one master role and one slave role while being visible[18]. Proprietary Mode to support 15 active slaves by using the "reserved" bit[18]. Bluetooth security features: Authentication, Pairing and Encryption. Supports low power connection states such as hold and sniff modes with selectable sniff intervals[19]. Adaptive Frequency Hopping (AFH), Interlaced scanning, Quality of Service, Channel Quality Driven Data Rate[18]. Channel assessment algorithm provides fast and accurate determination of occupied channels for use in adaptive frequency hopping mode[18]. Proprietary FEC for DQPSK and 8-PSK modes. Provides finer granularity of range vs. throughput control.		
35.	Bluetooth Profiles/Protocols[20]	All profiles are to	GAP	

[15]mDNS, DNS-SD and SNMP supported in future software releases.
[16]Current software releases support one slave.
[17]WiSeConnect™ release v1.6.1 onwards supports upto 8 active slaves and n-Link™ release v1.2.0 onwards supports upto 3 active slaves. Support for upto eight slaves for n-Link™ to be added in future releases.
[18]Supported in future software releases. Two slave roles can be supported only when LE mode is not enabled.
[19]Hold supported in future software releases.

S.No.	Feature	n-Link®	WiSeConnect®	Connect-io-n®
		be implemented in the Host.	GATT SPP SDP SMP L2CAP RFCOMM iAP1	
36.	ZigBee Features	**MAC:** Supported modes: ZigBee Coordinator, Router[21], End device. PHY features: Beacon[18], Non-Beacon, CCM Security, Promiscuous mode. Power saving using End Device Sleep, network periodic sleep. Supports CCM* Security levels 1-7. Supports Active scan, channel selection, Association and Disassociation, Orphan scanning, and coordinator realignment. **Network Layer:** Network Discovery Energy Detection Scan Network Formation Permit Joining Network Join Network Rejoin Stochastic Addressing Network Leave Network Reset Routing (Symmetric) Address Conflict PANID Conflict Network Status Updates Link Status Commands Data Transmission (Unicast and Broadcast)		

[20]Profiles not listed here can be offered as part of custom firmware. Contact Redpine Signals Sales (sales@redpinesignals.com) for details.
[21]Coordinator and Router modes supported in future software releases.

S.No.	Feature	n-Link®	WiSeConnect®	Connect-io-n®
		NIB Management Many-to-one and source routing Multicast relaying and route discovery **APS Layer:** APSDE Data primitives APSME Group Services APSME Binding Services APSME Fragmentation Service Reliable Transport Duplicate Rejection APS Layer Security **ZDO/ZDP Layer:** Device Discovery Service Discovery Security Manager Node Manager Network Manager Binding Manager Group Manager Startup Attributes Set		
37.	Power Save Modes[22]	Dynamic Clock Gating Low Power (LP) Mode – Modem and RF Transceiver Powered off. Host Interface is active. Supported with all host interfaces. Ultra-Low Power (ULP) Mode – Most of the module powered off except for a small portion running a timer. Host interface is inactive. Entry and exit of sleep mode can be through packet or GPIO based handshake. Supported only in SPI, UART (WiSeConnect® and Connect-io-n®) and SDIO (n-Link®) modes.		
38.	Miscellaneous Features	Automatic Firmware Checksum validation and	Wireless Firmware Upgrade Wireless Configuration	

[22]Refer to Technical Reference Manual of n-Link® Modules and Programmer Reference Manual/API User Guide of WiSeConnect® and Connect-io-n® Modules for more details on how to use these modes. Refer to the GPIO section of the Pin Description table to understand the signal requirements for these modes.

S.No.	Feature	n-Link®	WiSeConnect®	Connect-io-n®
		upgrade at power-up		

Table 1: RS9113 Module Family Features

3 Package Description

The RS9113 Modules are offered in two package variants – one with an integrated antenna (and U.FL connector) and the other without an antenna.

3.1 Package Description of Module without Antenna (Package # P6)

3.1.1 Mechanical Characteristics

Parameter	Value (L X W X H)	Units
Module Dimensions	14 x 15 x 2.1	mm
Tolerance	±0.2	mm

Table 2: Mechanical Dimensions of Module without Antenna

3.1.2 Package Dimensions

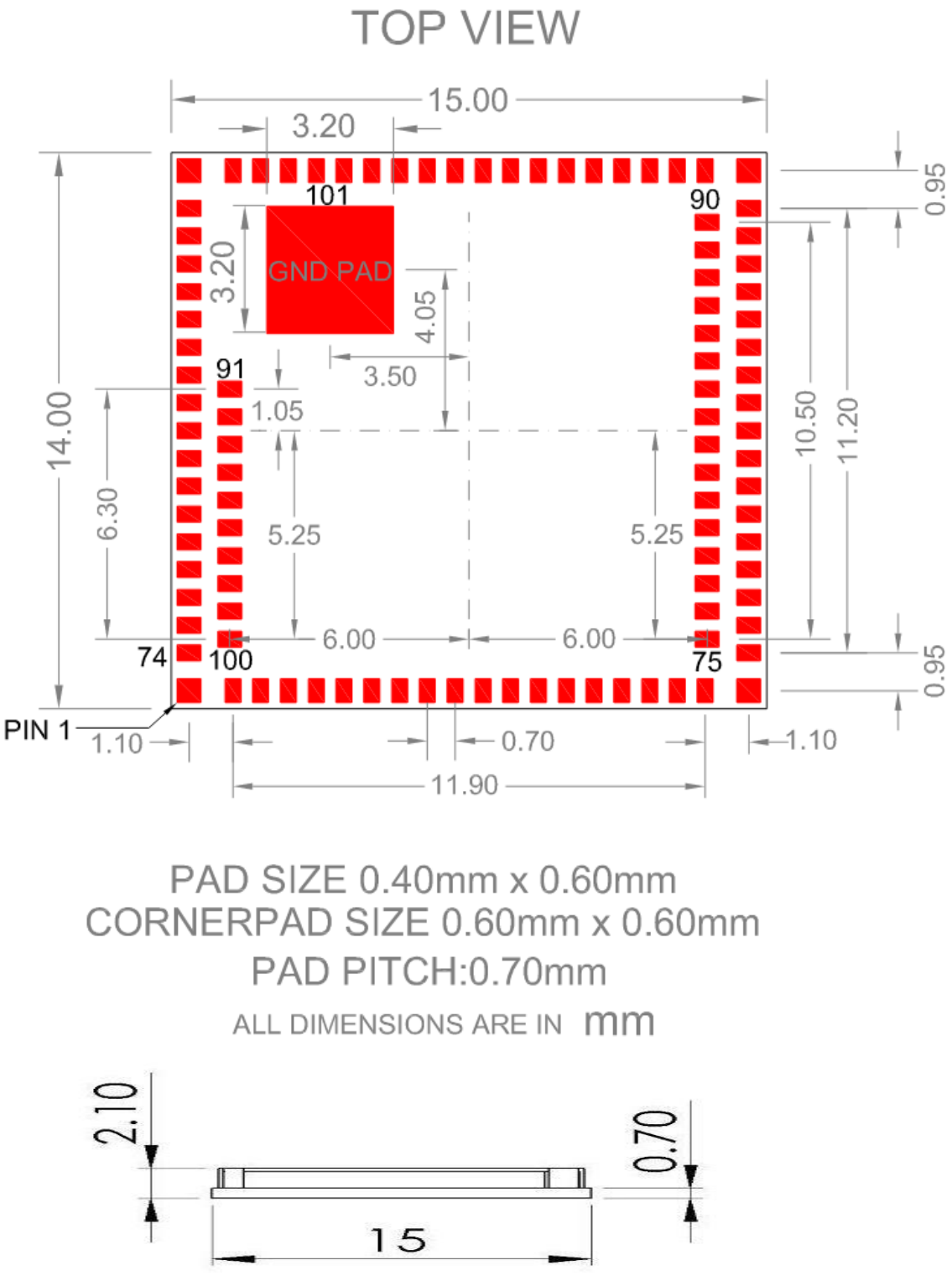

Figure 4: Package Dimensions of Module without Antenna

3.1.3 PCB Landing Pattern

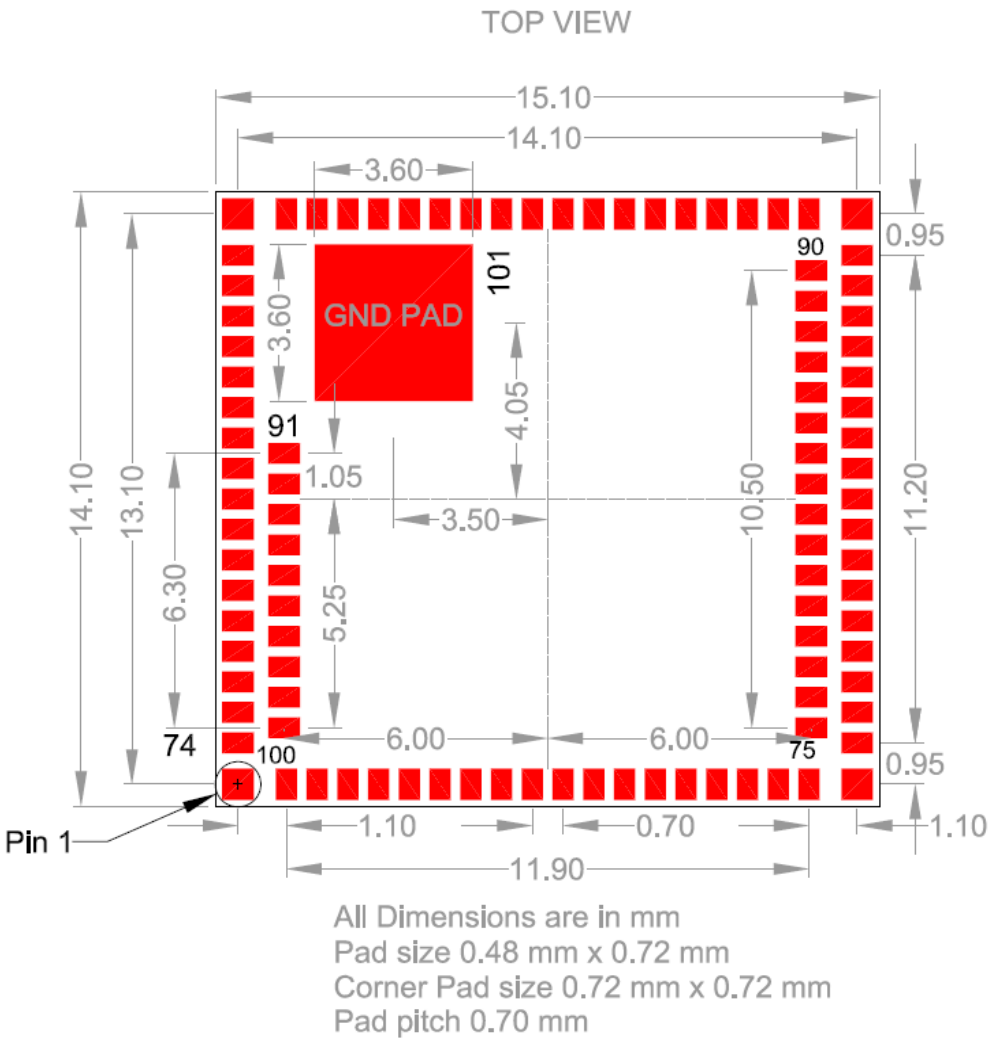

Figure 5: PCB Landing Pattern of Module without Antenna

3.2 Package Description of Module with Antenna (Package # P7)

3.2.1 Mechanical Characteristics

Parameter	Value (L X W X H)	Units
Module Dimensions	27 x 16 x 3.1	mm
Tolerance	±0.2	mm

Table 3: Mechanical Dimensions of Module with Antenna

3.2.2 Package Dimensions

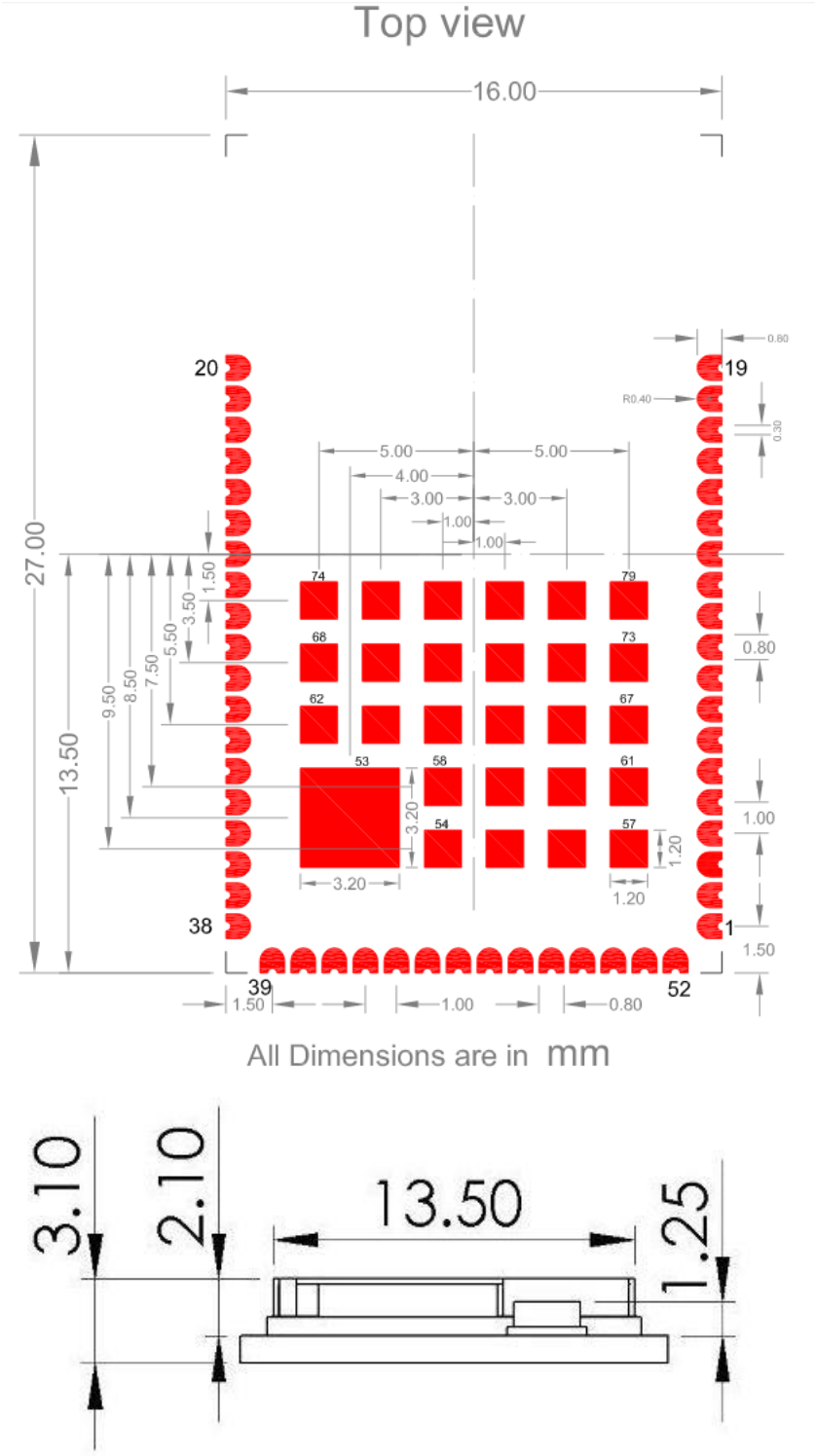

Figure 6: Package Dimensions of Module with Antenna

3.2.3 PCB Landing Pattern

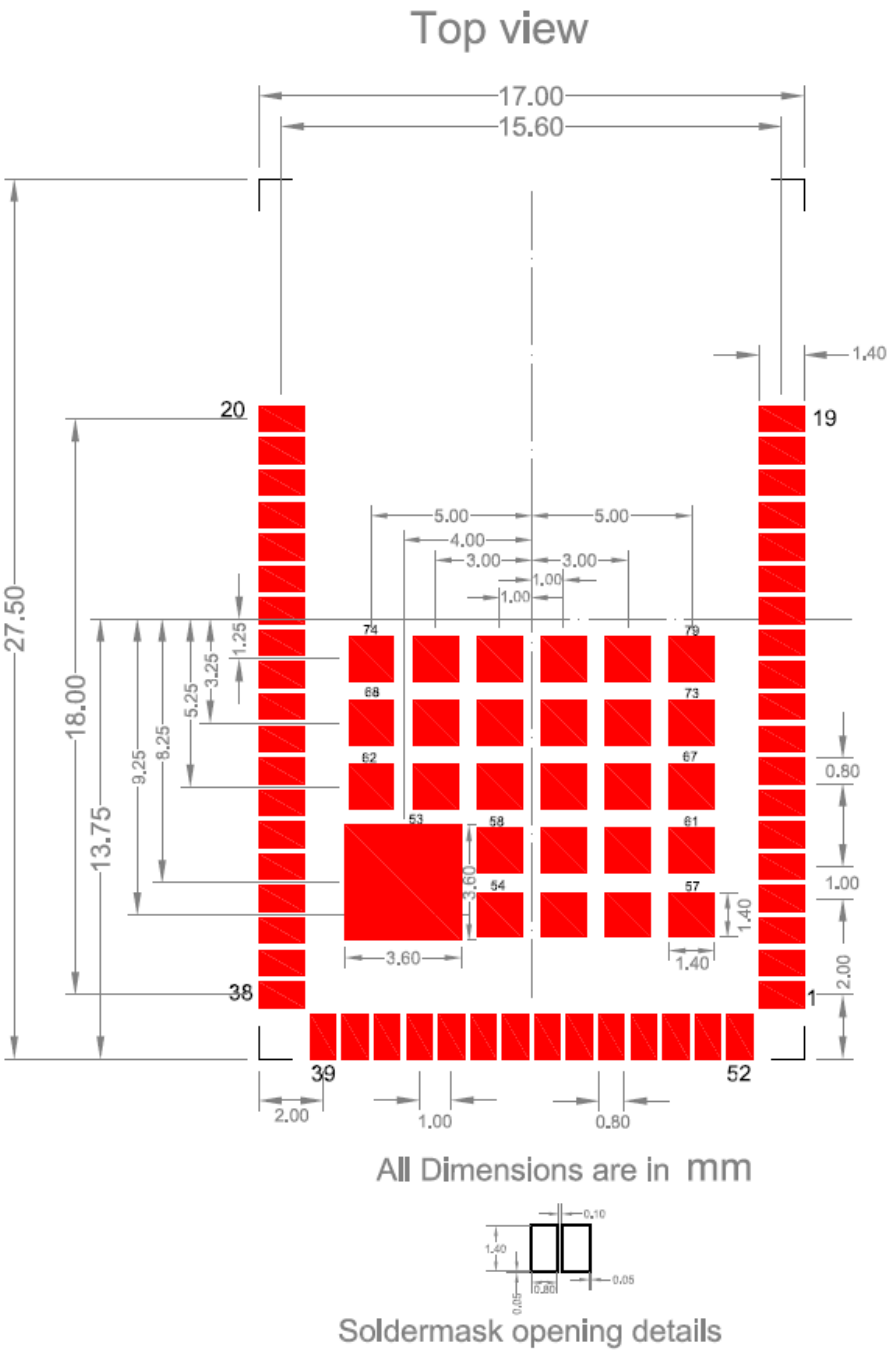

Figure 7: PCB Landing Pattern of Module with Antenna

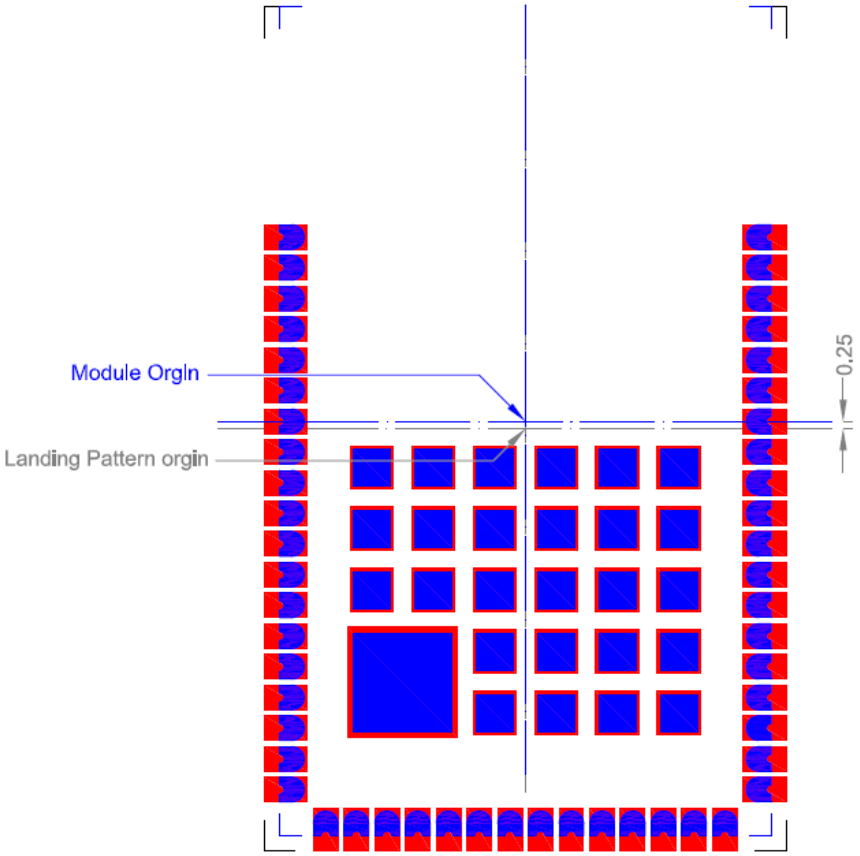

Figure 8: Mounting View of Module with Antenna

3.1 Recommended Reflow Profile

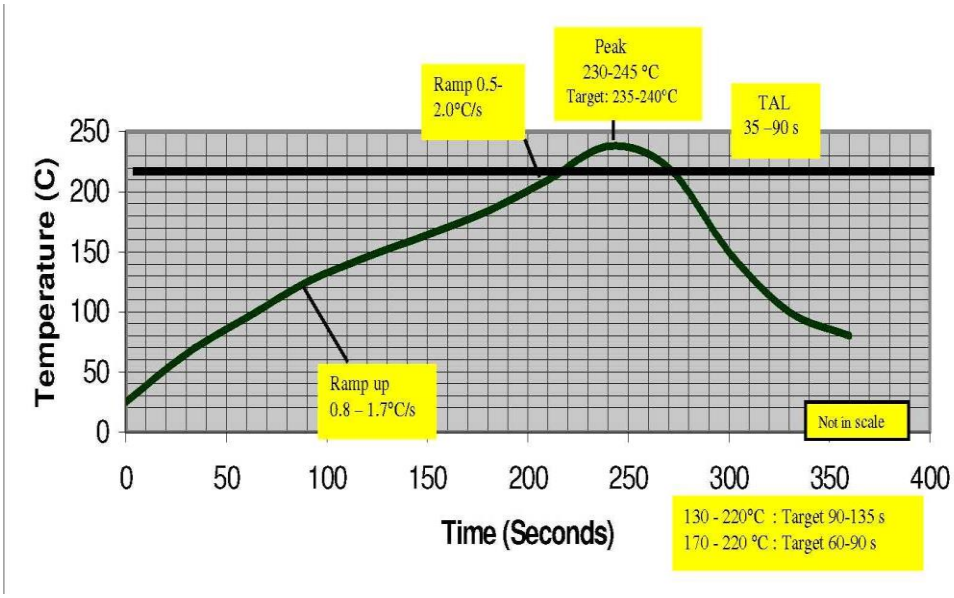

Figure 9: Reflow Diagram

Note: The profile shown is based on SAC 305 solder (3% silver, 0.5% copper). We recommend the ALPHA OM-338 lead-free solder paste. This profile is provided mainly for guidance. The total dwell time depends on the thermal mass of the assembled board and the sensitivity of the components on it.The recommended belt speed is 50-60 Cm/Min. A finished module can go through two more reflow processes

3.2 Baking Instructions

The RS9113 module packages are moisture sensitive and devices must be handled appropriately. After the devices are removed from their vacuum-sealed packs, they should be taken through reflow for board assembly within 168 hours at room conditions, or stored at under 10% relative humidity. If these conditions are not met, the devices must be baked before reflow. The recommended baking time is nine hours at 125°C.

4 Pinout and Pin Description

4.1 Pinout of Module without Antenna

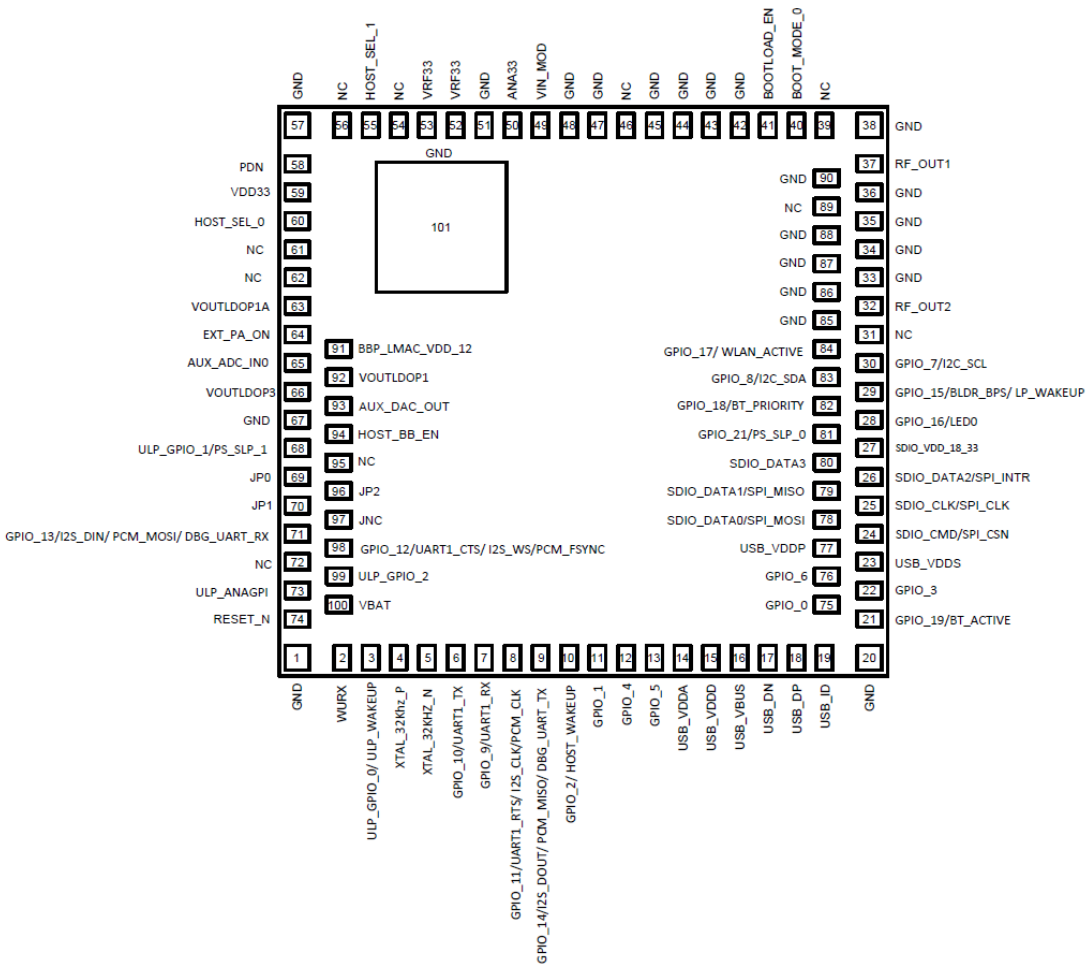

Figure 10: Pinout Diagram of Module without Antenna

4.2 Pinout of Module with Integrated Antenna

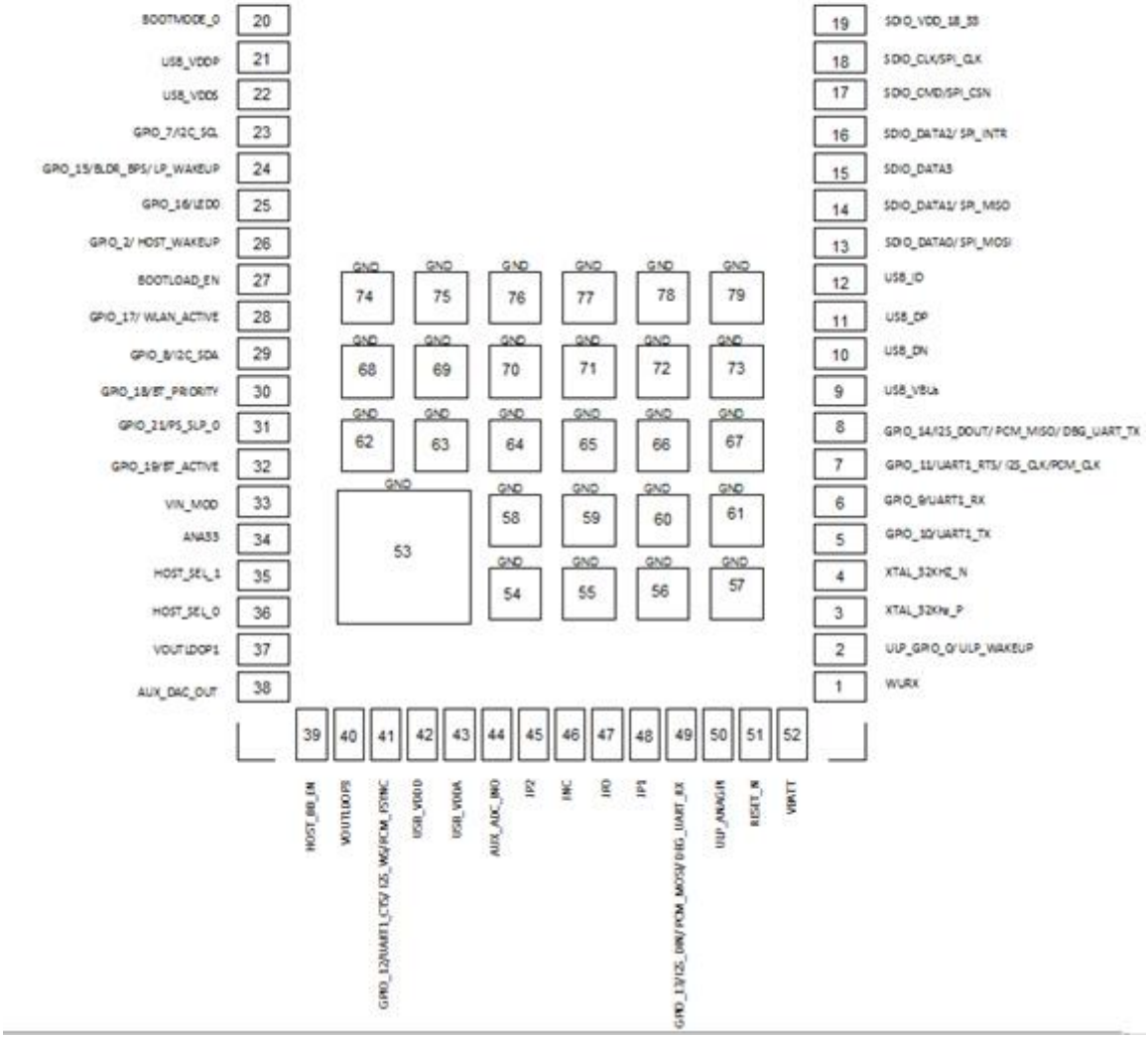

Figure 11: Pinout Diagram of Module with Antenna

4.3 Pin Description

This section describes the pins of the two packages of the RS9113 Module family. The information contained here should be used along with the information in the Module Integration Guide.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
Control and RF Interface					
1.	RESET_N	74	51	Input	Active-low asynchronous reset signal. The minimum reset assertion time is 20 ms.
2.	RF_OUT_2	32	---	RF In/RF Out	Default Antenna port. Connect to Antenna with a 50 Ω impedance. Refer to Module Integration Guide for details.
3.	RF_OUT_1	37	---	RF In/RF Out	Used in the case of Antenna Diversity[23]. If used, connect to Antenna with a 50 Ω impedance and follow same guidelines as RF_OUT_2 from Module Integration Guide. If unused, leave unconnected.
Power and Ground Interface[24]					
4.	VIN_MOD	49	33	Input	3.3V Digital Power Supply
5.	ANA33	50	34	Input	1.9V to 3.6V Analog Power Supply
6.	SDIO_VDD_18_33	27	19	Input	3.3V Digital Power Supply
7.	VBATT	100	52	Input	1.8V to 3.6V Digital Power Supply.
8.	VRF33	52, 53	---	Input	3.3V Analog Supply for the RF Transceiver.
9.	VDD33	59	---	Input	3.3V Digital Supply for the RF Transceiver.
10.	VOUTLDOP1	92	37	Output	USB Mode: Connect to USB_VDDD. Other Modes: Leave unconnected.
11.	VOUTLDOP3	66	40	Output	USB Mode: Connect to USB_VDDP. Other Modes: Leave unconnected.
12.	VOUTLDOP1A	63	---	Output	Connect to BBP_LMAC_VDD_12 through a filter. Refer to the Module Integration Guide for more details.
13.	BBP_LMAC_VDD_12	91	---	Input	Connect to the VOUTLDOP1A pin through a filter. Refer to the Module Integration Guide for more details.

[23]Supported in future software releases.
[24]Refer to the Module Integration Guide for recommendations on different supplies.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
14.	USB_VDDA	14	43	Input	USB Mode: 3.3V Analog Supply. Other Modes: Connect to Ground.
15.	USB_VDDS	23	22	Input	USB Mode: 3.3V Digital Supply. Other Modes: Connect to Ground.
16.	USB_VDDP	77	21	Input	USB Mode: Connect to VOUTLDOP3. Other Modes: Connect to Ground.
17.	USB_VDDD	15	42	Input	USB Mode: Connect to VOUTLDOP1. Other Modes: Connect to Ground.
18.	GND	1, 20, 33, 34, 35, 36, 38, 42, 43, 44, 45, 47, 48, 51, 57, 67, 85, 86, 87, 88, 90, 101	53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79	Ground	Common Ground
SDIO, Slave SPI and USB Interfaces					
19.	SDIO_CLK/SPI_CLK	25	18	Input	SDIO & SPI Modes: Interface clock from Host processor
				Input	Other modes: Reserved. Connect to Ground.
20.	SDIO_CMD/SPI_CSN	24	17	Inout	SDIO Mode: SDIO Interface Command Signal
				Input	SPI Mode: Active-low SPI Chip Select Signal
				Input	Other Modes: Reserved. Connect to Ground.
21.	SDIO_DATA0/SPI_MOSI	78	13	Inout	SDIO Mode: SDIO Interface Data0 Signal
				Input	SPI Mode: SPI Master-Out-Slave-In Signal
				Output	Other Modes: Reserved. Leave unconnected.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
22.	SDIO_DATA1/SPI_MISO	79	14	Inout	SDIO Mode: SDIO Interface DATA1 Signal
				Output	SPI Mode: SPI Master-In-Slave-Out Signal
				Input	Other Modes: Reserved. Connect to Ground.
23.	SDIO_DATA2/SPI_INTR	26	16	Inout	SDIO Mode: SDIO Interface DATA2 Signal
				Output	SPI Mode: Interrupt Signal to the Host. Active-high level, Active-low level and Open Drain modes are supported. In ULP mode, a pull-up or pull-down resistor of 100 kΩ might be required depending on whether the signal is configured as Active-low or Active-high. The pull-up/pull-down resistor can be avoided if the Host can mask this interrupt before the module enters ULP Sleep mode and unmask it after it exits ULP Sleep mode.
				Input	Other modes: Reserved. Connect to Ground.
24.	SDIO_DATA3	80	15	Inout	SDIO Mode: SDIO Interface DATA3 Signal
				Input	Other Modes: Reserved. Connect to Ground.
25.	USB_VBUS	16	9	Input	USB Mode: 5V VBUS Signal from USB Connector.
				Input	Other Modes: Leave unconnected.
26.	USB_DN	17	10	Inout	Negative Data Channel from USB Connector.
				Inout	Other Modes: Leave unconnected.
27.	USB_DP	18	11	Inout	Positive Data Channel from USB Connector.
				Inout	Other Modes: Leave unconnected.
28.	USB_ID	19	12	Inout	ID signal from USB Connector.
				Inout	Other Modes: Leave unconnected.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
GPIO Interface[25]					
29.	GPIO_0	75	---	Inout	Reserved – connect a 100 kΩ pull-down resistor.
30.	GPIO_1	11	---	Inout	Reserved – connect a 100 kΩ pull-up resistor.
31.	GPIO_2/HOST_WAKE UP	10	26	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Host Wakeup Interrupt Mode: This pin is used by firmware to indicate a pending packet to the Host processor. It should be used only if the Host processor is not able to wake up from a sleep state using the host interface specific interrupt like SDIO_DATA2/SPI_INTR. A pull up or pull down has to be placed on this pin based on whether the pin is configured as active low or active high interrupt in the Host processor, respectively. This feature can be enabled and configured through API (for WiSeConnect®/Connect-io-n®) and driver settings (for n-Link®).
32.	GPIO_3	22	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
33.	GPIO_4	12	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
34.	GPIO_5	13	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off

[25]All unused GPIOs can be configured by the Host processor (through a software command) as outputs to reduce current consumption.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
					using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
35.	GPIO_6	76	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
36.	GPIO_7/I2C_SCL	30	23	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	I^2C Mode: I^2C interface clock signal – connect a 10 kΩ pull-up resistor on this signal as per the I^2C standard. This feature is supported only when the I^2S mode is enabled in the n-Link™ releases v1.5.0 onwards. In WiSeConnect™ this feature is supported for IAP communication from release 1.6.0 onwards.
37.	GPIO_8/I2C_SDA	83	29	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Inout	I^2C Mode: I^2C interface data signal – connect a 10 kΩ pull-up resistor on this signal as per the I^2C standard. This feature is supported only when the I^2S mode is enabled in the n-Link™ releases v1.5.0 onwards. In WiSeConnect™ this feature is supported for IAP communication from release 1.6.0 onwards.
38.	GPIO_9/UART1_RX	7	6	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 1 Serial Input. This pin is configured as UART pin if UART is selected as the Host Interface.
39.	GPIO_10/UART1_TX	6	5	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 1 Serial Output. This pin is configured as UART pin if UART is

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
					selected as the Host Interface.
40.	GPIO_11/UART1_RTS /I2S_CLK/PCM_CLK	8	7	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 1 Request To Send – connect a 100 kΩ pull-down resistor if the host is not controlling this signal at all times. This pin is configured as UART pin if UART is selected as the Host Interface.
				Input	I^2S Mode: I2S Clock signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
				Input	PCM Mode: PCM Clock signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
41.	GPIO_12/UART1_CTS /I2S_WS/PCM_FSYN C	98	41	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 1 Clear To Send – connect a 100 kΩ pull-down resistor if the host is not controlling this signal at all times. This pin is configured as UART pin if UART is selected as the Host Interface.
				Input	I^2S Mode: I2S WS signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
				Input	PCM Mode: PCM FSYNC signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
42.	GPIO_13/I2S_DIN/PC M_MOSI/DBG_UART _RX	71	49	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 2 (Debug) Serial Input.
				Input	I^2S Mode: I2S Data Input signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
				Input	PCM Mode: PCM Master-Out-Slave-In signal. Supported only in n-Link™ in Slave mode from release v1.5.0

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
					onwards.
43.	GPIO_14/I2S_DOUT/ PCM_MISO/DBG_UART_TX	9	8	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 2 (Debug) Serial Output.
				Output	I^2S Mode: I2S Data Output signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
				Output	PCM Mode: PCM Master-In-Slave-Out signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
44.	GPIO_15/BLDR_BPS/ LP_WAKEUP	29	24	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	BLDR_BPS/LP_WAKEUP – in this mode, the signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module should wakeup from its Low Power (LP) sleep mode. The BLDR_BPS functionality is valid only for WiSeConnect®/Connect-io-n® modules.
45.	GPIO_16/LED0	28	25	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	LED Mode: Control signal for an external LED.
46.	GPIO_17/WLAN_ACTIVE	84	28	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Bluetooth Coexistence Mode: Active-high signal to indicate to an external Bluetooth IC that WLAN transmission is active. Not supported in the current firmware.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
47.	GPIO_18/BT_PRIORITY	82	30	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	Bluetooth Coexistence Mode: Active-high signal used to indicate to the module that Bluetooth transmissions are higher priority. Not supported in the current firmware.
48.	GPIO_19/BT_ACTIVE	21	32	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	Bluetooth Coexistence Mode: Active-high signal used to indicate to the module that an external Bluetooth IC is transmitting. Not supported in the current firmware.
49.	GPIO_21/PS_SLP_0	81	31	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Power Save Mode: This signal is used to indicate to the Host processor when the module enters (logic low) and exits (logic high) the LP and ULP Sleep modes when the GPIO Handshake mode is enabled. For ULP mode, connect a 100 kΩ pull-down resistor. For ULP mode, the ULP_GPIO_1 signal, if available in the package, may be used instead of GPIO_21 for the same purpose but without the need for the pull-down resistor.
50.	ULP_GPIO_0/ULP_WAKEUP	3	2	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	Power Save Mode: Active-high input to indicate that the module should exit its Ultra low power sleep mode – connect a 100 kΩ pull-down resistor if the host is not controlling this signal at all times.
51.	ULP_GPIO_1/PS_SLP_1	68	---	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Power Save Mode: This signal is used to indicate to the Host processor when the module enters (logic low) and exits (logic high) the ULP Sleep mode. The GPIO_21 signal may be used for the

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
					same purpose in case the package does not have the ULP_GPIO_1 signal available – GPIO_21 will need a pull-down resistor.
52.	ULP_GPIO_2	99	---	Inout	Reserved – leave this pin unconnected.
53.	ULP_ANAGPI	73	50	Input	Reserved – leave this pin unconnected.
Host Selection Interface[26]					
54.	HOST_SEL_0	60	36	Inout	SDIO Mode: Leave unconnected. SPI Mode: Connect a 4.7 kΩ pull-down resistor. USB Mode: Leave unconnected. USB-CDC Mode: Leave unconnected. UART Mode: Connect a 4.7 kΩ pull-down resistor.
55.	HOST_SEL_1	55	35	Inout	SDIO Mode: Leave unconnected. SPI Mode: Leave unconnected. USB Mode: Connect a 4.7 kΩ pull-down resistor. USB-CDC Mode: Connect a 4.7 kΩ pull-down resistor. UART Mode: Connect a 4.7 kΩ pull-down resistor.
56.	BOOTMODE_0	40	20	Inout	SDIO Mode: Leave unconnected. SPI Mode: Leave unconnected. USB Mode: Connect a 4.7 kΩ pull-down resistor. USB-CDC Mode: Leave unconnected. UART Mode: Leave unconnected.
Miscellaneous Signals					
57.	HOST_BB_EN	94	39	Output	Control signal used to indicate the entry (logic low) and exit (logic high) of the module into ULP mode. May be

[26]These are bootstrap signals and should not be actively driven to logic high or logic low by an external source. They should either be left unconnected or pulled down with a 4.7 kΩ resistor as per their descriptions.

S.No	Pin Name	Pin # in P6	Pin # in P7	Direction	Description
					used to control an external Load Switch and/or DC-DC for switching off the 3.3V supplies (other than VBATT) and reduce current consumption in ULP Mode. Refer to the Module Integration Guide for more details.
58.	JP0	69	47	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
59.	JP1	70	48	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
60.	JP2	96	45	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
61.	JNC	97	46	Output	Reserved – leave this pin unconnected.
62.	AUX_DAC_OUT	93	38	Output	Reserved – leave unconnected.
63.	AUX_ADC_IN0	65	44	Input	Reserved – leave unconnected.
64.	BOOTLOAD_EN	41	27	Inout	Reserved – leave unconnected.
65.	XTAL_32KHZ_N	5	4	Input	Reserved – leave unconnected.
66.	XTAL_32Khz_P	4	3	Input	Reserved – leave unconnected.
67.	EXT_PA_ON	64	---	Output	Reserved – leave unconnected.
68.	WURX	2	1	Input	Reserved – leave unconnected.
69.	PDN	58	---	Input	Reserved – connect to 100kΩ pull-down resistor.
70.	NC	31, 39,46, 54, 56, 61, 62, 72, 89, 95	---	NC (No Connect)	Leave unconnected.

Table 4: Pin Descriptions

5 Specifications

5.1 Absolute Maximum Ratings

Absolute maximum ratings in the table given below are the values beyond which the device could be damaged. Functional operation at these conditions or beyond these conditions is not guaranteed.

Parameter	Symbol	Value	Units
Input digital supply voltages	VIN_MOD, SDIO_VDD_18_33	3.6	V
USB VBUS voltage	USB_VBUS	5.25	V
Input analog supply voltage	ANA33	3.6	V
Input analog voltage for USB	USB_VDDA	3.6	V
Input digital voltage for USB	USB_VDDS	3.6	V
Input analog supply voltage for RF	VRF33	3.6	V
Input digital supply voltage for RF	VDD33	3.6	V
Input digital supply voltage for ultra-low power deep sleep related sections	VBATT	3.6	V
RF Input Level	RF_OUT_1, RF_OUT_2	10	dBm
Storage temperature	T_{store}	-65 to 150	°C
Operating temperature range	T_{op}	-40 to 85	°C
Electrostatic discharge tolerance (HBM)	ESD_{HBM}	2000[27]	V
Electrostatic discharge tolerance (CDM)	ESD_{CDM}	500	V
Electrostatic discharge tolerance (MM)	ESD_{MM}	60	V
Maximum Current consumption in TX mode	I_{max}	500	mA

Table 5: Absolute Maximum Ratings

[27] ESD Tolerance for HBM is 2000V for all pins except WURX. For WURX the tolerance is 1500V

5.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Input digital supply voltages	VIN_MOD, SDIO_VDD_18_33	3.0	3.3	3.6	V
Input analog supply voltage	ANA33	1.9	3.3	3.6	V
Input analog voltage for USB	USB_VDDA	3.0	3.3	3.6	V
Input digital voltage for USB	USB_VDDS	3.0	3.3	3.6	V
Input analog supply voltage for RF	VRF33	3.0	3.3	3.6	V
Input digital supply voltage for RF	VDD33	3.0	3.3	3.6	V
Input digital supply voltage for ultra-low power deep sleep related sections	VBATT	1.8	3.3	3.6	V
Ambient Temperature	T_a	-40	25	85	°C

Table 6: Recommended Operating Conditions

5.3 Reliability Qualification

The modules have been stress-tested for High Temperature Operating Life as per the JEDEC standard JESD22-A108D. The following are the details of the tests.

Parameters	Values/Details
Ambient Temperature	110°C
Junction Temperature	125°C
Supply Voltage	3.6V
Operational mode	Regular Ping with no power save modes activated.
Stress Duration	1000 hours
Number of Modules Tested	3 lots of 80 modules each
Intervals at which modules were removed from Temperature chamber for testing	168, 360, 720 and 1000 hours
Duration of the Tests (duration for which modules were kept outside the chamber)	12 to 13 hours

Parameters	Values/Details
Testing performed at each interval	1) Receive Sensitivity in Channels 1 and 11 for 1 Mbps, 6 Mbps and 54 Mbps data rates 2) Transmit power level and EVM in Channels 1 and 11 for 1 Mbps, 6 Mbps and 54 Mbps data rates 3) Peak current consumption in Transmit and Receive modes
Number of failed modules	Zero

Table 7: HTOL Based Stress Testing

The stress testing as per the JEDEC JESD22-A108D standard enables us to predict the operating life of the modules from the acceleration factor calculated using the Arrhenius equation as per JEDEC JEP122G. The Arrhenius equation is as follows:

$$A_T = \lambda_{T1}/\lambda_{T2} = exp[(-E_{aa}/k)(1/T_1 - 1/T_2)]$$

where[28]

A_T = Acceleration Factor

E_{aa} = Apparent activation energy (eV). 0.75eV is a conservative industry standard

k = Boltzmann's constant (8.62×10^{-5} eV/K)

T_1 = Temperature at use, in Kelvin

T_2 = Temperature at stress, in Kelvin

Using the data from the HTOL Based Stress Testing and assuming a junction temperature of 55°C for a use case scenario, we can safely assume an operating life of >9 years. The junction temperature for the module's ICs is usually 15 to 20°C more than the ambient temperature.

5.4 DC Characteristics – Digital I/O Signals

Parameter	Min.	Typ.	Max.	Units
Input high voltage	2	-	3.6	V
Input low voltage	-0.3	-	0.8	V
Output low voltage	-	-	0.4	V
Output high voltage	2.4	-	-	V
Input leakage current (at 3.3V or 0V)	-	-	±10	µA
Tristate output leakage current (at 3.3V or 0V	-	-	±10	µA

Table 8: Input/Output DC Characteristics

[28]Refer to the JEDEC JEP122G standard for more details on each parameter of the equation

5.5 AC Characteristics

5.5.1 SDIO Interface

5.5.1.1 Full Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO Clock Period	T_{sdio}	40	-	-	ns
SDIO Data Input Setup Time	T_s	5	-	-	ns
SDIO Data Input Hold Time	T_h	5	-	-	ns
SDIO Data Output – Clock-to-Output-Valid time during data transfer	T_{odd}	0	-	14	ns
SDIO Data Output – Clock-to-Output-Valid time during identification	T_{odi}	0	-	50	ns
Output Load		0	-	40	pF

Table 9: AC Characteristics – SDIO Full Speed Mode (as per SDIO v2.0 Protocol)

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO Clock Period	T_{sdio}	40	-	-	ns
SDIO Data Input Setup Time	T_s	4	-	-	ns
SDIO Data Input Hold Time	T_h	1	-	-	ns
SDIO Data Output – Clock-to-Output-Valid time during data transfer	T_{odd}	0	-	12	ns
SDIO Data Output – Clock-to-Output-Valid time during identification	T_{odi}	0	-	50	ns
Output Load		0	-	40	pF

Table 10: AC Characteristics – SDIO Full Speed Mode (on Silicon)

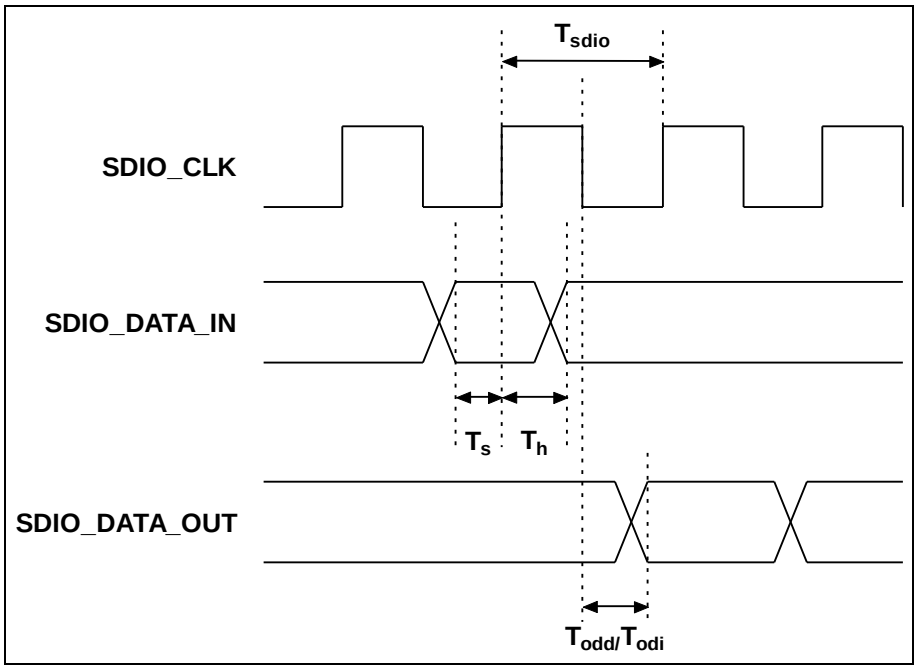

Figure 12: SDIO Interface Timings – Full Speed Mode

5.5.1.2 High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO Clock Period	T_{sdio}	20	-	-	ns
SDIO Data Input Setup Time	T_s	6	-	-	ns
SDIO Data Input Hold Time	T_h	2	-	-	ns
SDIO Data Output – Clock-to-Output-Valid time	T_{od}	-	-	14	ns
Output Load		0	-	40	pF

Table 11: AC Characteristics – SDIO High Speed Mode (as per SDIO v2.0 Protocol)

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO Clock Period	T_{sdio}	20	-	-	ns
SDIO Data Input Setup Time	T_s	4	-	-	ns
SDIO Data Input Hold Time	T_h	1	-	-	ns
SDIO Data Output – Clock-to-Output-Valid time	T_{od}	-	-	12	ns

Parameter	Symbol	Min.	Typ.	Max.	Units
Output Load		0	-	40	pF

Table 12: AC Characteristics – SDIO High Speed Mode (on Silicon)

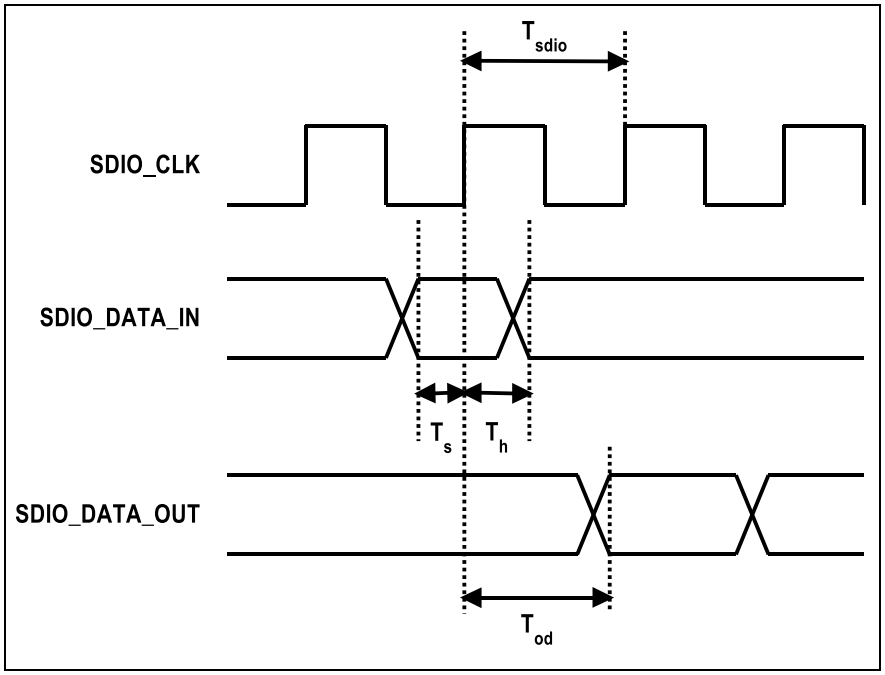

Figure 13: SDIO Interface Timings – High Speed Mode

5.5.2 SPI Slave (Host SPI) Interface

5.5.2.1 Low Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI Clock Period	T_{spi}	40	-	-	ns
SPI_CSN to Output Valid time	T_{cs}	-	-	7.5	ns
SPI_CSN Setup Time	T_{cst}	5	-	-	ns
SPI_MOSI Setup Time	T_{sd}	1.5	-	-	ns
SPI_MOSI Hold Time	T_{hd}	1	-	-	ns
SPI_MISO Clock-to-Output-Valid time	T_{od}	-	-	10	ns
Output Load		0	-	10	pF

Table 13: AC Characteristics – Slave SPI Low Speed Mode

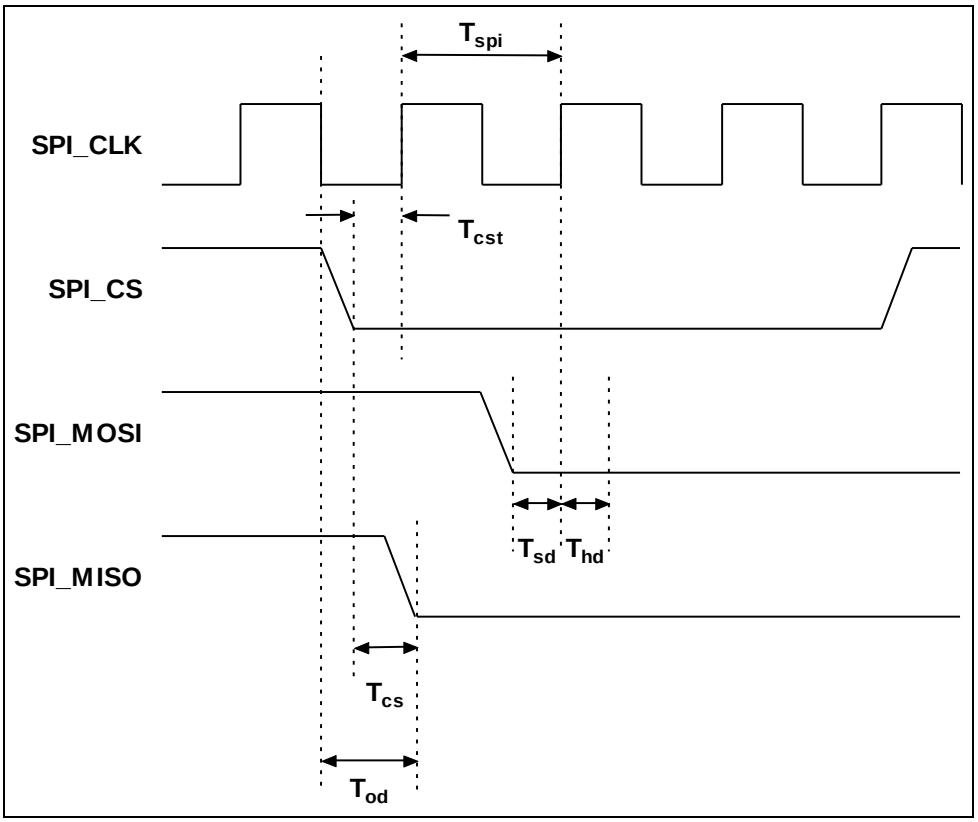

Figure 14: Slave SPI Interface Timings – Low Speed Mode

5.5.2.2 High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI Clock Period	T_{spi}	12.5	-	-	ns
SPI_CSN to Output Valid time	T_{cs}	-	-	7.5	ns
SPI_CSN Setup Time	T_{cst}	5	-	-	ns
SPI_MOSI Setup Time	T_{sd}	1	-	-	ns
SPI_MOSI Hold Time	T_{hd}	1	-	-	ns
SPI_MISO Clock-to-Output-Valid time	T_{od}	2.5	-	8.75	ns
Output Load		0	-	10	pF

Table 14: AC Characteristics – Slave SPI High Speed Mode

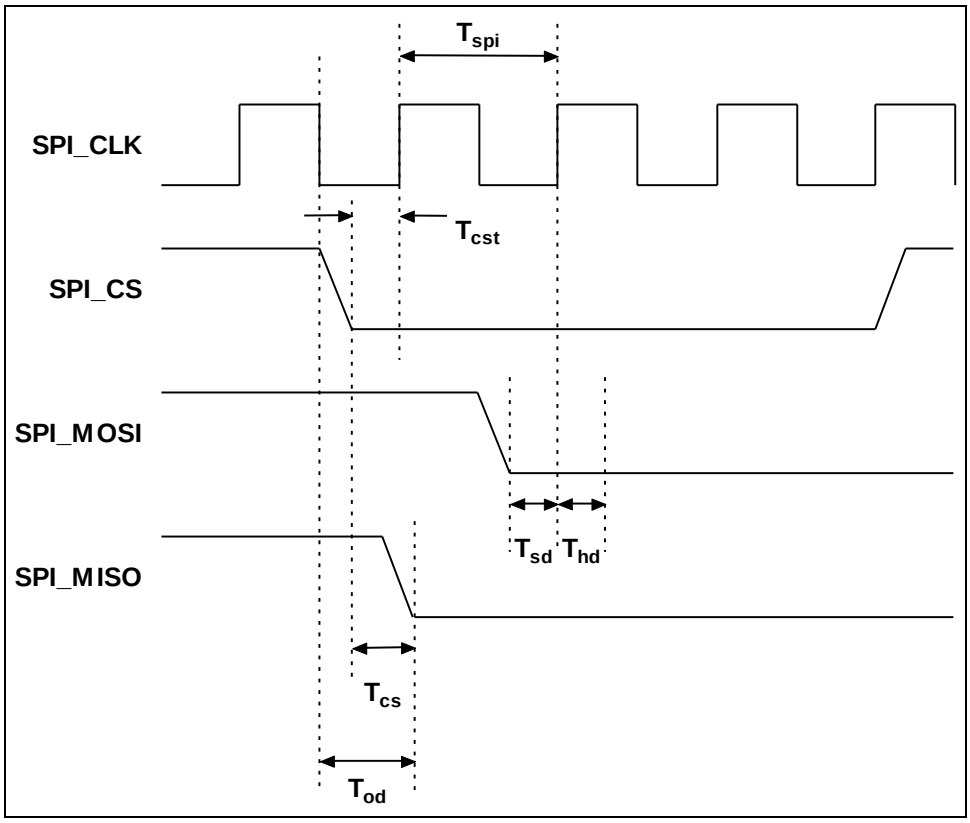

Figure 15: Slave SPI Interface Timings – High Speed Mode

5.5.3 I²C Interface

5.5.3.1 Fast Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
I2C_SCL Period	T_{i2c}	2.5	-	10	µs
I2C_SCL Low Period	T_{low}	1.3	-	-	µs
I2C_SCL High Period	T_{high}	0.6	-	-	µs
Start Condition, Setup time	T_{sstart}	0.6	-	-	µs
Start Condition, Hold time	T_{hstart}	0.6	-	-	µs
I2C_SDA, Setup Time	T_{sd}	100	-	-	µs
Stop Condition, Setup time	T_{sstop}	0.6	-	-	µs
Output Load		0		10	pF

Table 15: AC Characteristics – I²C Fast Speed Mode

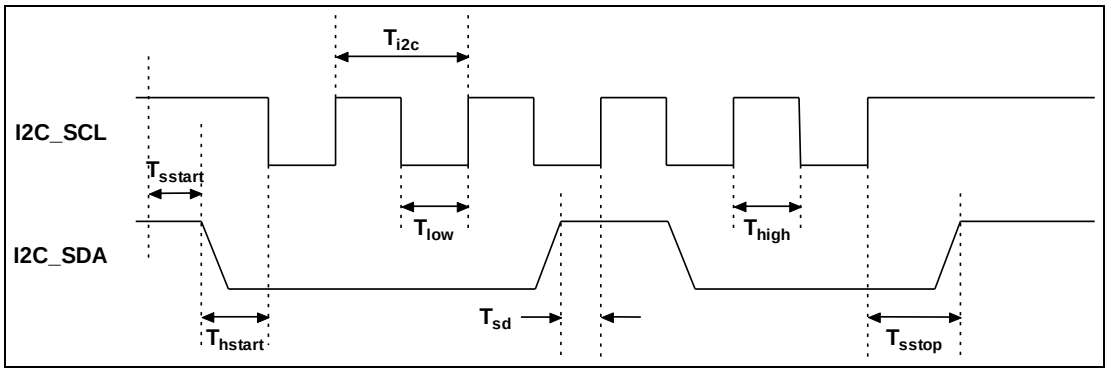

Figure 16: Interface Timings – I²C Fast Speed Mode

5.5.3.2 High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
I2C_SCL Period	T_{i2c}	0.3	-	2.5	µs
I2C_SCL Low Period	T_{low}	160	-	-	ns
I2C_SCL High Period	T_{high}	60	-	-	ns
Start Condition, Setup time	T_{sstart}	160	-	-	ns
Start Condition, Hold time	T_{hstart}	160	-	-	ns
I2C_SDA, Setup Time	T_{sd}	10	-	-	ns
I2C_SDA, Hold Time	T_{hd}	0	-	70	ns
Stop Condition, Setup time	T_{sstop}	160	-	-	ns
Output Load		0		10	pF

Table 16: AC Characteristics – I²C High Speed Mode

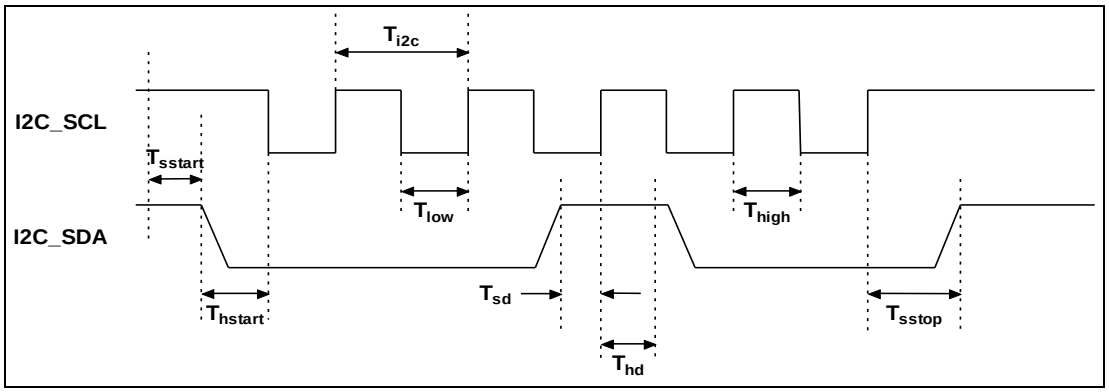

Figure 17: Interface Timings – I²C High Speed Mode

5.5.4 I²S and PCM Interfaces

Parameter	Symbol	Min.	Typ.	Max.	Units
I2S_CLK/PCM_CLK Period	T_{i2spcm}	30	-	-	ns
I2S_CLK/PCM_CLK Low Period	T_{low}	13	-	-	ns
I2S_CLK/PCM_CLK High Period	T_{high}	13	-	-	ns
I2S_DOUT/PCM_MISO Setup Time	T_{os}	18	-	-	ns
I2S_DOUT/PCM_MISO Hold Time	T_{oh}	3	-	-	ns
I2S_DIN/I2S_WS/PCM_MOSI/PCM_FSYNC Setup Time	T_{is}	10	-	-	ns
I2S_DIN/I2S_WS/PCM_MOSI/PCM_FSYNC Hold Time	T_{ih}	3	-	-	ns
Output Load		0		20	pF

Table 17: AC Characteristics – I²S and PCM

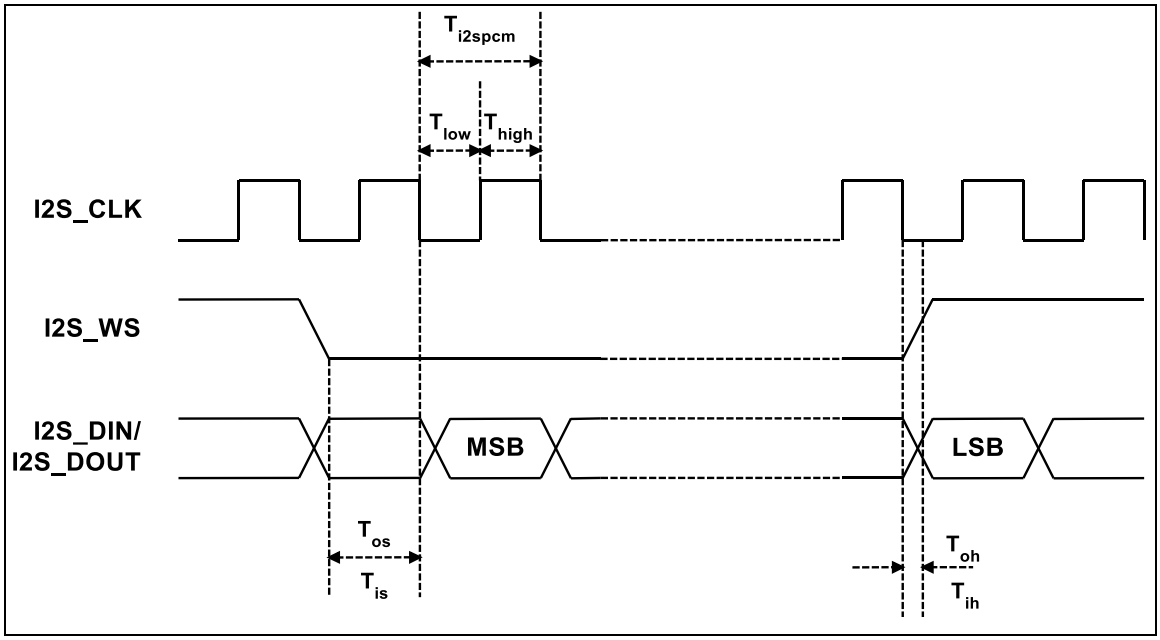

Figure 18: Interface Timings – I²S

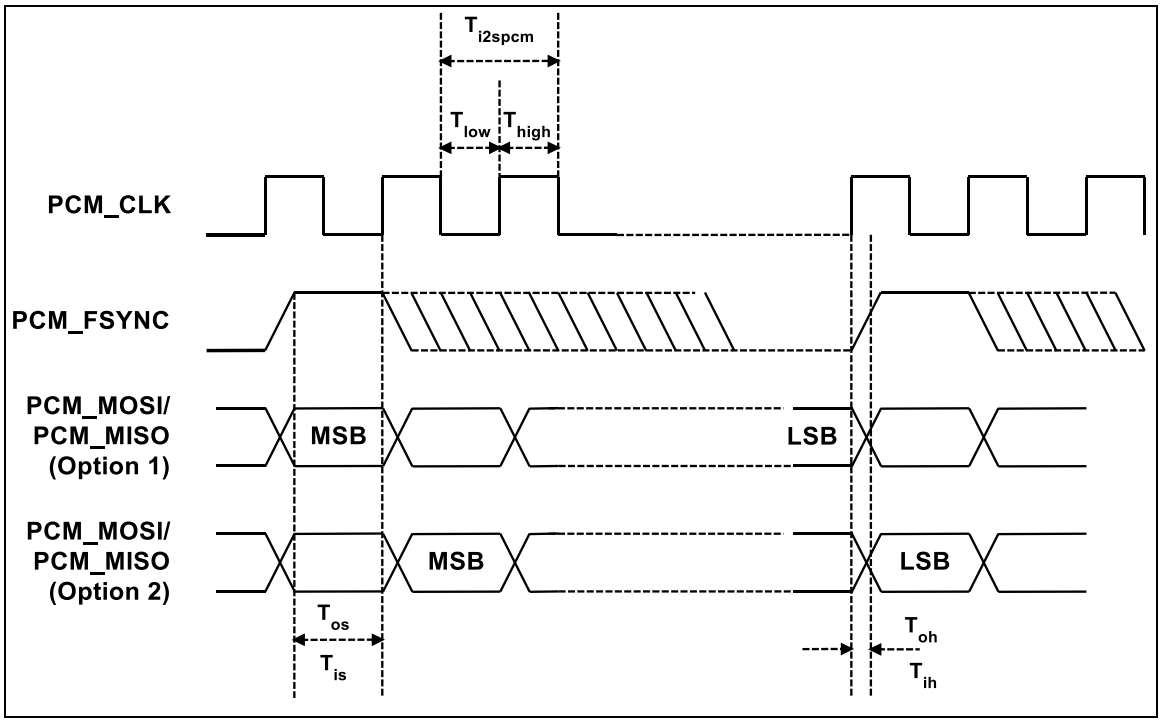

Figure 19: Interface Timings – PCM

NOTE: The PCM interface supports two modes – one where the MS bit of the frame is transmitted at the same rising clock edge as the FSYNC signal and the second where the MS bit is transmitted one clock cycle after the FSYNC signal is asserted. This is programmable and depicted in the above timing diagram as Option 1 and Option 2.

5.5.5 USB Interface

5.5.5.1 Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
t_{rise}	1.5 Mbps	75	-	300	ns
	12 Mbps	4	-	20	
	480 Mbps	0.5	-	-	
t_{fall}	1.5 Mbps	75	-	300	ns
	12 Mbps	4	-	20	
	480 Mbps	0.5	-	-	
Jitter	1.5 Mbps	-	-	10	ns
	12 Mbps	-	-	1	
	480 Mbps	-	-	0.2	

Table 18: Timing Characteristics for USB Interface

5.5.5.2 Electrical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{cm} DC (DC level measured at receiver connector)	HS Mode LS/FS Mode	-0.05 0.8	- -	0.5 2.5	V
Crossover Voltages	LS Mode FS Mode	1.3 1.3	- -	2 2	V
Power supply ripple noise (Analog 3.3V)	< 160 MHz	-50	-	50	mV

Table 19: Electrical Characteristics for USB Interface

5.5.5.3 Voltage Thresholds

Parameter	Min.	Typ.	Max.	Units
A-Device Session Valid	0.8	1.4	2.0	V
B-Device Session Valid	0.8	1.4	4.0	V
B-Device Session End	0.2	0.45	0.8	V

Table 20: Input/Output DC Characteristics

5.5.6 Reset Timing

The figure below shows the requirement for the Reset assertion time during power up and during module operation.

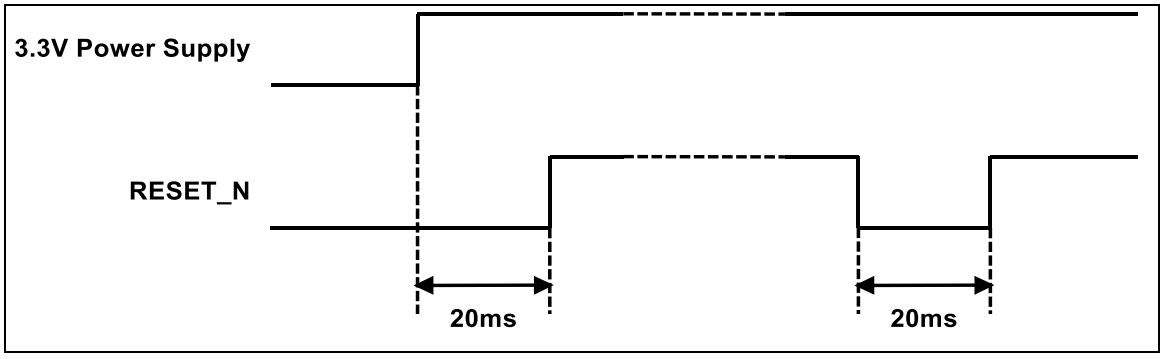

Figure 20: Reset Timing

5.6 Regulatory Specifications and Certifications

5.6.1 Regulatory Specifications

The modules have been certified for FCC, IC ,CE/ETSI and TELEC. Note that any changes to the module's configuration including (but not limited to) the programming values of the RF

Transceiver and Baseband can cause the performance to change beyond the scope of the certification. These changes, if made, may result in the module having to be certified afresh.

The table below lists the details of the regulatory certifications.

Regulatory Certification	Grantee Code	Product Code	Description
FCC	XF6	RS9113SB	Single-band Module
FCC	XF6	RS9113DB	Dual-band Module
IC	8407A	RS9113SB	Single-band Module
IC	8407A	RS9113DB	Dual-band Module
TELEC	005-101325	RS9113SB	Single-band Module
TELEC	005-101228	RS9113DB	Dual-band Module

Table 21: Regulatory Certifications

NOTE: Click on the links below for details on product variants and ordering information:

1) Product Variants
2) Ordering Information

5.6.2 Software Certifications

The module's software has been certified for Wi-Fi Alliance and Bluetooth-SIG test plans. The table below lists the details of the certifications. Contact Redpine Signals Sales (sales@redpinesignals.com) for information on certifications not listed here.

Wireless Protocol	Certifying Authority	Certification ID	Software Variant Certified
Wi-Fi (802.11 a/b/g/n)	Wi-Fi Alliance®	WFA64481	WiSeConnect™
Bluetooth	Bluetooth SIG	QD ID: 83360 (Bluetooth 4.0) QD ID: 79352 (Bluetooth 2.1)	n-Link™ and WiSeConnect™

Table 22: Software Certifications

The details of the features certified are available at the hyperlinks for each Certification ID.

6 Software Architecture

6.1 n-Link® Software Architecture

The n-Link® Software Architecture is a host based architecture with the OS providing the core functionality support for Wi-Fi, Bluetooth and ZigBee features and having zero load in the data path. The kernel layer interfaces with the host driver to provide functionality for different wireless modules.

The figure below illustrates the n-Link® Software Architecture with WLAN, Bluetooth and ZigBee.

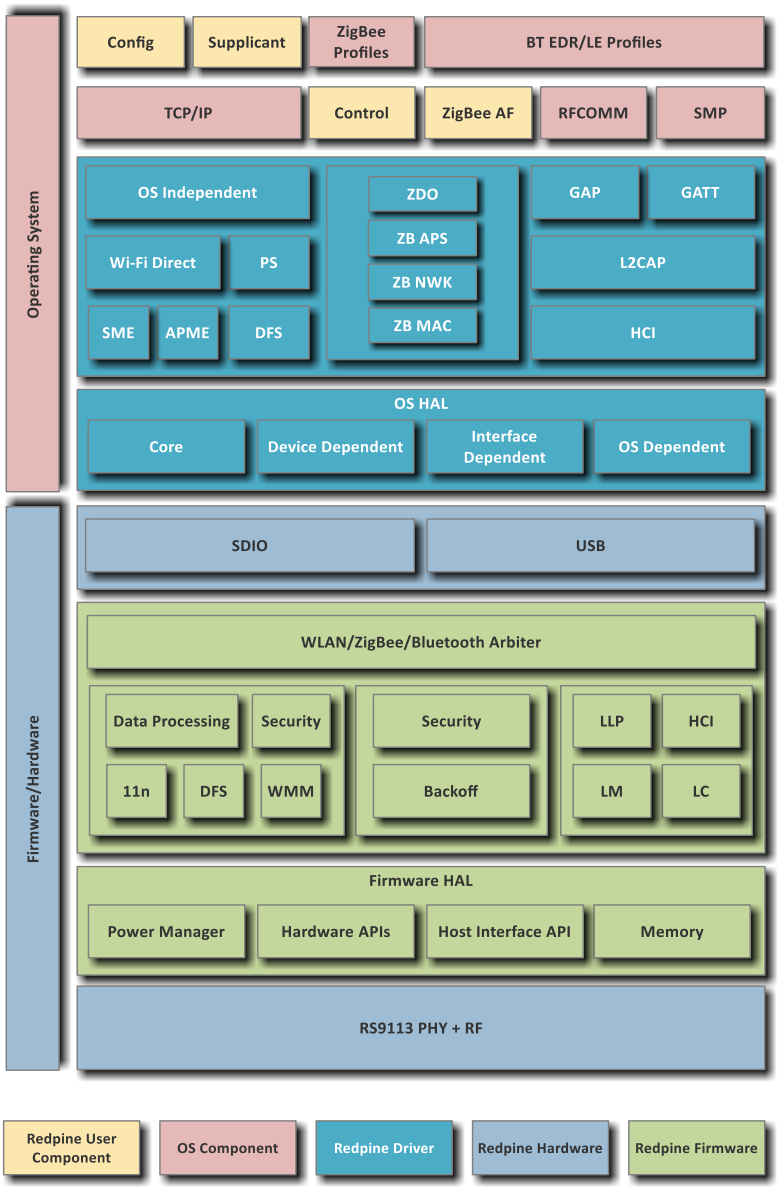

Figure 21: n-Link®Software Architecture

6.1.1 Operating System Support

The n-Link® modules support the following versions of Linux and Android OS:

1) Linux kernel versions between 2.6.30 and 3.16
2) Wind River Linux 5.0.1
3) Android 4.4.3

Operating Systems to be supported in the future include Windows.

6.2 WiSeConnect®/Connect-io-n® Software Architecture

The figure below illustrates the software architecture of the WiSeConnect®/Connect-io-n® modules.

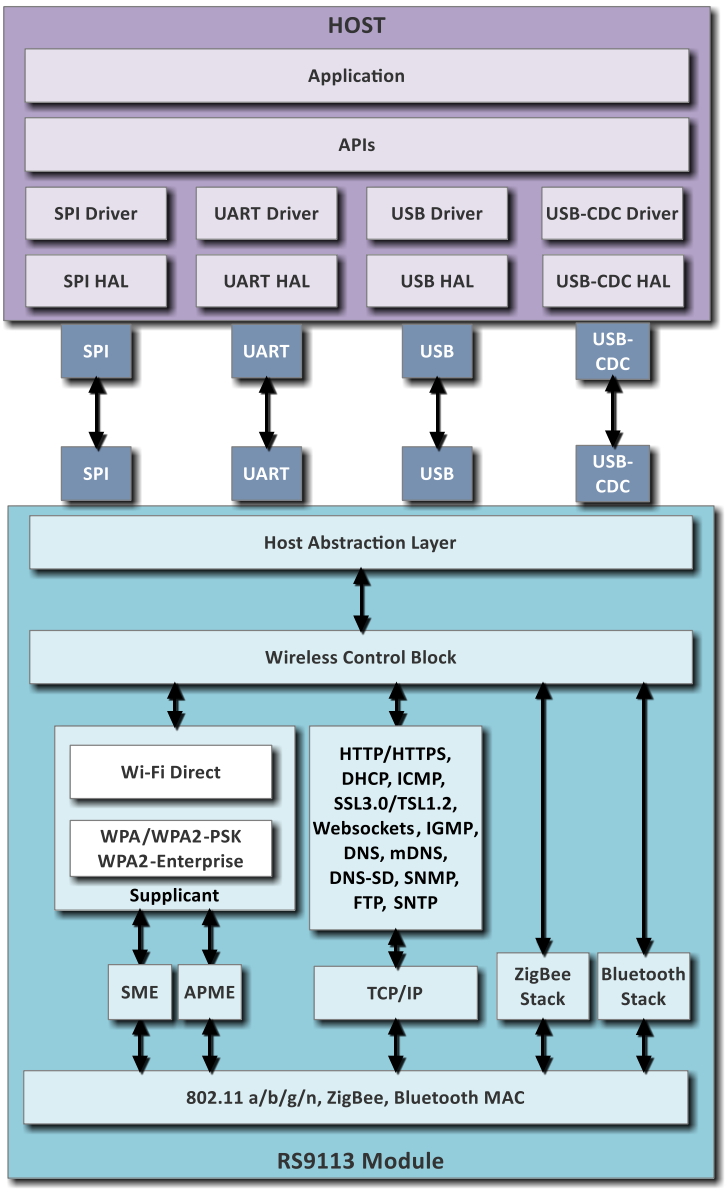

Figure22: WiSeConnect®/Connect-io-n® Software Architecture

As shown in the figure above, the WiSeConnect®/Connect-io-n® module is integrated with the host using the SPI, UART, USB or USB-CDC interface. The module receives all configuration commands from the Host and transfers data to or receives data from the host through this interface.

The module incorporates Wi-Fi Direct™, Access Point, WPA/WPA2-PSK, WPA/WPA2-Enterprise (EAP-TLS, EAP-FAST, EAP-TTLS, EAP-PEAP, EAP-LEAP) Security[29], Client Mode, Web-Server, TCP/IP Stack, DHCP Server, ARP, WPA supplicant, ZB stack, BT stack and profiles etc., to act as a wireless device server. It handles all the network connectivity functions.[30]

[29]Wi-Fi Direct™ and Enterprise Security modes are supported only in WiSeConnect® modules.
[30]Contact Redpine Signals Sales (sales@redpinesignals.com) for more details on what combination of features are supported.

7 Module Marking and Ordering Information

7.1 Module Marking Information

The figure below illustrates the marking on the modules.

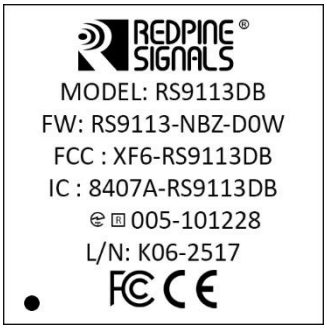

Figure 23: Module Marking Information

The table below explains the marking on the modules.

Marking	Description
RS9113SB RS9113DB	Model Numbers for Single-band and Dual-band modules
RS9113-NB0-S0W	Software/Firmware supported – refer to the Product Naming and Variants section for more details.
XF6-RS9113SB XF6-RS9113DB	FCC Grant IDs for Single-band and Dual-band modules
8407A-RS9113SB 8407A-RS9113DB	IC Grant IDs for Single-band and Dual-band modules
005-101325 005-101228	Japan Type Approval Certificate Number for Single-band and Dual-band modules
ABC-WWYY ABC-WWYY-N	Lot Code Information: ABC – Internal usage WW – Week of manufacture YY – Year of manufacture N - Alternate Flash devices have been added due to the EOL of original Flash device
FC	FCC Compliance Mark
CE	CE Compliance Mark

Marking	Description
	TELEC Compliance Mark

Table 23: Module Marking Information

7.2 Ordering Information

The RS9113 Module Family has the following variants.

Module Part #	Wi-Fi 2.4GHz	Wi-Fi 5GHz	BT	ZB	Integrated Antenna &U.FL	SW Variant	Host Interface					Package #
							SDIO	USB	SPI	UART	USB-CDC	
RS9113-N00-S0N	Y	N	N	N	N	n-Link®	Y	Y	N	N	N	P6
RS9113-N00-D0N	Y	Y	N	N	N	n-Link®	Y	Y	N	N	N	P6
RS9113-N00-S1N	Y	N	N	N	Y	n-Link®	Y	Y	N	N	N	P7
RS9113-N00-D1N	Y	Y	N	N	Y	n-Link®	Y	Y	N	N	N	P7
RS9113-NB0-S0N	Y	N	Y	N	N	n-Link®	Y	Y	N	N	N	P6
RS9113-NB0-D0N	Y	Y	Y	N	N	n-Link®	Y	Y	N	N	N	P6
RS9113-NB0-S1N	Y	N	Y	N	Y	n-Link®	Y	Y	N	N	N	P7
RS9113-NB0-D1N	Y	Y	Y	N	Y	n-Link®	Y	Y	N	N	N	P7
RS9113-N0Z-S0N	Y	N	N	Y	N	n-Link®	Y	Y	N	N	N	P6
RS9113-N0Z-D0N	Y	Y	N	Y	N	n-Link®	Y	Y	N	N	N	P6
RS9113-N0Z-S1N	Y	N	N	Y	Y	n-Link®	Y	Y	N	N	N	P7
RS9113-N0Z-D1N	Y	Y	N	Y	Y	n-Link®	Y	Y	N	N	N	P7
RS9113-NBZ-S0N	Y	N	Y	Y	N	n-Link®	Y	Y	N	N	N	P6
RS9113-NBZ-D0N	Y	Y	Y	Y	N	n-Link®	Y	Y	N	N	N	P6
RS9113-NBZ-S1N	Y	N	Y	Y	Y	n-Link®	Y	Y	N	N	N	P7
RS9113-NBZ-D1N	Y	Y	Y	Y	Y	n-Link®	Y	Y	N	N	N	P7
RS9113-N00-S0W	Y	N	N	N	N	WiSeConnect®	N	Y	Y	Y	Y	P6
RS9113-N00-D0W	Y	Y	N	N	N	WiSeConnect®	N	Y	Y	Y	Y	P6
RS9113-N00-S1W	Y	N	N	N	Y	WiSeConnect®	N	Y	Y	Y	Y	P7
RS9113-N00-D1W	Y	Y	N	N	Y	WiSeConnect®	N	Y	Y	Y	Y	P7

Module Part #	Wi-Fi 2.4GHz	Wi-Fi 5GHz	BT	ZB	Integrated Antenna &U.FL	SW Variant	Host Interface					Package #
							SDIO	USB	SPI	UART	USB-CDC	
RS9113-NB0-S0W	Y	N	Y	N	N	WiSeConnect®	N	Y	Y	Y	Y	P6
RS9113-NB0-D0W	Y	Y	Y	N	N	WiSeConnect®	N	Y	Y	Y	Y	P6
RS9113-NB0-S1W	Y	N	Y	N	Y	WiSeConnect®	N	Y	Y	Y	Y	P7
RS9113-NB0-D1W	Y	Y	Y	N	Y	WiSeConnect®	N	Y	Y	Y	Y	P7
RS9113-N0Z-S0W	Y	N	N	Y	N	WiSeConnect®	N	Y	Y	Y	Y	P6
RS9113-N0Z-D0W	Y	Y	N	Y	N	WiSeConnect®	N	Y	Y	Y	Y	P6
RS9113-N0Z-S1W	Y	N	N	Y	Y	WiSeConnect®	N	Y	Y	Y	Y	P7
RS9113-N0Z-D1W	Y	Y	N	Y	Y	WiSeConnect®	N	Y	Y	Y	Y	P7
RS9113-NBZ-S0W	Y	N	Y	Y	N	WiSeConnect®	N	Y	Y	Y	Y	P6
RS9113-NBZ-D0W	Y	Y	Y	Y	N	WiSeConnect®	N	Y	Y	Y	Y	P6
RS9113-NBZ-S1W	Y	N	Y	Y	Y	WiSeConnect®	N	Y	Y	Y	Y	P7
RS9113-NBZ-D1W	Y	Y	Y	Y	Y	WiSeConnect®	N	Y	Y	Y	Y	P7
RS9113-N00-S0C	Y	N	N	N	N	Connect-io-n®	N	Y	Y	Y	Y	P6
RS9113-N00-D0C	Y	Y	N	N	N	Connect-io-n®	N	Y	Y	Y	Y	P6
RS9113-N00-S1C	Y	N	N	N	Y	Connect-io-n®	N	Y	Y	Y	Y	P7
RS9113-N00-D1C	Y	Y	N	N	Y	Connect-io-n®	N	Y	Y	Y	Y	P7
RS9113-NB0-S0C	Y	N	Y	N	N	Connect-io-n®	N	Y	Y	Y	Y	P6
RS9113-NB0-D0C	Y	Y	Y	N	N	Connect-io-n®	N	Y	Y	Y	Y	P6
RS9113-NB0-S1C	Y	N	Y	N	Y	Connect-io-n®	N	Y	Y	Y	Y	P7
RS9113-NB0-D1C	Y	Y	Y	N	Y	Connect-io-n®	N	Y	Y	Y	Y	P7
RS9113-N0Z-S0C	Y	N	N	Y	N	Connect-io-n®	N	Y	Y	Y	Y	P6
RS9113-N0Z-D0C	Y	Y	N	Y	N	Connect-io-n®	N	Y	Y	Y	Y	P6
RS9113-N0Z-S1C	Y	N	N	Y	Y	Connect-io-n®	N	Y	Y	Y	Y	P7
RS9113-N0Z-D1C	Y	Y	N	Y	Y	Connect-io-n®	N	Y	Y	Y	Y	P7
RS9113-NBZ-S0C	Y	N	Y	Y	N	Connect-io-n®	N	Y	Y	Y	Y	P6

Module Part #	Wi-Fi 2.4GHz	Wi-Fi 5GHz	BT	ZB	Integrated Antenna &U.FL	SW Variant	Host Interface					Package #
							SDIO	USB	SPI	UART	USB-CDC	
RS9113-NBZ-D0C	Y	Y	Y	Y	N	Connect-io-n®	N	Y	Y	Y	Y	P6
RS9113-NBZ-S1C	Y	N	Y	Y	Y	Connect-io-n®	N	Y	Y	Y	Y	P7
RS9113-NBZ-D1C	Y	Y	Y	Y	Y	Connect-io-n®	N	Y	Y	Y	Y	P7

Table 24: RS9113 Module Variants

7.3 Collateral

7.3.1 Collateral for n-Link® Modules

The following documentation and software are available along with the n-Link® modules.

- Module Integration Guide.
- Device drivers
- Technical Reference Manual
- Evaluation Kit (EVK)
- EVK User Guide

7.3.2 Collateral for WiSeConnect®/Connect-io-n® Modules

The following documentation and software are available along with the WiSeConnect®/Connect-io-n® modules.

- Module Integration Guide
- API's for supported interfaces.
- API User Guide
- Software Programming Reference manual (PRM).
- Evaluation Kit (EVK)
- EVK User Guide

7.4 Packing Information

The modules are packaged and shipped in Trays.

Each tray for the P6 package can accommodate 84 modules. The mechanical details of the tray for the P6 package are given in the figure below.

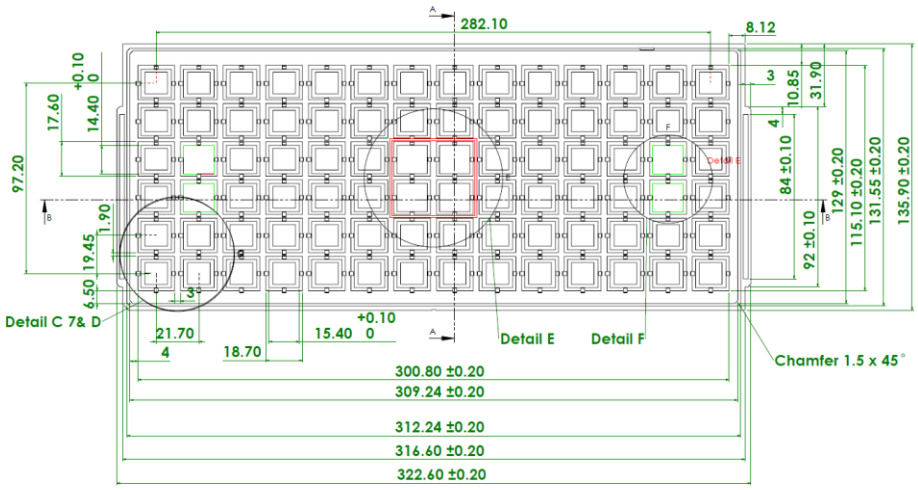

Figure 24: Mechanical Details of Tray for P6 Package

Each tray for the P7 package can accommodate 70 modules. The mechanical details of the tray for the P7 package are given in the figure below.

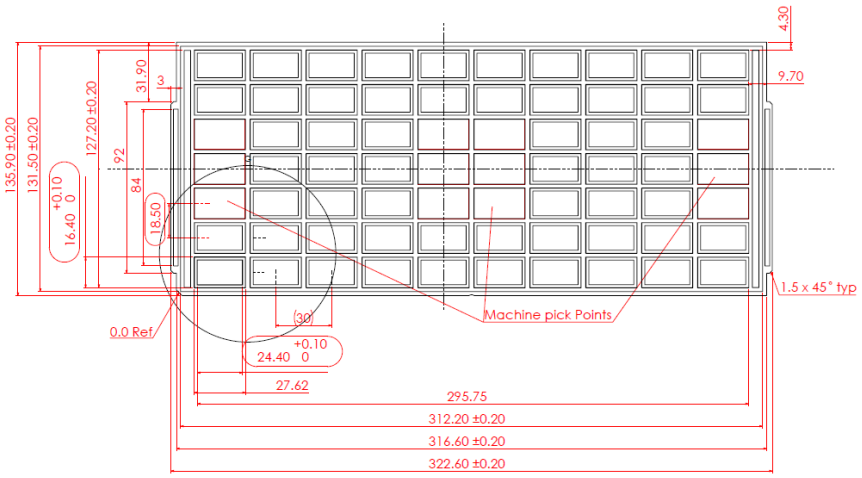

Figure 25: Mechanical Details of Tray for P7 Package

7.5 Contact Information

For additional information, please contact Sales at Redpine Signals, Inc.

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Phone: +1 408 748 3385

E-mail: sales@redpinesignals.com

Website: http://www.redpinesignals.com/

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Revision History

Revision No.	Version No.	Date	Changes
1.	3.0	April 2015	1) Merged the information from the n-Link® and WiSeConnect®/Connect-io-n® Modules' separate datasheets into a single document. 2) Merged the pin description tables for the two package variants. 3) Added detailed performance specifications. 4) Added Antenna specifications.
2.	3.1	June 2015	1) Corrected the Supported Operating Modes in Section 2 with respect to Wi-Fi Direct™. 2) Corrected the direction of GPIO_10/UART1_TX in Section 4.3. 3) Corrected the description for JN2 and JNC in Section 4.3. 4) Corrected information related to VBATT in Table 5 and Table 6. 5) Added WPA/WPA2-PSK in all places where WPA/WPA2-Enterprise is mentioned 6) Mentioned that the Access Point mode in WiSeConnect®/Connect-io-n® comes with limited packet buffering in Section 2. 7) Added missing 54 Mbps in the list of Data Rates in Section 2. 8) Added ECDH under Advanced Security Features in Section 2. 9) Added USB 1.1 as a supported interface in addition to USB 2.0. 10) Removed footnote related to FTP Client being offered in future software releases of WiSeConnect®/Connect-io-n®. This feature is supported now. 11) Added SNTP as a supported feature for WiSeConnect®/Connect-io-n®. 12) Added Android and Wind River Linux as supported OS' for n-Link® modules.
3.	3.2	July 2015	1) Updated the Supported Operating Modes in Section 2. 2) Added section on Current Consumption specifications. 3) Corrected mention of PEAP-MSCHAP-v2 to EAP-PEAP across the document. 4) Updated Bluetooth Profiles list for WiSeConnect®/Connect-io-n® - added iAP1. 5) Corrected directions of JP2 and JNC pins. 6) Updated Peak Gain specifications of Antenna.

Revision No.	Version No.	Date	Changes
4.	3.3	September 2016	1) Updated Features section. 2) Updated Tolerance Level for Mechanical Dimensions from ±0.1mm to ±0.2mm. 3) Updated Pin Description table with details of I^2C, I^2S and PCM pins details. 4) Updated Pin Description table for details of UART RTS and CTS signals. 5) Corrected pin numbers of JP1, JP2 and JNC signals for module without antenna in the Pin Description table. 6) Updated Absolute Maximum Rating for USB VBUS to 5.25V. 7) Added AC Characteristics for I^2C, I^2S and PCM interfaces. 8) Added information on Wi-Fi and Bluetooth certification.
5.	3.4	September 2017	1) Corrected the Pinout diagram for Module with Antenna (Package # P7). Pin number 51 is RESET_N and pin number 52 is VBATT. 2) Corrected the interface timings figure for SDIO High Speed mode. 3) Updated Module Marking information 4) Updated Regulatory specifications and certifications and ordering information to include TELEC compliance 5) Added a the Mounting view for module with integrated antenna 6) Added support for EAP-LEAP
6.	3.5	January 2018	1) Corrected Module Marking Information