UltraFast Precision 10ns Comparator

DESCRIPTION

The RH1016 is an UltraFast™ 10ns comparator that interfaces directly to TTL/CMOS logic while operating from either ±5V or single 5V supplies. Tight offset voltage specifications and high gain allow the RH1016 to be used in precision applications. Matched complementary outputs further extend the versatility of this comparator.

A unique output stage provides active drive in both directions for maximum speed into TTL/CMOS logic or passive loads, yet does not exhibit the large current spikes found in conventional output stages. This allows the RH1016 to remain stable with the outputs in the active region which greatly reduces the problem of output "glitching" when the input signal is slow moving or is low level.

The RH1016 has a LATCH pin which will retain input data at the outputs, when held high. Quiescent negative power supply current is only 3mA. This allows the negative supply pin to be driven from virtually any supply voltage with a simple resistive divider. Device performance is not affected by variations in negative supply voltage.

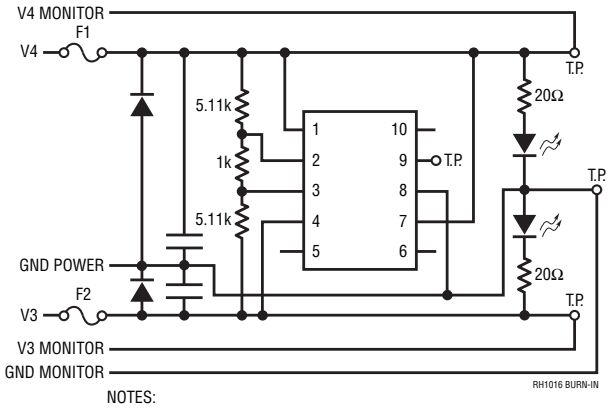
The wafer lots are processed to Linear Technology's in-house Class S flow to yield circuits usable in stringent military applications.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

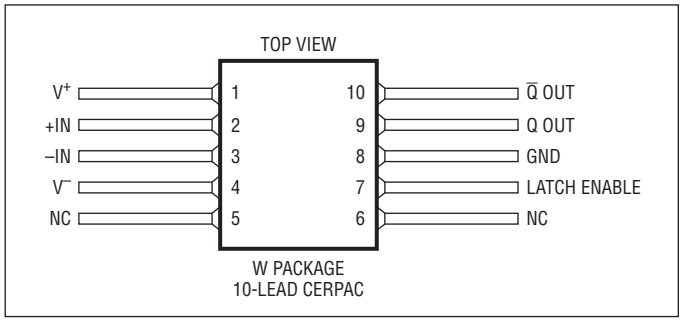
Positive Supply Voltage (Note 5)..... 7V
Negative Supply Voltage ..... –7V
Differential Input Voltage (Note 7)..... ±5V
+IN, –IN and LATCH ENABLE Current (Note 7) .... ±10mA
Output Current (Continuous) (Note 7) ..... ±20mA
Operating Temperature Range..... –55°C to 125°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

BURN-IN CIRCUIT



NOTES:
1. UNLESS OTHERWISE SPECIFIED, COMPONENT TOLERANCES SHALL BE PER MILITARY SPECIFICATION.
2. T_J = 161°C MAXIMUM
3. T_C = 139°C MINIMUM
4. T_A = 100°C MINIMUM
BURN-IN VOLTAGES: V4 = 5.5V TO 6V
V3 = –5.5V TO –6V

PACKAGE INFORMATION



W PACKAGE
10-LEAD CERPAC

TABLE 1: ELECTRICAL CHARACTERISTICS

(Preirradiation) V^+ = 5V, V^- = –5V, $V_{OUT(Q)}$ = 1.4V, V_{LATCH} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SUB-GROUP	–55°C ≤ T_A ≤ 125°C MIN	–55°C ≤ T_A ≤ 125°C TYP	–55°C ≤ T_A ≤ 125°C MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$	2		1	±3	1			±4	2, 3	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift								4			µV/°C
I_{OS}	Input Offset Current		2		0.3	1	1			1.3	2, 3	µA
I_B	Input Bias Current		3		5	10	1			13	2, 3	µA
	Input Voltage Range	 Single 5V Supply	6 6					–3.75 1.25		3.5 3.5		V V
CMRR	Common Mode Rejection	$-3.75V \le V_{CM} \le 3.5V$					1	80	90		2, 3	dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \le V^+ \le 5.4V$		60	75		1	54			2, 3	dB
		Negative Supply $-7V \le V^- \le -2V$		80	100		1	80			2, 3	dB
A_V	Small-Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		1400	3000		4					V/V
V_{OH}	Output High Voltage	$V^+ \ge 4.6V$, I_{OUT} = 1mA					1	2.65	3.2		2, 3	V
		I_{OUT} = 10mA					1	2.40	3		2, 3	V
V_{OL}	Output Low Voltage	I_{SINK} = 4mA					1		0.3	0.55	2, 3	V
I^+	Positive Supply Current						1		25	35	2, 3	mA
I^-	Negative Supply Current						1		3	5	2,3	mA
V_{IH}	LATCH Pin High Input Voltage							2				V
V_{IL}	LATCH Pin Low Input Voltage									0.8		V
I_{IL}	LATCH Pin Current	V_{LATCH} = 0V					1			500	2, 3	µA
t_{PD}	Propagation Delay	ΔV_{IN} = 100mV, OD = 5mV	4		10	14	4			16	5	ns
		ΔV_{IN} = 100mV, OD = 20mV	4		9	12	4			15	5	ns

TABLE 1A: ELECTRICAL CHARACTERISTICS

(Postirradiation) T_A = 25°C, V^+ = 5V, V^- = –5V, $V_{OUT(Q)}$ = 1.4V, V_{LATCH} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$	2		±4		±4.5		±5		±5.5		±6	mV
I_{OS}	Input Offset Current		2		2		2.5		5		8		12	µA
I_B	Input Bias Current		3		12		12		14		17		20	µA
	Input Voltage Range		6	–3.75	3.5	–3.75	3.5	–3.75	3.5	–3.75	3.5	–3.75	3.5	V
		Single 5V Supply	6	1.25	3.5	1.25	3.5	1.25	3.5	1.25	3.5	1.25	3.5	V
CMRR	Common Mode Rejection Ratio	$-3.75V \le V_{CM} \le 3.5V$		80		77		74		70		65		dB
PSRR	Supply Voltage Rejection	Positive Supply $4.6V \le V^+ \le 5.4V$		60		58		56		53		50		dB
		Negative Supply $-7V \le V^- \le -2V$		78		76		74		72		70		dB
A_V	Small-Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		1300		1200		1100		1000		900		V/V
V_{OH}	Output High Voltage	$V^+ \ge 4.6V$, I_{OUT} = 1mA		2.65		2.65		2.64		2.63		2.60		V
		I_{OUT} = 10mA		2.40		2.40		2.39		2.38		2.35		V
V_{OL}	Output Low Voltage	I_{SINK} = 4mA			0.55		0.55		0.56		0.57		0.6	V
I^+	Positive Supply Current				35		35		35		35		35	mA
I^-	Negative Supply Current				5		5		5		5		5	mA
I_{IL}	LATCH Pin Current	V_{LATCH} = 0V			525		575		650		725		800	µA
t_{PD}	Propagation Delay	ΔV_{IN} = 100mV, OD = 5mV	4		16		16		16		16		16	ns
		ΔV_{IN} = 100mV, OD = 20mV	4		14		14		14		14		14	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 3: Input bias current (I_B) is defined as the average of the two input currents.

Note 4: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The RH1016 is sample tested with a 1V step and 500mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} limits shown can be guaranteed with this test if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to overdrive.

Note 5: Electrical specifications apply only up to 5.4V.

Note 6: Input voltage range is guaranteed in part by CMRR testing and in part by design and characterization. See the LT1016 data sheet for discussion of input voltage range for supplies other than ±5V or 5V.

Note 7: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5
Group A Test Requirements (Method 5005)	1*,2,3,4,5
Group B and D for Class S, End Point Electrical Parameters (Method 5005)	1,2,3

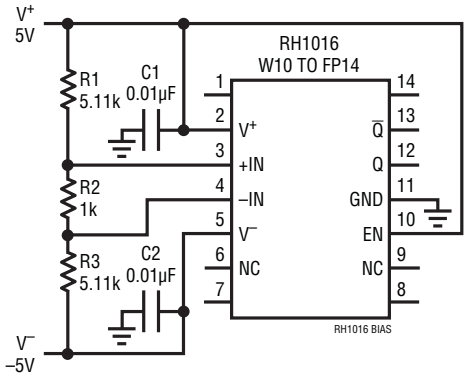
*PDA applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

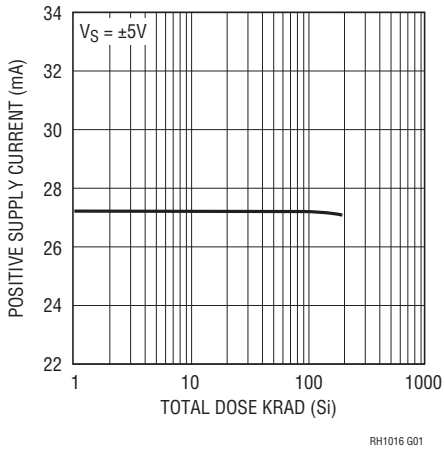
Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT

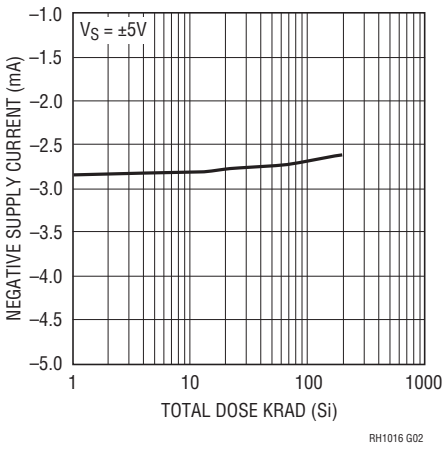


TYPICAL PERFORMANCE CHARACTERISTICS

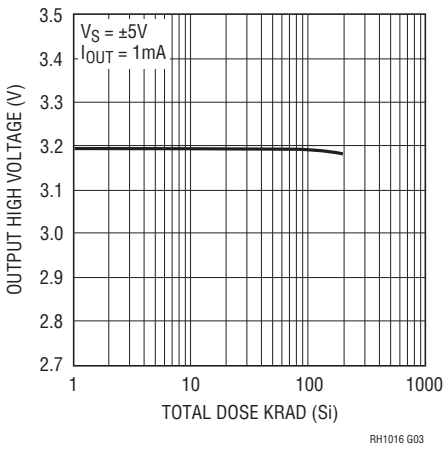
Positive Supply Current



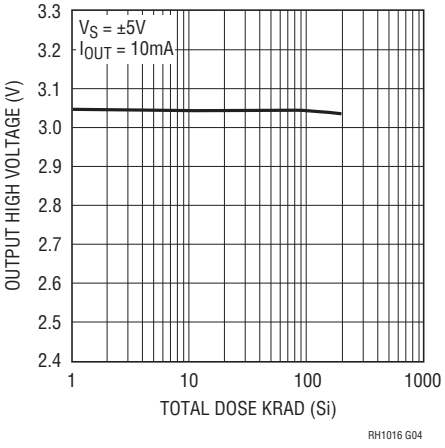
Negative Supply Current



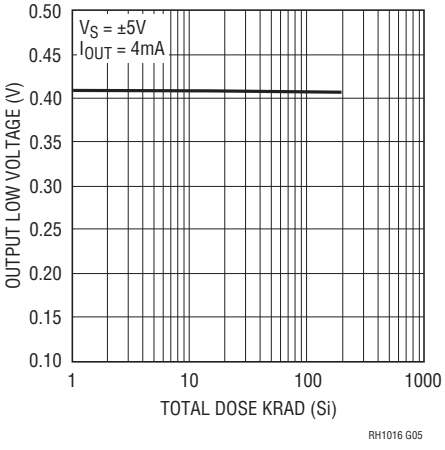
Output High Voltage



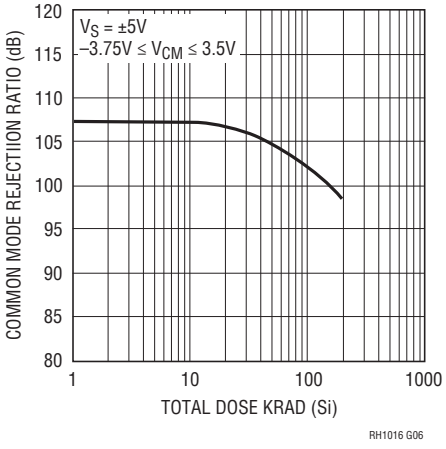
Output High Voltage



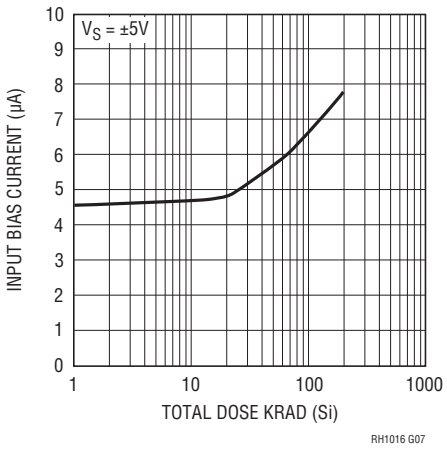
Output Low Voltage



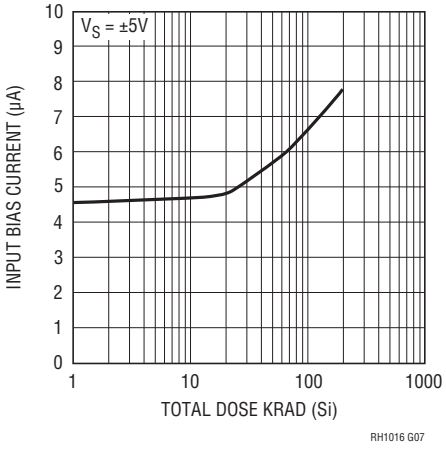
Common Mode Rejection Ratio



Input Bias Current

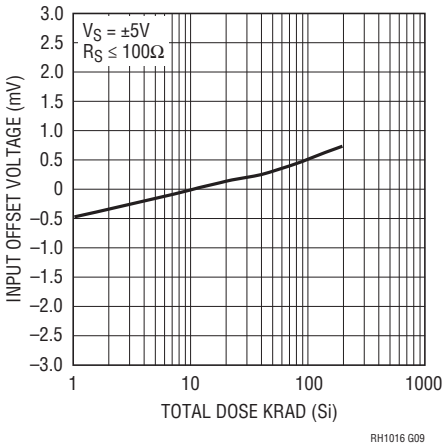


Input Offset Current

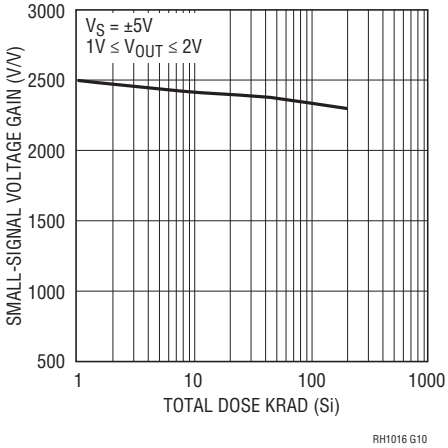


TYPICAL PERFORMANCE CHARACTERISTICS

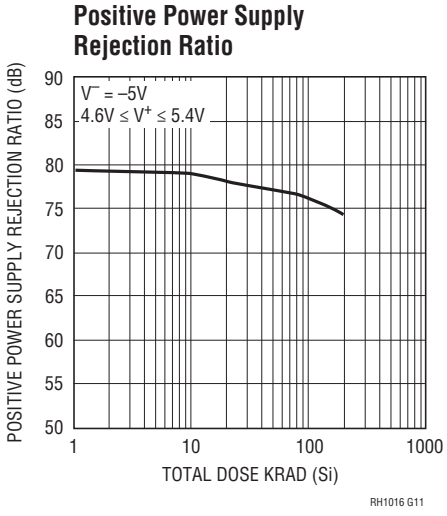
Input Offset Voltage



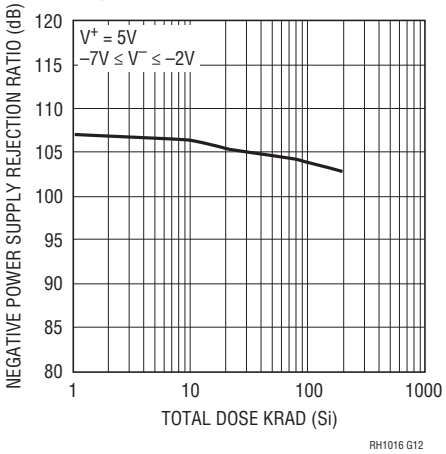
Small-Signal Voltage Gain



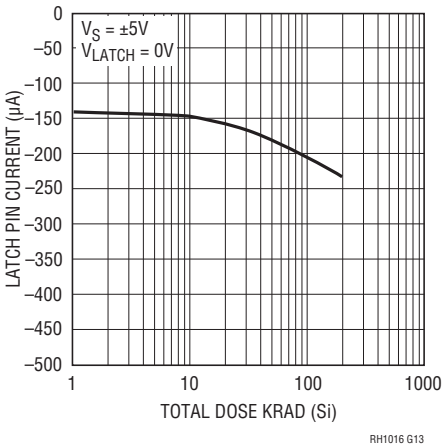
Positive Power Supply Rejection Ratio



Negative Power Supply Rejection Ratio



LATCH Pin Current



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