CY8CMBR3145,CY8CMBR3155 CY8CMBR3175 Datasheet

CapSense® Controller with SmartSense™ Auto-Tuning, 8 Buttons for Mobile Solutions

General Description

The CY8CMBR31x5 CapSense® controllers support up to eight sensing inputs and are ideal for implementing capacitive buttons, sliders, and proximity sensing user interface solutions. These controllers have been optimized for the mobile market and support advanced features, such as water-tolerant designs (mist, water droplets, or streaming water), glove touch up to 4-mm thick, and 1-mm passive stylus.

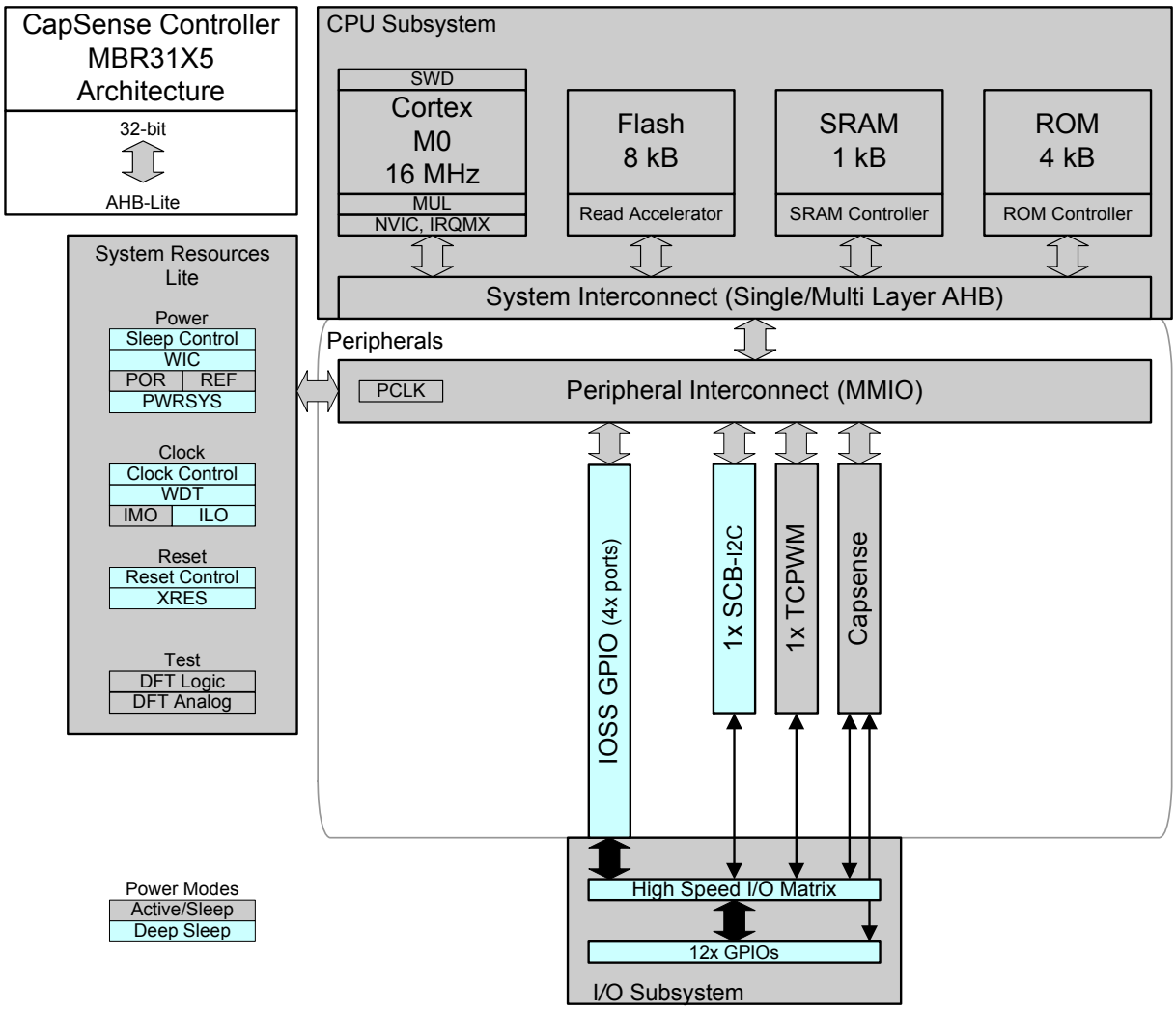
The CY8CMBR31x5 family features an advanced analog sensing channel and the Capacitive Sigma Delta PLUS (CSD PLUS) sensing algorithm, which delivers a signal-to-noise ratio (SNR) of greater than 100:1 to ensure touch accuracy even in extremely noisy environments. These controllers are enabled with Cypress's SmartSense™ Auto-tuning algorithm, which compensates for manufacturing variations and dynamically monitors and maintains optimal sensor performance in all environmental conditions. In addition, SmartSense Auto-tuning enables a faster time-to-market by eliminating the time-consuming manual tuning efforts during development and production ramp-up. These devices are offered in a 16-QFN package.

Features

- Programmable CapSense controller
  - Patented CSD sensing algorithm
  - High sensitivity (0.1 pF)
    - Overlay thickness of up to 15 mm for glass and 5 mm for plastic
    - Proximity solutions
  - Best-in-class >100:1 SNR performance
    - Superior noise-immunity performance against conducted and radiated noise
    - Ultra-low radiated emissions
  - SmartSense Auto-tuning
    - Sets and maintains optimal sensor performance during run-time
    - Eliminates manual tuning during development and production
- Low-power CapSense
  - Average current consumption of 13 µA per sensor at 120-ms scan time
  - Wide parasitic capacitance (CP) range: 5-45 pF
- Advanced user interface features
  - Water tolerance
  - Buzzer signal output for audible touch feedback
  - Attention line interrupt to the host to indicate any change in sensor status
- 32-bit MCU Sub-system
  - 16-MHz ARM Cortex-M0 CPU
  - 8-KB flash
  - 1-KB SRAM
- Low-power 1.71-V to 5.5-V operation
  - Deep Sleep mode with wake-up on interrupt and I^2C address detect
- Industrial temperature range: -40 °C to +85 °C
- I^2C slave
  - Supports up to 400 kHz
  - Wake-on-hardware address match
- PSoC Creator Design Environment
  - Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
  - Applications programming interface (API) component for all fixed-function and programmable peripherals including CapSense
- Industry-standard tool compatibility
  - After schematic entry, development can be done with ARM-based industry-standard development tools
- Package options
  - 16-pin QFN (3 × 3 × 0.6 mm)

Contents

Figure 1. Block Diagram



CY8CMBR31x5 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for CY8CMBR31x5 devices. The SWD interface is fully compatible with industry standard third party tools. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the CY8CMBR31x5 family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, CY8CMBR31x5 with device security enabled may not be returned for failure analysis. This is a trade-off that the CY8CMBR31x5 allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the CY8CMBR31x5 is part of the 32-bit MCU subsystem, which is optimized for low power operation with extensive clock gating. Most instructions are 16-bits in length and the CPU executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4. It includes a nested vectored interrupt controller (NVIC) block with 8 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode allowing power to be switched off to the main processor when the chip is in Deep Sleep mode. The Cortex-M0 CPU also provides a Non-Maskable Interrupt input (NMI), which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the Serial Wire Debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for CY8CMBR31x5 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The CY8CMBR31x5 has a flash module with a flash accelerator tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver zero wait-state (WS) access time at 16 MHz.

SRAM

1K bytes of SRAM are provided with zero wait-state access at 16 MHz.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section Power on page 7. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on Power-On Reset) until voltage levels are as required for proper functionality or generates resets (for example, on Brown-Out Detection). The CY8CMBR31x5 operates with a single external supply over the range of 1.8 V ±5% or 1.8 to 5.5 V, and has three different power modes. Transitions between these modes are managed by the power system. The CY8CMBR31x5 provides Active, Sleep, and Deep Sleep low-power modes.

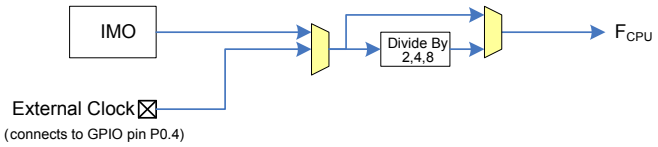
All sub-systems are operational in the Active mode. The CPU sub-system (CPU, Flash, and SRAM) is clock-gated off in the Sleep mode while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In the Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µS.

Clock System

The CY8CMBR31x5 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for the CY8CMBR31x5 consists of the IMO and the ILO internal oscillators and provision for an external clock.

Figure 2. CY8CMBR31x5 MCU Clocking Architecture



The F_{CPU} signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are a total of four clock dividers for the CY8CMBR31x5, each with 16-bit divide capability. The 16-bit capability enables flexible generation fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the CY8CMBR31x5. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2% (24 and 32 MHz).

ILO Clock Source

The ILO is a very low power 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in the Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register, which is firmware readable.

Reset

The CY8CMBR31x5 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows the software to determine the cause of the reset. An internal power-on reset (POR) is provided on the 16-pin package.

Voltage Reference

The CY8CMBR31x5 reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a ±5% reference.

Analog Blocks

Low-power Comparators

The CY8CMBR31x5 has a low-power comparator, which uses the built-in voltage reference. Any pin can be used as a Compare input and the output of the comparator can be brought out to a pin. The selected comparator input is connected to the minus input of the comparator with the plus input always connected to the 1.2-V voltage reference. This comparator is also used for CapSense purposes and is not available during CapSense operation.

Current DACs

The CY8CMBR31x5 has two current DACs (IDACs), which can drive any pin on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Busses

The CY8CMBR31x5 has two concentric independent busses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs and comparator) to connect to any port pin. Sets of pins can be driven under firmware control.

Fixed Function Digital

Timer/Counter/PWM Block

The Timer/Counter/PWM block consists of a 16-bit counter with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention.

Serial Communication Blocks (SCB)

The CY8CMBR31x5 has a serial communication block, which implements a multi-master I^2C interface.

I^2C Mode: The hardware I^2C block implements a slave interface. This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EzI2C that creates a mailbox address range in the memory of the CY8CMBR31x5 and effectively reduces I^2C communication to reading from and writing to an array in memory.

In addition, the block supports an 8-deep FIFO for receive and transmit which increases the time given for the CPU to read data. This greatly reduces the need for clock stretching caused by the CPU not having read data on time. The I^2C peripheral is compatible with the I^2C Standard-mode and Fast Mode devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in the open-drain mode.

The CY8CMBR31x5 is not completely compliant with the I^2C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

GPIO

The CY8CMBR31x5 has 12 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (3 for CY8CMBR31x5 because its pins are associated with three logical ports).

Special Function Peripherals

CapSense

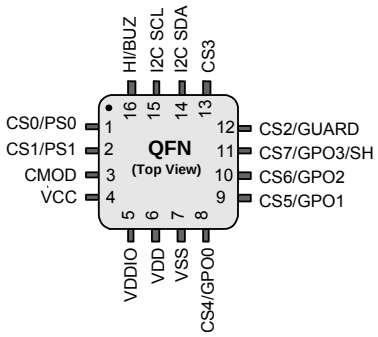
CapSense is supported on eight pins (Capsense pins) in the CY8CMBR31x5 through a CapSense Sigma-Delta (CSD) block that can be connected to any Capsense pin via analog switches that connect to an amux bus. The CapSense function can thus be provided on any available pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another amux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

Pinouts

CY8CMBR31x5 (8 Sensing Inputs)

Table 1. Pin Diagram and Definitions - CY8CMBR31x5

16-QFN						Pin Diagram
Pin #	Pin Name	Type	Description	If unused	Default Configuration	
1	CS0/PS0	–	CapSense Button / Proximity Sensor, controls GPO0	Ground/Ground	CS0	
2	CS1/PS1	–	CapSense Button / Proximity Sensor, controls GPO1	Ground/Ground	CS1	
3	CMOD	–	External modulator capacitor. Connect 2.2 nF/5 V/X7R or NPO capacitor	NA	CMOD	
4	VCC	Power	Connect 0.1-µF capacitor and leave it floating for operation at > 1.8 V. Connect to VDD for 1.8-V operation	NA	VCC	
5	VDDIO	Power	Power for I2C and $\overline{HI}$ lines	Connect to VDD	VDDIO	
6	VDD	Power	Power	NA	VDD	
7	VSS	Power	Ground	NA	VSS	
8	CS4/GPO0	I/DO	CapSense Button / GPO	Ground/Leave open	GPO0	
9	CS5/GPO1	–	CapSense Button / GPO	Ground/Leave open	GPO1	
10	CS6/GPO2	I/DO	CapSense Button / GPO	Ground/Leave open	GPO2	
11	CS7/GPO3/ SH	I/DO	CapSense Button / GPO/ Shield electrode	Ground/Leave open/Leave open	GPO3	
12	CS2/GUARD	–	CapSense Button, controls GPO0 / Guard Sensor	Leave open/Leave open	CS2	
13	CS3	–	CapSense Button, controls GPO3	Ground	CS3	
14	I2C SDA	DIO	I2C Data	Leave open	I2C SDA	
15	I2C SCL	DIO	I2C Clock	Leave open	I2C SCL	
16	$\overline{HI}$/BUZ	DO	Host Interrupt/Buzzer Output Supply voltage for Buzzer and pull-up resistor on HI should be equal to VDDIO	Leave open/leave open	$\overline{HI}$	
17	Center Pad	E-pad	Connect to VSS for best mechanical, thermal and electrical performance	Floating, not connected to any other signal	E-pad	

Legend: I = Analog Input, O = Analog Output, DIO = Digital Input/Output, CS = CapSense Button, PS = Proximity Sensor SH = Shield Electrode, BUZ = Buzzer Output, GPO = General Purpose Output, GUARD = Guard Sensor

Descriptions of the pin functions are as follows:

VDDD: Power supply for both analog and digital sections.

VDDIO: This pin provides a separate voltage domain (for details, refer to the "Power" section on page 7).

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V ±5%).

Power

The following power system diagram shows the set of power supply pins as implemented for the CY8CMBR31x5. The system has one regulator in the Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDD input. There is a separate regulator for the Deep Sleep mode. The supply voltage range is either 1.8 V ±5% or 1.8 V to 5.5 V with all functions and circuits operating over that range.

The VDDIO pin, available in the 16-pin QFN package, provides a separate voltage domain for the following pins: P3.0, P3.1, and P3.2. P3.0 and P3.1 can be I^2C pins and the chip can thus communicate with an I^2C system running at a different voltage (where VDDIO ≤ VDD). For instance, VDD can be 3.3 V and VDDIO can be 1.8 V.

The CY8CMBR31x5 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply.

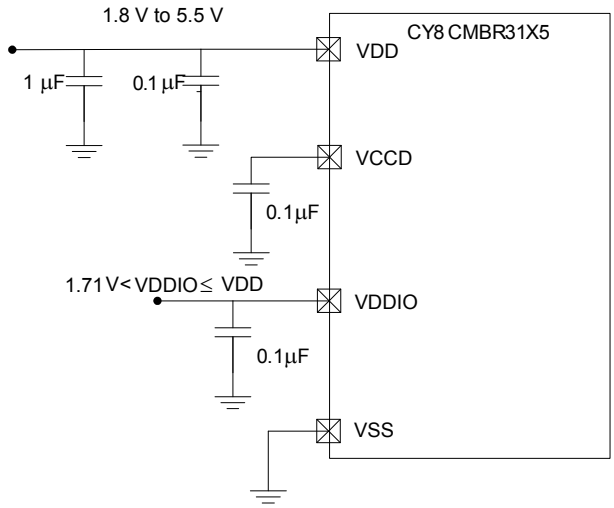
Unregulated External Supply

In this mode, the CY8CMBR31x5 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the CY8CMBR31x5 supplies the internal logic and the VCCD output of the CY8CMBR31x5 must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better).

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme follows (VDDIO is available on the 16-pin QFN package).

Power supply connections when 1.8 ≤ VDD ≤ 5.5 V

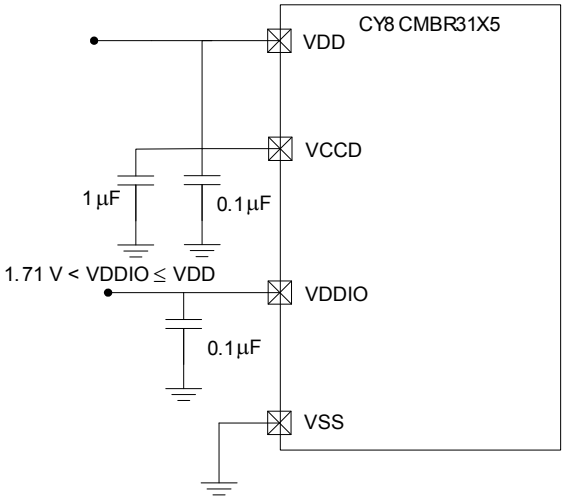


Regulated External Supply

In this mode, the CY8CMBR31x5 is powered by an external power supply that must be within the range of 1.71 to 1.89 V (1.8 ±5%); note that this range needs to include power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

An example of a bypass scheme follows (VDDIO is available on the 16-pin QFN package).

Power supply connections when 1.71 ≤ VDD ≤ 1.89 V



Development Support

The CY8CMBR31x5 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the CY8CMBR31x5 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the CY8CMBR31x5 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95	V	
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5	V	
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–140	–	140	mA	

Device Level Specifications

All specifications are valid for -40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
SID255	V_{DD}	Power supply input voltage (V_{CCD} = V_{DD})	1.71	–	1.89	V	Internally unregulated supply
SID54	V_{DDIO}	V_{DDIO} domain supply	1.71	–	V_{DD}	V	
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.8 to 5.5 V							
SID9	I_{DD5}	Execute from Flash; CPU at 6 MHz	–	2.0	2.85	mA	
SID12	I_{DD8}	Execute from Flash; CPU at 12 MHz	–	3.2	3.75	mA	
SID16	I_{DD11}	Execute from Flash; CPU at 16 MHz	–	4.0	4.5	mA	
Sleep Mode, V_{DDD} = 1.71 to 5.5 V							
SID25	I_{DD20}	I^2C wakeup, WDT on. 6 MHz	–	1.1	–	mA	
SID25A	I_{DD20A}	I^2C wakeup, WDT on. 12 MHz	–	1.4	–	mA	
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	8.2	µA	

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 3. DC Specifications *(continued)*

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	12	µA	
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	9.2	µA	
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Table 4. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	16	MHz	1.71 ≤ V_{DD} ≤ 5.5
SID49[2]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	
SID50[2]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	µs	

GPIO

Table 5. GPIO DC Specifications (referenced to VDDIO for 16-Pin QFN VDDIO pins)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[3]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID241	V_{IH}[3]	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	
SID243	V_{IH}[3]	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	

Notes
2. Guaranteed by characterization.
3. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 5. GPIO DC Specifications (referenced to VDDIO for 16-Pin QFN VDDIO pins) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	3	7	pF	
SID67[4]	V_{HYSTTL}	Input hysteresis LVTTL	15	40	–	mV	$V_{DDD} \geq 2.7$ V
SID68[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	$V_{DD} < 4.5$ V
SID68A[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–	mV	$V_{DD} > 4.5$ V
SID69[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	
SID69A[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	85	mA	

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	16	MHz	90/10% V_{IO}

Note
4. Guaranteed by characterization.

XRES

Table 7. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	7	pF	
SID81[5]	$V_{HYSXRES}$	Input voltage hysteresis	–	05*V_{DD}	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5V

Table 8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83[5]	$T_{RESETWIDTH}$	Reset pulse width	5	–	–	µs	
BID#194[5]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	3	ms	

Analog Peripherals

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID330[5]	I_{CMP1}	Block current, High Bandwidth mode	–	–	110	µA	
SID331[5]	I_{CMP2}	Block current, Low Power mode	–	–	85	µA	
SID332[5]	$V_{OFFSET1}$	Offset voltage, High Bandwidth mode	–	10	30	mV	
SID333[5]	$V_{OFFSET2}$	Offset voltage, Low Power mode	–	10	30	mV	
SID334[5]	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	
SID338[5]	VINP_COMP	Comparator input range	0	–	3.6	V	Max input voltage is lower of 3.6 V or V_{DD}

Table 10. Comparator AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID336[5]	T_{COMP1}	Response Time High Bandwidth mode, 50-mV overdrive	–	–	90	ns	
SID337[5]	T_{COMP2}	Response Time Low Power mode, 50-mV overdrive	–	–	110	ns	

Note
5. Guaranteed by characterization.

CSD

Table 11. CSD and IDAC Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD and IDAC Specifications							
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	VDD > 2V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	VDD > 1.75V (with ripple), 25 C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD#15	VREF	Voltage reference for CSD and Comparator	1.1	1.2	1.3	V	
SID.CSD#16	IDAC1IDD	IDAC1 (8-bits) block current	–	–	1125	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1125	µA	
SID308	V_{CSD}	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.8	–	V_{DD} –0.8	V	
SID309	$IDAC1_{DNL}$	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	$IDAC1_{INL}$	INL for 8-bit resolution	–3	–	3	LSB	
SID311	$IDAC2_{DNL}$	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	$IDAC2_{INL}$	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	$IDAC1_{CRT1}$	Output current of IDAC1 (8 bits) in high range	–	612	–	µA	
SID314A	$IDAC1_{CRT2}$	Output current of IDAC1(8 bits) in low range	–	306	–	µA	
SID315	$IDAC2_{CRT1}$	Output current of IDAC2 (7 bits) in high range	–	304.8	–	µA	
SID315A	$IDAC2_{CRT2}$	Output current of IDAC2 (7 bits) in low range	–	152.4	–	µA	
SID320	$IDAC_{OFFSET}$	All zeroes input	–	–	±1	LSB	
SID321	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±10	%	
SID322	$IDAC_{MISMATCH}$	Mismatch between IDACs	–	–	7	LSB	
SID323	$IDAC_{SET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$IDAC_{SET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 12. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 8 MHz	–	–	145	µA	All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 16 MHz	–	–	160	µA	All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 16 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[6]
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I^2C

Table 13. Fixed I^2C DC Specifications[7]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	25	µA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	
SID.PWR#5	ISBI2C	I^2C enabled in Deep Sleep mode	–	–	2.5	µA	

Table 14. Fixed I^2C AC Specifications[7]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	400	Kbps	

Notes
6. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
7. Guaranteed by characterization.

Memory

Table 15. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 16. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[8]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[8]	Row erase time	–	–	13	ms	
SID176	$T_{ROWPROGRAM}$[8]	Row program time after erase	–	–	7	ms	
SID178	$T_{BULKERASE}$[8]	Bulk erase time (16 KB)	–	–	15	ms	
SID180[9]	$T_{DEVPROG}$[8]	Total device program time	–	–	7.5	seconds	
SID181[9]	F_{END}	Flash endurance	100 K	–	–	cycles	
SID182[9]	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	
SID182A[9]		Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	

System Resources

Power-on Reset (POR)

Table 17. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185[9]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	
SID186[9]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4	V	

Table 18. Brown-out Detect (BOD) for VCCD

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190[9]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	
SID192[9]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5	V	

Notes
8. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
9. Guaranteed by characterization.

SWD Interface

Table 19. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215[10]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	
SID216[10]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	
SID217[10]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	
SID217A[10]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	

Internal Main Oscillator

Table 20. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	

Table 21. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±2	%	2 V ≤ VDD ≤ 5.5 V, and –25 °C ≤ TA ≤ 85 °C
SID223A	$F_{IMOTOLVCCD}$	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±4	%	All other conditions
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	

Internal Low-Speed Oscillator

Table 22. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231[10]	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	
SID233[10]	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	

Table 23. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234[10]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	
SID236[10]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	

Note
10. Guaranteed by characterization.

Table 24. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305[11]	ExtClkFreq	External clock input frequency	0	–	16	MHz	
SID306[11]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	

Table 25. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262[11]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	

Note
11. Guaranteed by characterization.

Ordering Information

The CY8CMBR31x5 part numbers and features are listed in the following table.

MPN	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Water Tolerance	Proximity Detection	Glove Touch	Stylus Support
CY8CMBR3145-LQXI	16-pin QFN	8K	1K	8	Yes	No	No	No
CY8CMBR3145-LQXIT	16-pin QFN (Tape and Reel)	8K	1K	8	Yes	No	No	No
CY8CMBR3155-LQXIT	16-pin QFN	8K	1K	8	Yes	Yes	Yes	No
CY8CMBR3155-LQXIT	16-pin QFN (Tape and Reel)	8K	1K	8	Yes	Yes	Yes	No
CY8CMBR3175-LQXI	16-pin QFN	8K	1K	8	Yes	Yes	Yes	Yes
CY8CMBR3175-LQXIT	16-pin QFN (Tape and Reel)	8K	1K	8	Yes	Yes	Yes	Yes

Packaging

Table 26. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25.00	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (16-pin QFN)		–	49.6	–	°C/Watt

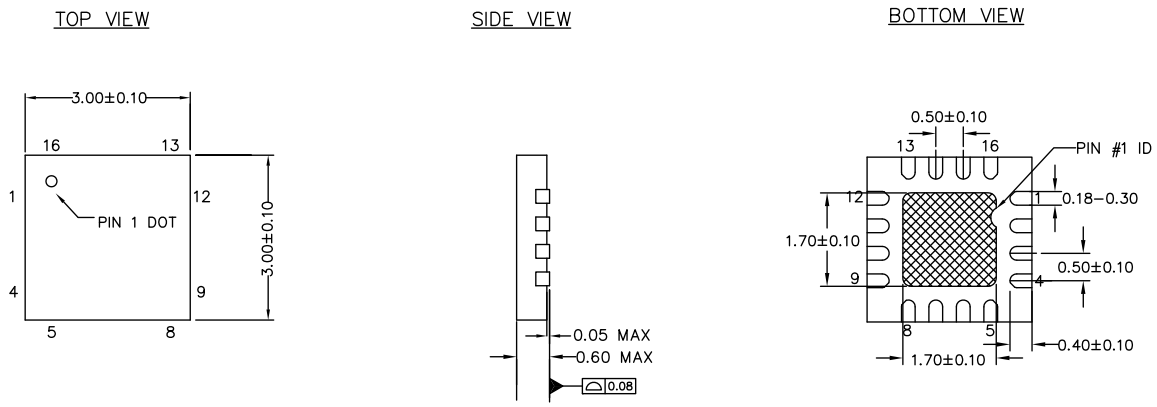
Table 27. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

Table 28. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

Figure 3. 16-pin (210-mil) QFN Package Outline



NOTES

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO–248
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web

001-87187 **

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Acronyms

Table 29. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 29. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 29. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 29. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 30. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: CY8CMBR3145,CY8CMBR3155, CY8CMBR3175 Datasheet CapSense® Controller with SmartSense™ Auto-Tuning, 8 Buttons for Mobile Solutions Document Number: 001-90144				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4199359	WKA	11/27/2013	New datasheet
*A	4283569	WKA	02/26/2014	Added note stating Low Power 1.71V to 5.5V operation in Features. Updated IMO tolerance setting in IMO Clock Source. Changed ILO oscillator from 32 kHz to 40 kHz in ILO Clock Source. Updated Low-power Comparators section. Changed internally regulated voltage range from 2.0 to 5.5 V to 1.8 to 5.5 V. Corrected max value of BID46 to 140. Updated the description for SID255. Added SID35 in DC Specifications. Added BID194 in XRES AC Specifications. Added SID338 in Comparator DC Specifications. Added specs for max allowed ripple on power supply in CSD and IDAC Block Specifications. Added SID.CSD15, SID.CSD16, and SID.CSD17 in CSD and IDAC Block Specifications. Modified description and conditions for SID223 and SID223A. Modified description for SID231. Updated SID237 description and values. Updated SID262 description and removed SID256 from Block Specs.
*B	4348760	WKA	05/06/2014	Removed reference to single-cycle SRAM access using the flash accelerator. Added note to clarify that low-power comparator is also used for CapSense operation in Low-power Comparators. Electrical Specifications: Added max I_{DD} data in Active mode for CPU running at 6, 12, and 16 MHz. Added max I_{DD} data in Deep Sleep mode for 1.8 to 3.6 V, 3.6 to 5.5 V, and 1.71 to 1.89 V. Added max I_{DD} data for Comparator block current in High Bandwidth and Low Power modes. Changed Comparator response time in both modes to match characterization data. Unified data table for Timer-Counter-Pulse-Width-Modulator (TCPWM) block for common specs. Added Block current consumption at 3, 8, and 16 MHz from characterization. Added spec for Quadrature input resolution and list of trigger events. Changed I^2C Block current at 100 kHz to match characterization data. Added Deep Sleep mode current consumption. Added Flash bulk erase time and total device program time specifications. Added power supply slew rate specification. Changed minimum POR and BOD falling trip voltage spec and added BOD max trip voltage. Changed IMO operating current at 48 MHz and 24 MHz to match character-ization data. Added clarifying note in IMO frequency variation to state valid frequency settings and added IMO start-up time spec. Corrected typo in Units for Comparator offset voltage in Low Power mode; changed from V (Volts) to mV (millivolts). Removed T_{JC} row from Package Characteristics. Changed datasheet status to Final.

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