Low Power JFET-Input Op Amps

ADA4062-2/ADA4062-4

FEATURES

- **Low input bias current: 50 pA maximum**
- **Offset voltage**
  - **1.5 mV maximum for B grade (ADA4062-2 SOIC package)**
  - **2.5 mV maximum for A grade**
- **Offset voltage drift: 5 µV/°C typical**
- **Slew rate: 3.3 V/µs typical**
- **CMRR: 90 dB typical**
- **Low supply current: 165 µA typical**
- **High input impedance**
- **Unity-gain stable**
- **±5 V to ±15 V dual-supply operation**
- **Packaging**
  - **8-lead SOIC, 8-lead MSOP, 10-lead LFCSP, 14-lead TSSOP, and 16-lead LFCSP packages**

APPLICATIONS

- **Power controls and monitoring**
- **Active filters**
- **Industrial/process controls**
- **Body probe electronics**
- **Data acquisition**
- **Integrators**
- **Input buffering**

GENERAL DESCRIPTION

The ADA4062-2 and ADA4062-4 are dual and quad JFET-input amplifiers with industry-leading performance. They offer lower power, offset voltage, drift, and ultralow bias current. The ADA4062-2 B grade (SOIC package) features a typical low offset voltage of 0.5 mV, an offset drift of 5 µV/°C, and a bias current of 2 pA.

The ADA4062 family is ideal for various applications, including process controls, industrial and instrumentation equipment, active filtering, data conversion, buffering, and power control and monitoring. With a low supply current of 165 µA per amplifier, they are well suited for lower power applications.

The ADA4062 family is also specified for the extended industrial temperature range of −40°C to +125°C. The ADA4062-2 is available in lead-free, 8-lead SOIC, 8-lead MSOP, and 10-lead LFCSP (1.6 mm × 1.3 mm × 0.55 mm) packages, while the ADA4062-4 is available in lead-free, 14-lead TSSOP and 16-lead LFCSP packages.

PIN CONFIGURATIONS

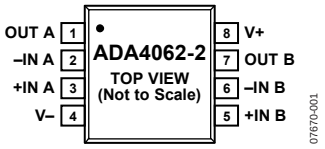

Figure 1. 8-Lead Narrow-Body SOIC and 8-Lead MSOP

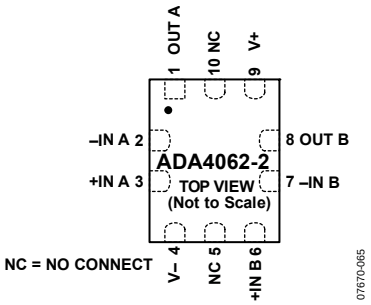

Figure 2. 10-Lead LFCSP

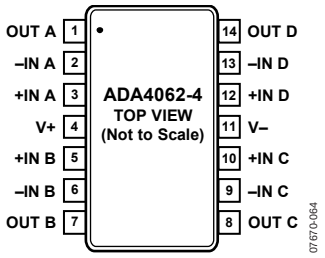

Figure 3. 14-Lead TSSOP

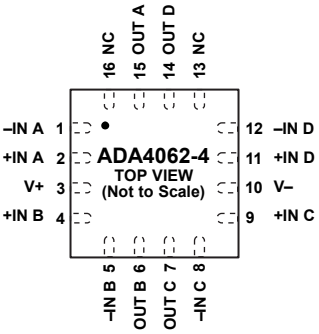

Figure 4. 16-Lead LFCSP

Table 1. Low Power Op Amps

	Precision CMOS	Precision High Bandwidth	High Bandwidth
Single	AD8663	AD8641	
Dual	AD8667	AD8642	AD8682
Quad	AD8669	AD8643	AD8684

Rev. B

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7/09—Rev. 0 to Rev. A

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10/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
B Grade (ADA4062-2, 8-Lead SOIC Only)				0.5	1.5	mV
		−40°C ≤ T_A ≤ +125°C			3	mV
A Grade				0.75	2.5	mV
		−40°C ≤ T_A ≤ +125°C			5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		5		µV/°C
Input Bias Current	I_B			2	50	pA
		−40°C ≤ T_A ≤ +125°C			5	nA
Input Offset Current	I_{OS}			0.5	25	pA
		−40°C ≤ T_A ≤ +125°C			2.5	nA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	−11.5		+15	V
Common-Mode Rejection Ratio	CMRR					
B Grade (ADA4062-2, 8-Lead SOIC Only)		V_{CM} = −11.5 V to +11.5 V	80	90		dB
		−40°C ≤ T_A ≤ +125°C	80			dB
A Grade		V_{CM} = −11.5 V to +11.5 V	73	90		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −10 V to +10 V	76	83		dB
		−40°C ≤ T_A ≤ +125°C	72			dB
Input Resistance	R_{IN}			10		TΩ
Input Capacitance, Differential Mode	C_{INDM}			1.5		pF
Input Capacitance, Common Mode	C_{INCM}			4.8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	13	13.5		V
		−40°C ≤ T_A ≤ +125°C	12.5			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−13.8	−13	V
		−40°C ≤ T_A ≤ +125°C			−12.5	V
Short-Circuit Current	I_{SC}			20		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR					
B Grade (ADA4062-2, 8-Lead SOIC Only)		V_{SY} = ±4 V to ±18 V	80	90		dB
		−40°C ≤ T_A ≤ +125°C	80			dB
A Grade		V_{SY} = ±4 V to ±18 V	74	90		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		165	220	µA
		−40°C ≤ T_A ≤ +125°C			260	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = 1		3.3		V/µs
Settling Time	t_S	To 0.1%, V_{IN} = 10 V step, C_L = 100 pF, R_L = 10 kΩ, A_V = 1		3.5		µs
Gain Bandwidth Product	GBP	R_L = 10 kΩ, A_V = 1		1.4		MHz
Phase Margin	Φ_M	R_L = 10 kΩ, A_V = 1		78		Degrees
Channel Separation (ADA4062-2 Only)	CS	f = 1 kHz		135		dB
Channel Separation (ADA4062-4 Only)	CS	f = 1 kHz		130		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		5		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$\pm V_{SY}$
Differential Input Voltage	$\pm V_{SY}$
Input Current	±10 mA
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. It was measured using a standard 4-layer board.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	120	45	°C/W
8-Lead MSOP	142	45	°C/W
10-Lead LFCSP	132	46	°C/W
14-Lead TSSOP	112	35	°C/W
16-Lead LFCSP	75	12	°C/W

POWER SEQUENCING

The supply voltages of the op amps must be established simultaneously with, or before, any input signals are applied. If this is not possible, the input current must be limited to 10 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

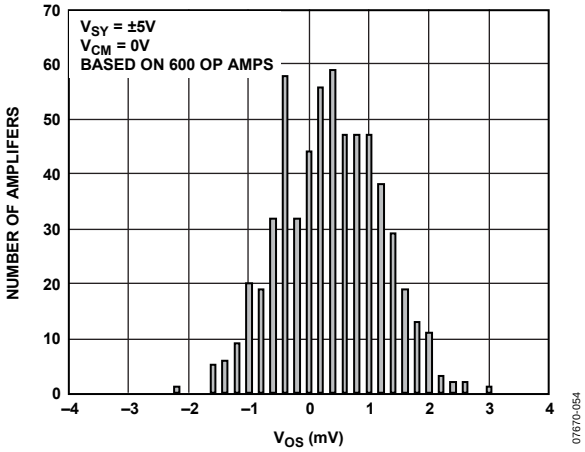


Figure 5. Input Offset Voltage Distribution

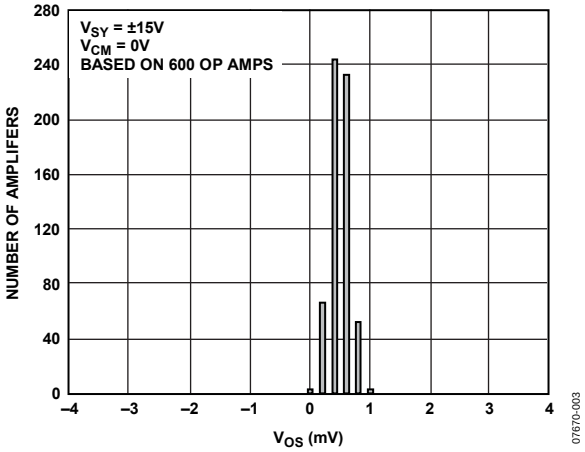


Figure 8. Input Offset Voltage Distribution

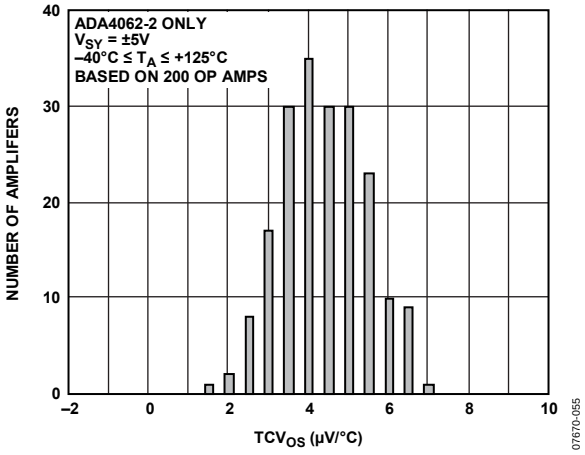
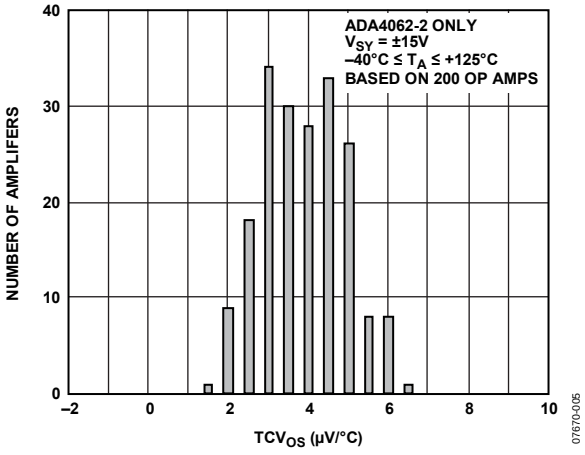


Figure 6. Input Offset Voltage Drift Distribution



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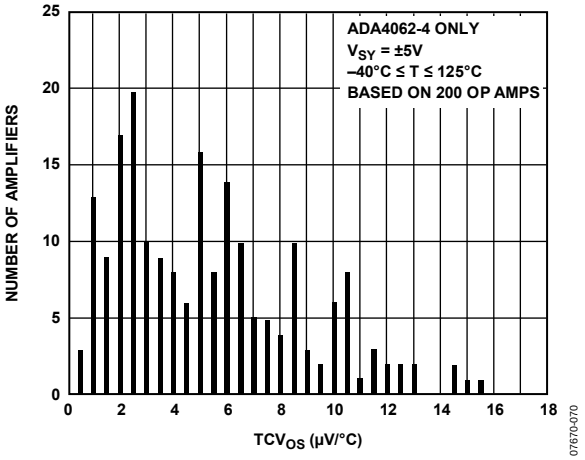
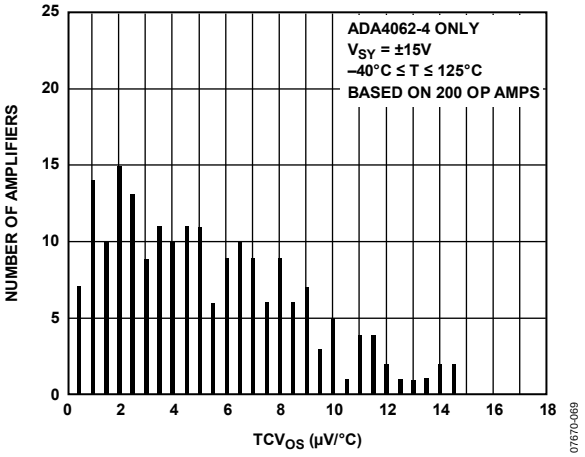


Figure 7. Input Offset Voltage Drift Distribution



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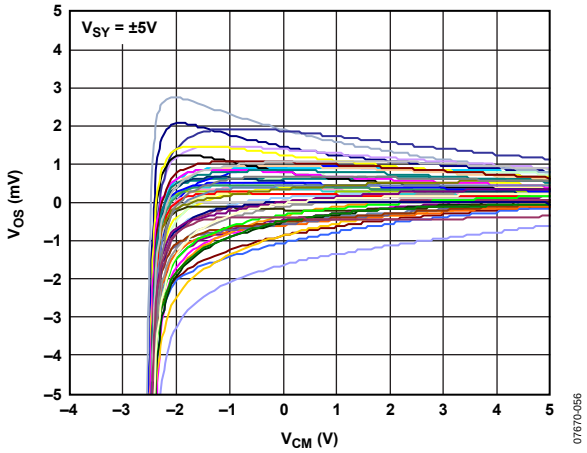

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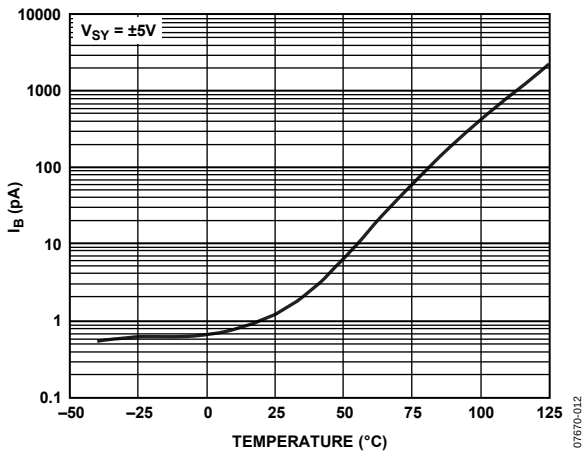

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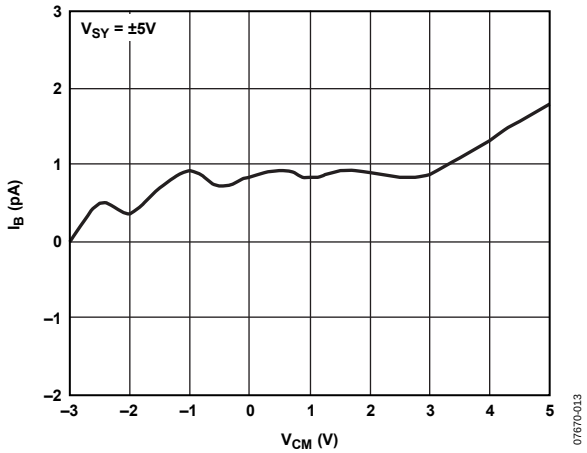

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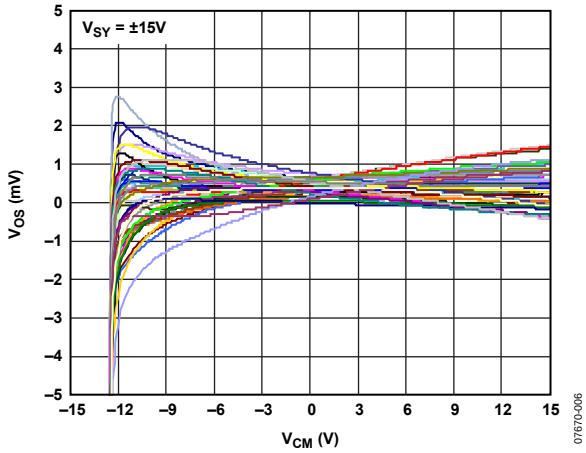

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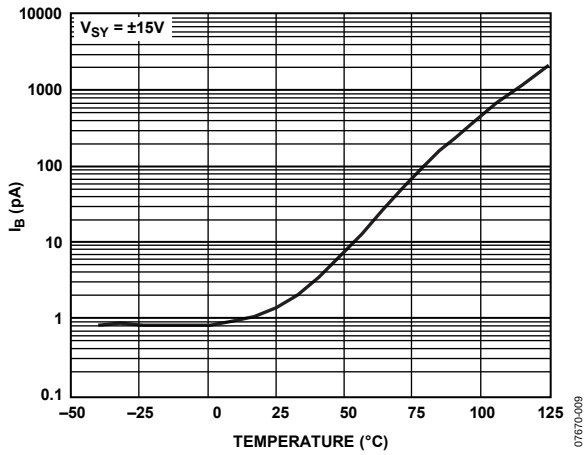

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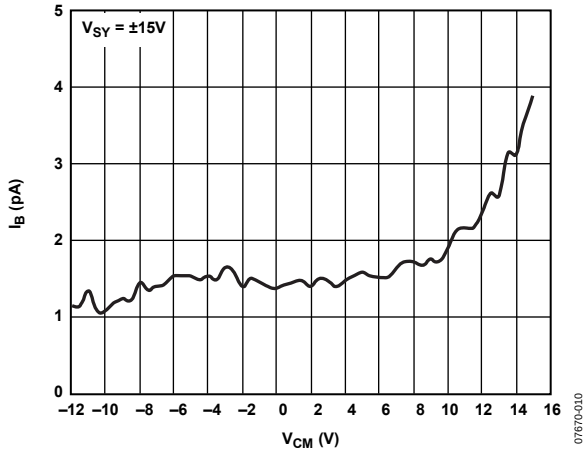

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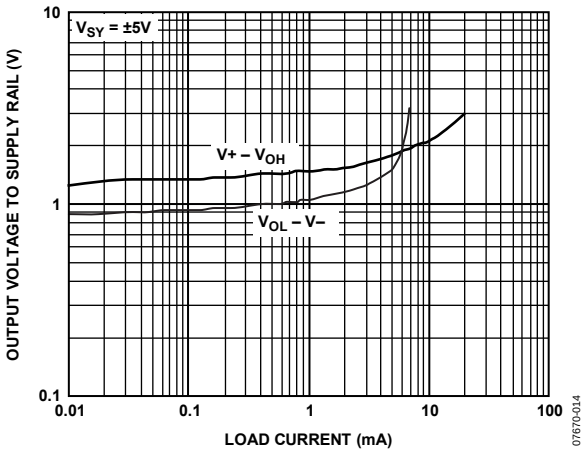

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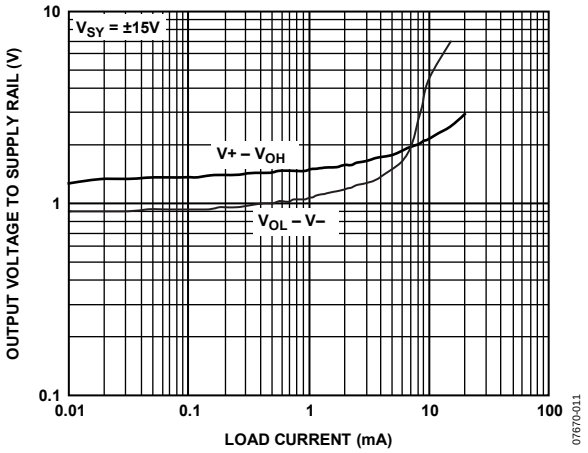

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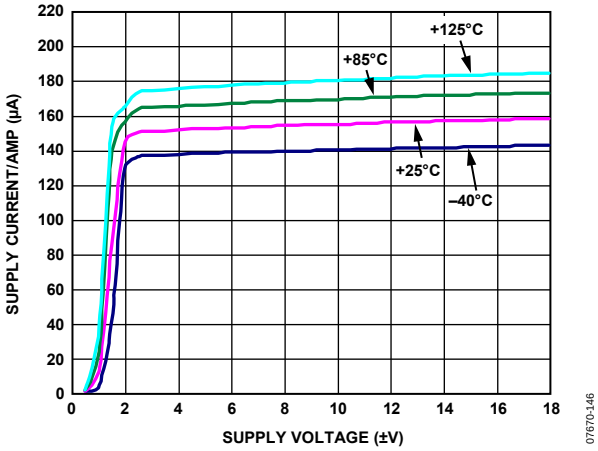

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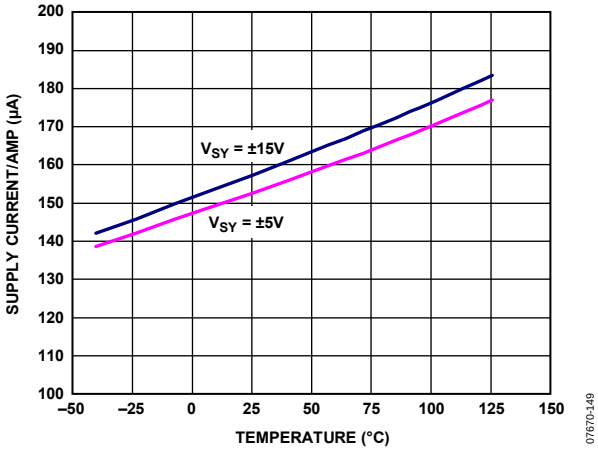

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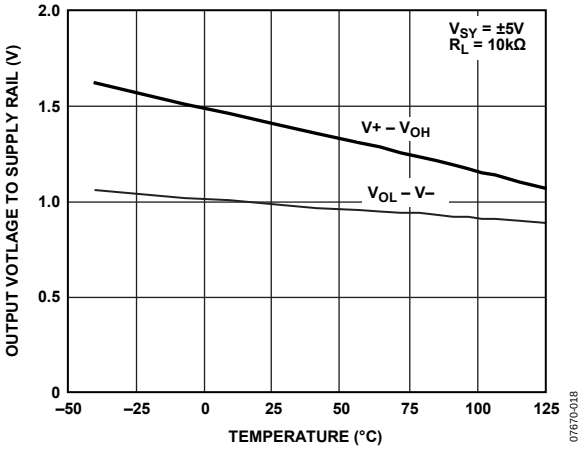

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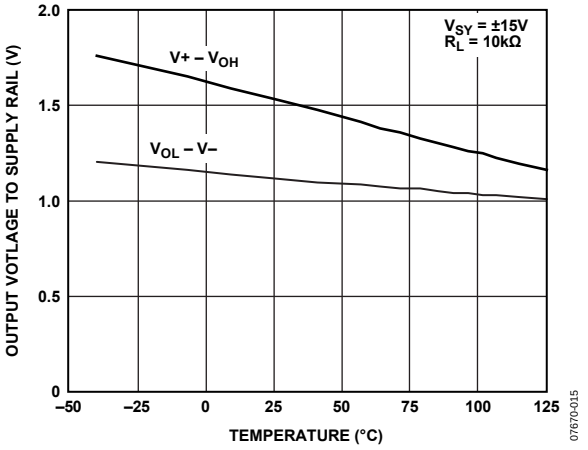


Figure 22. Output Voltage to Supply Rail vs. Temperature

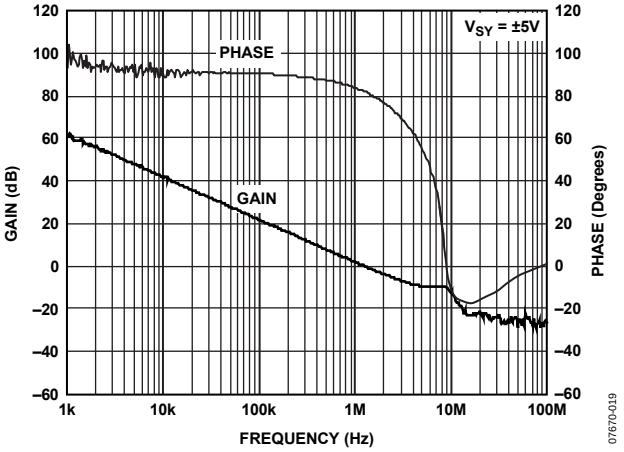
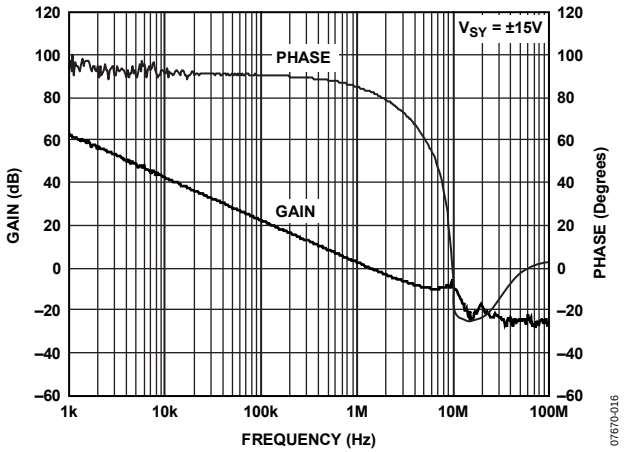


Figure 23. Open-Loop Gain and Phase vs. Frequency



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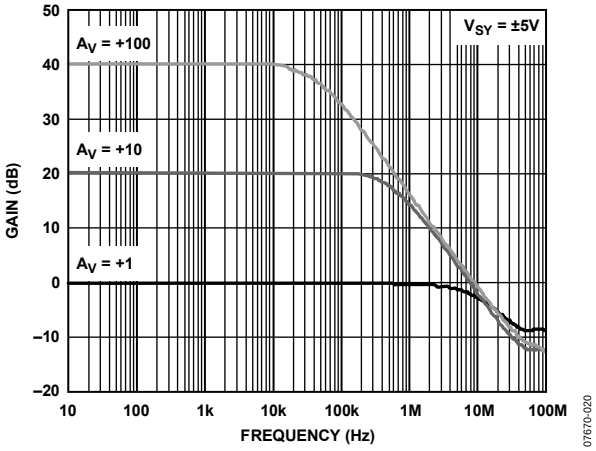

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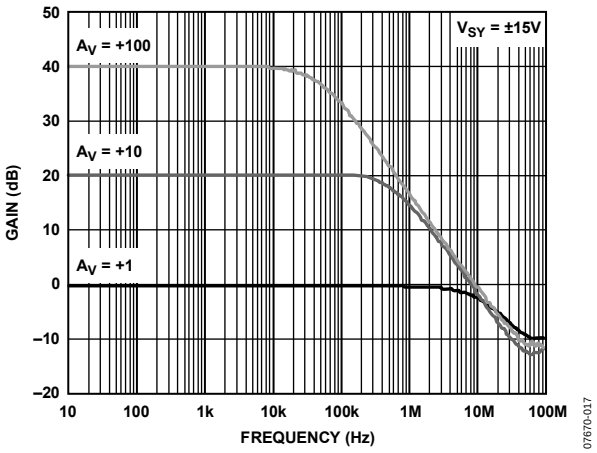

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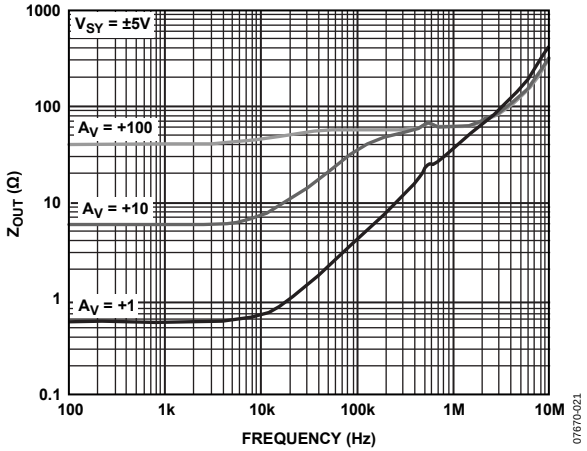

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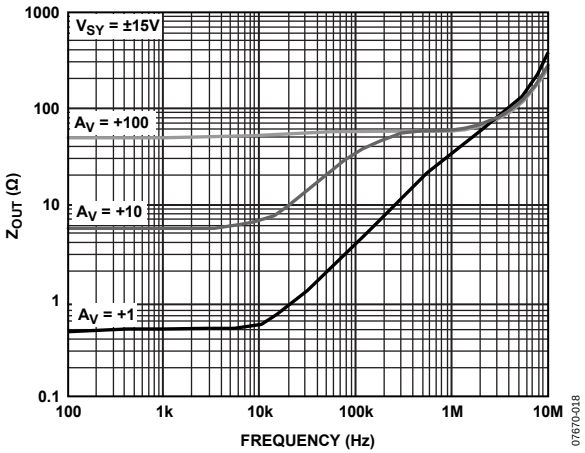

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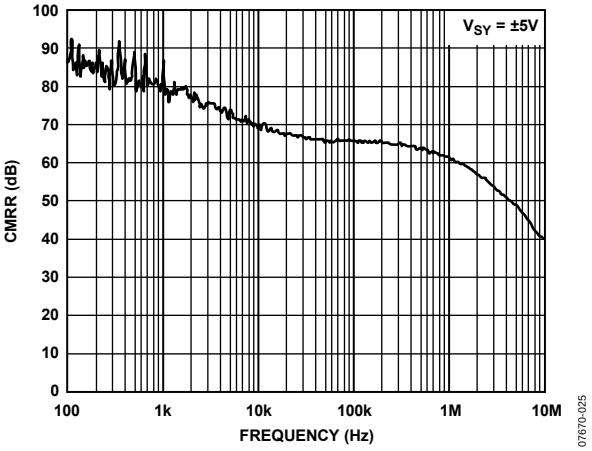


Figure 29. CMRR vs. Frequency

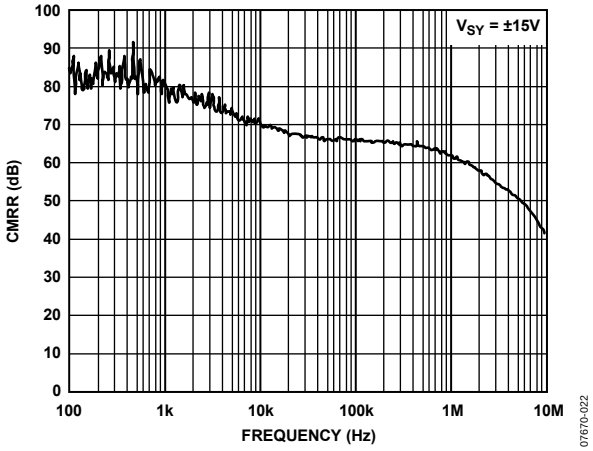
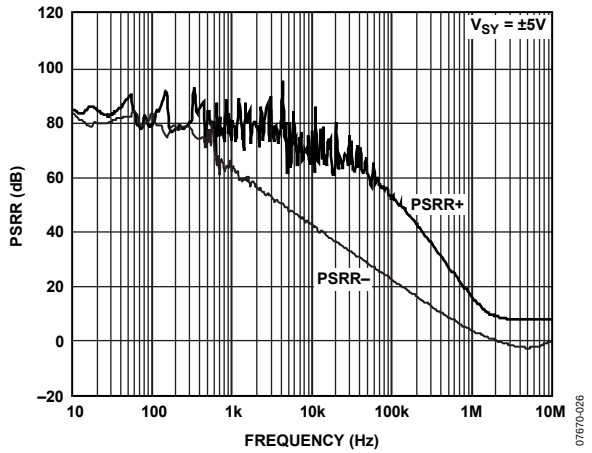


Figure 32. CMRR vs. Frequency



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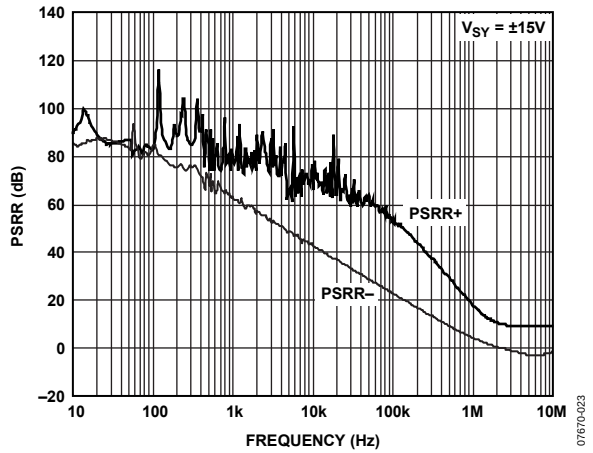

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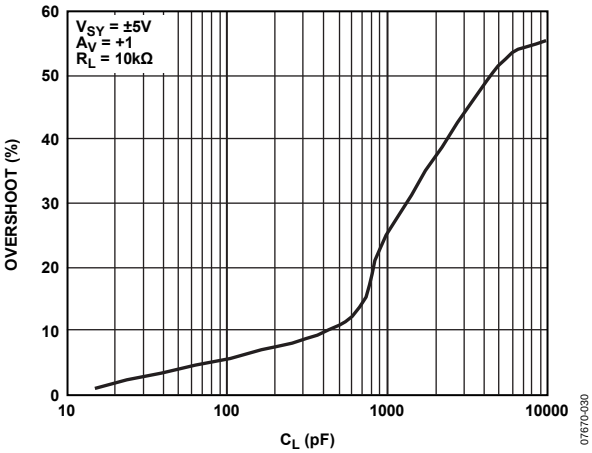


Figure 31. Small-Signal Overshoot vs. Load Capacitance

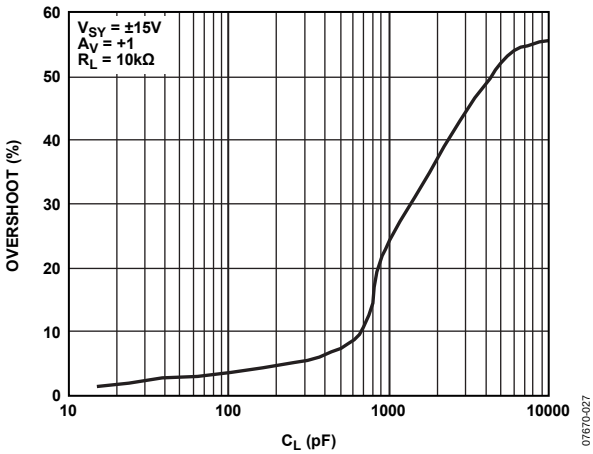


Figure 34. Small-Signal Overshoot vs. Load Capacitance

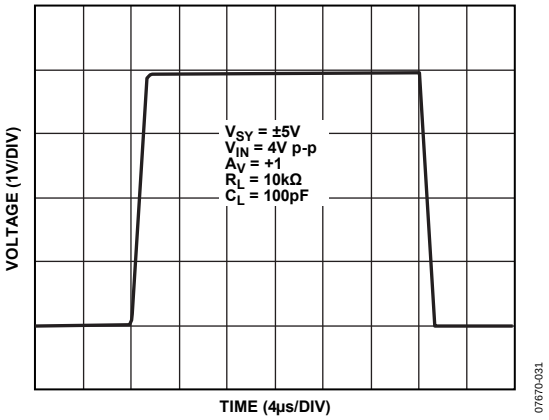


Figure 35. Large-Signal Transient Response

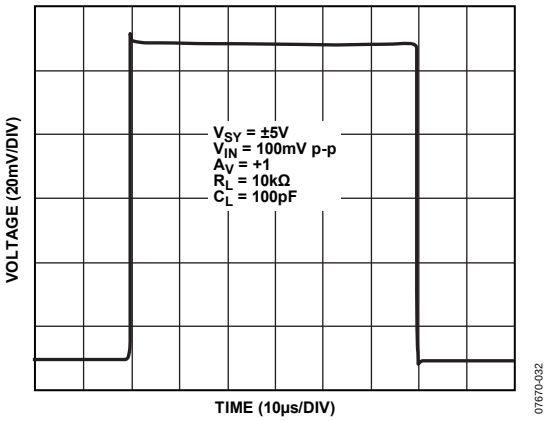


Figure 36. Small-Signal Transient Response

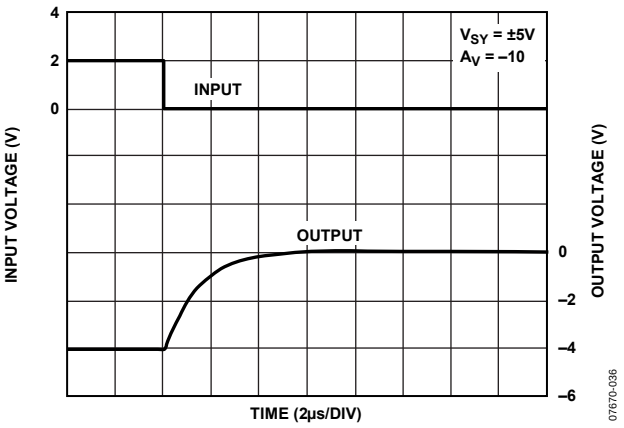


Figure 37. Negative Overload Recovery

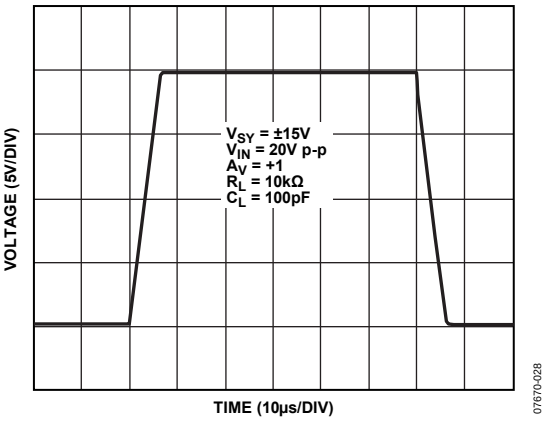


Figure 38. Large-Signal Transient Response

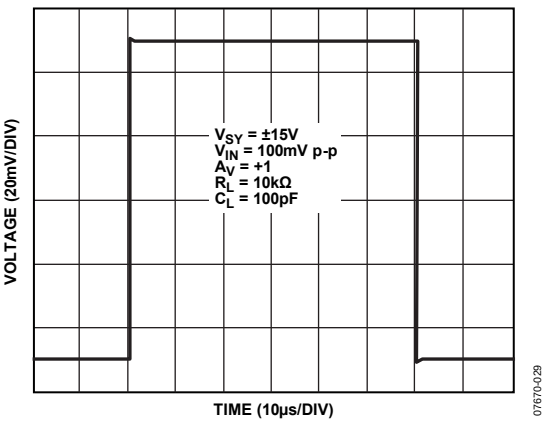


Figure 39. Small-Signal Transient Response

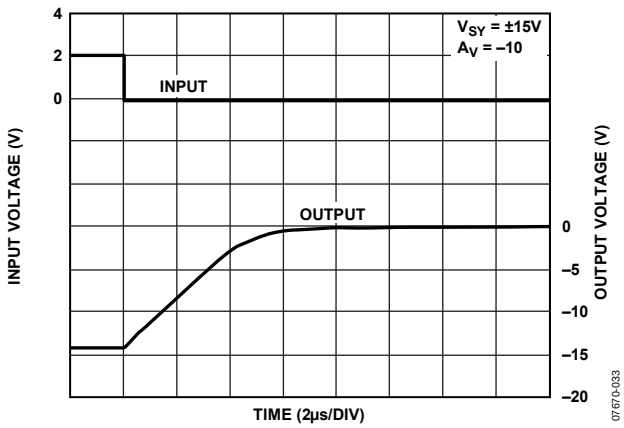


Figure 40. Negative Overload Recovery

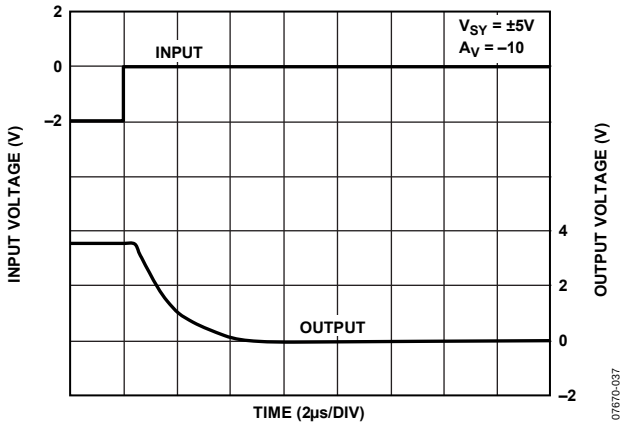


Figure 41. Positive Overload Recovery

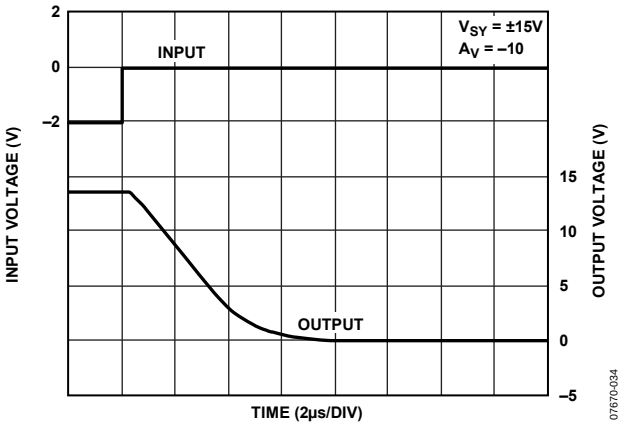


Figure 44. Positive Overload Recovery

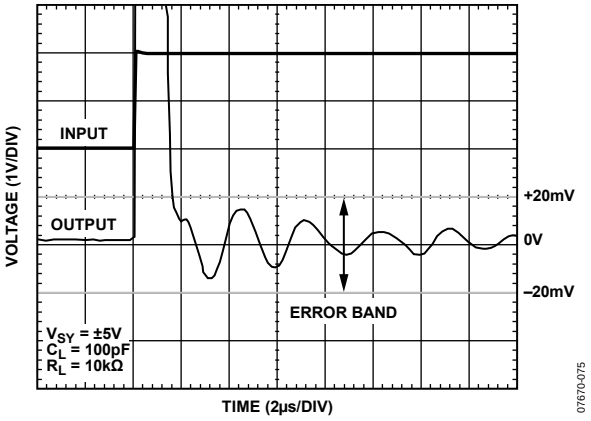


Figure 42. Positive Settling Time to 0.1%

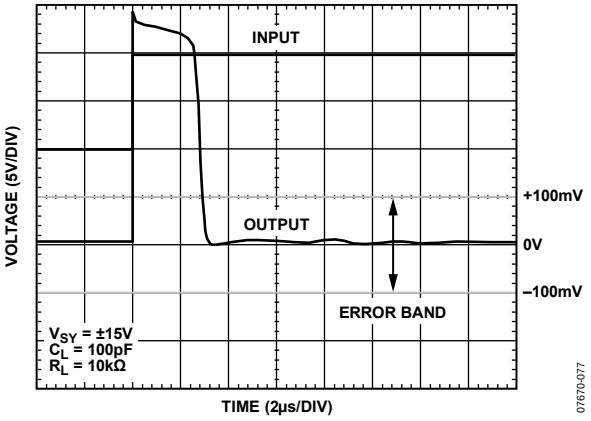


Figure 45. Positive Settling Time to 0.1%

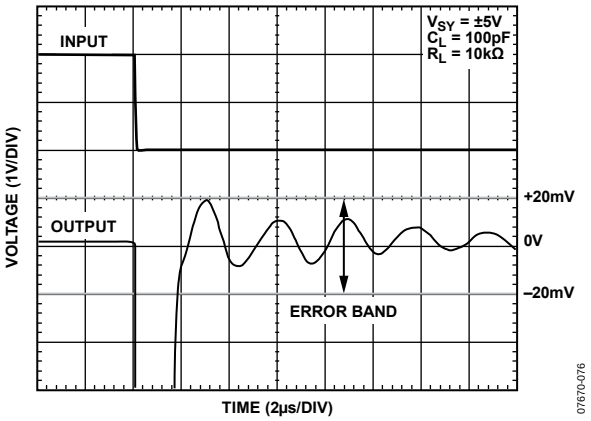


Figure 43. Negative Settling Time to 0.1%

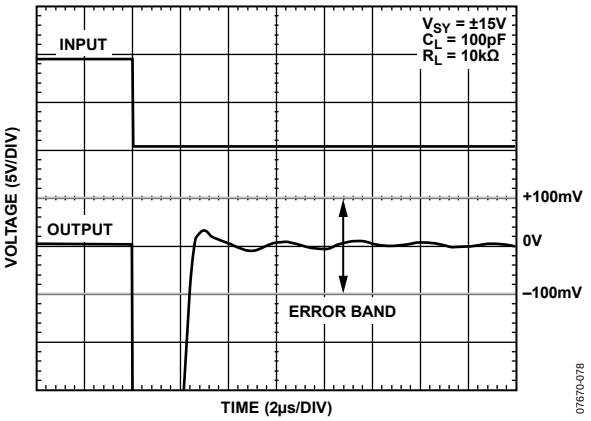


Figure 46. Negative Settling Time to 0.1%

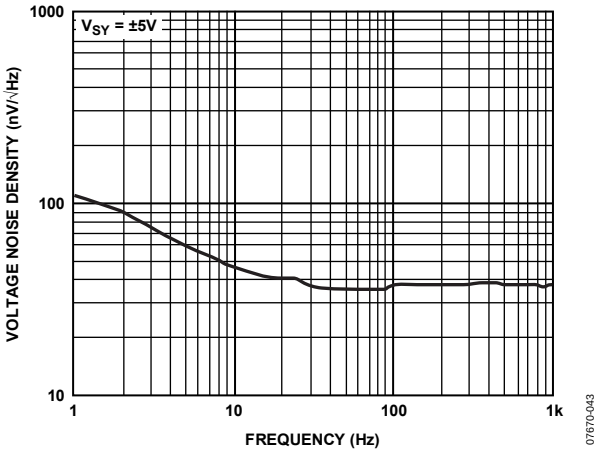


Figure 47. Voltage Noise Density

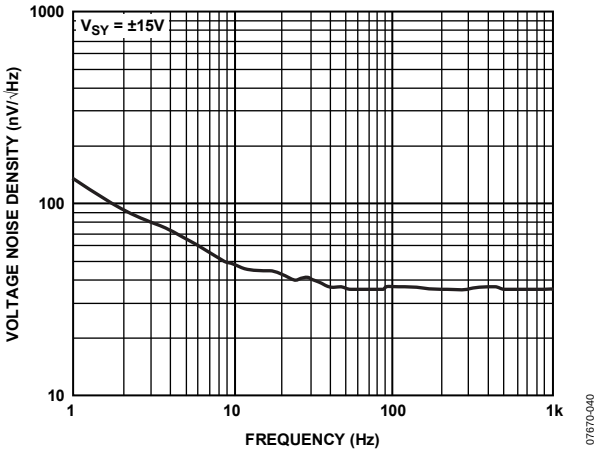


Figure 50. Voltage Noise Density

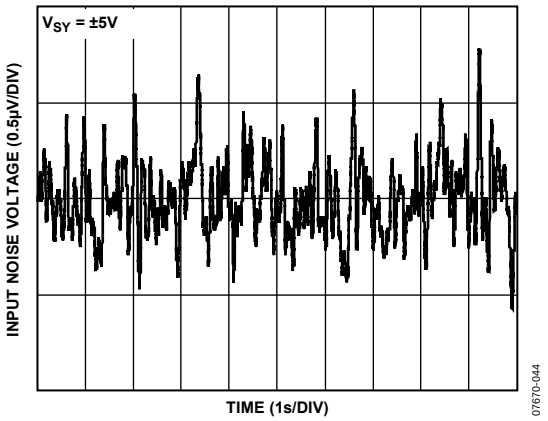


Figure 48. 0.1 Hz to 10 Hz Noise

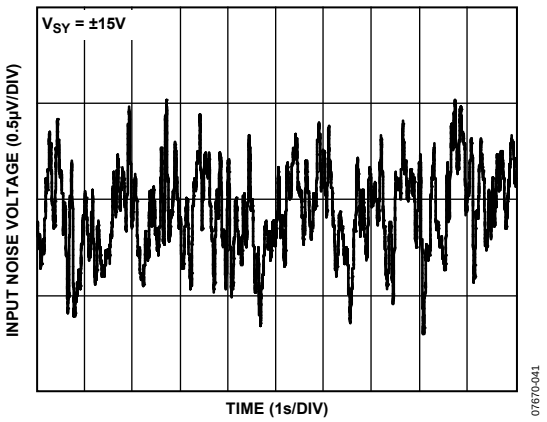


Figure 51. 0.1 Hz to 10 Hz Noise

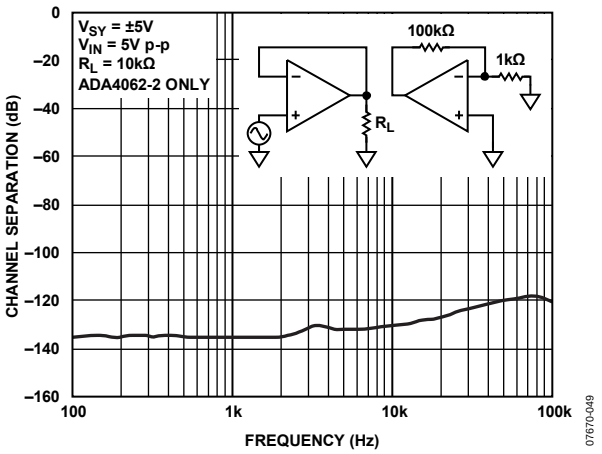


Figure 49. Channel Separation vs. Frequency (ADA4062-2 Only)

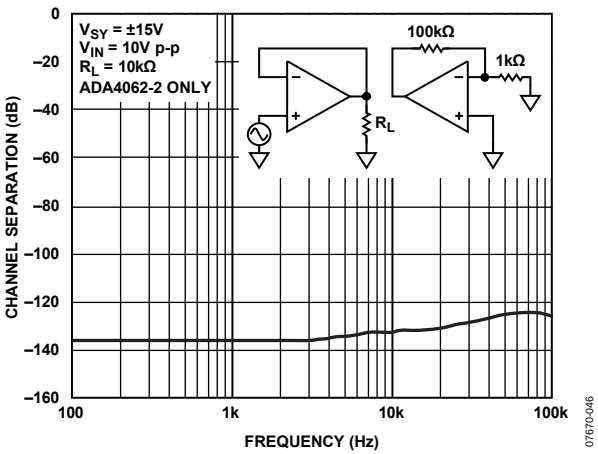


Figure 52. Channel Separation vs. Frequency (ADA4062-2 Only)

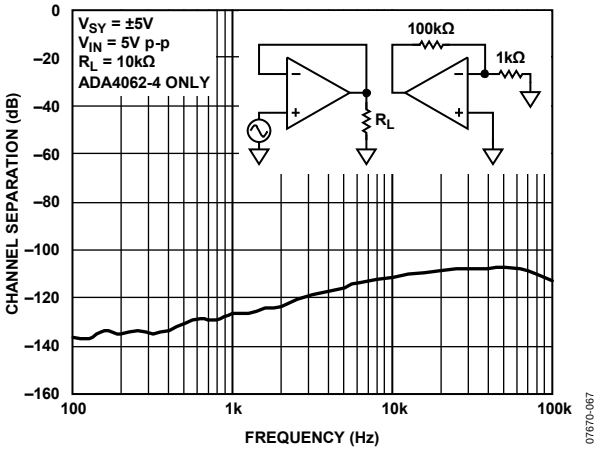


Figure 53. Channel Separation vs. Frequency (ADA4062-4 Only)

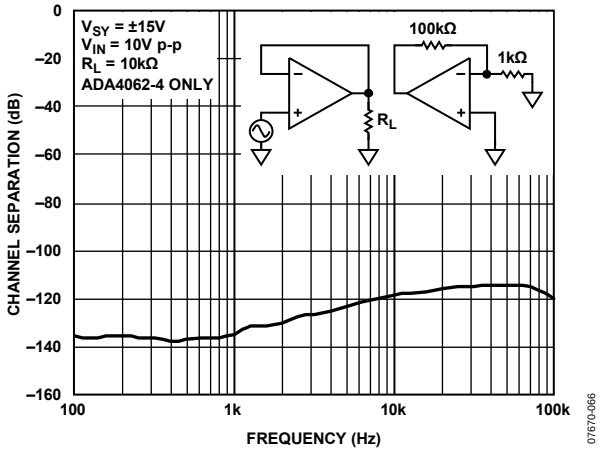


Figure 56. Channel Separation vs. Frequency (ADA4062-4 Only)

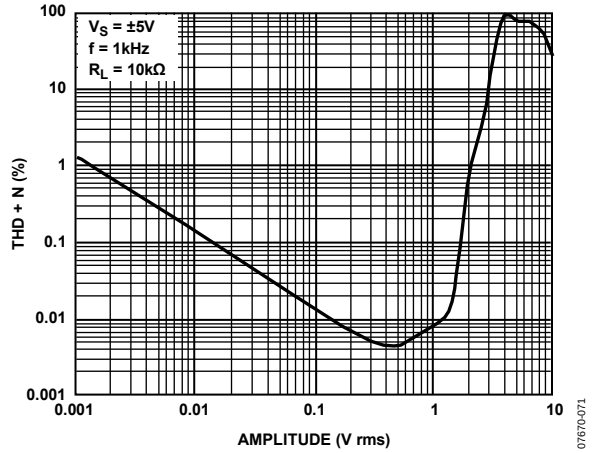


Figure 54. THD + N vs. Amplitude

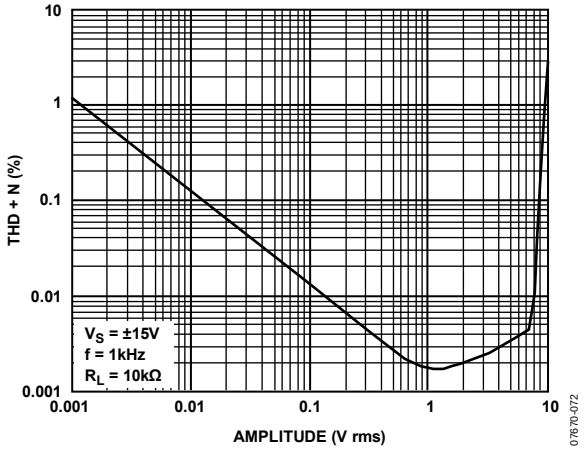


Figure 57 THD + N vs. Amplitude

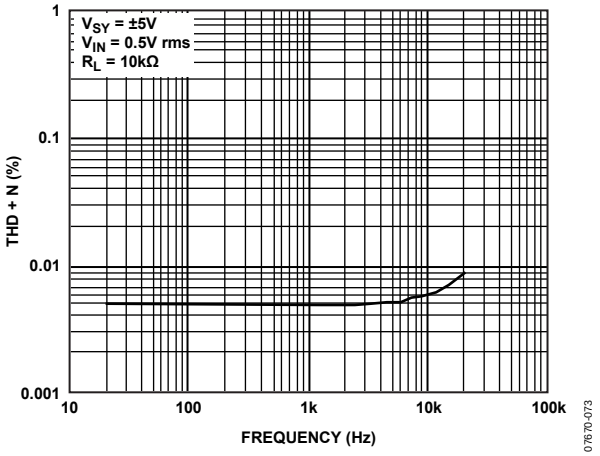


Figure 55. THD + N vs. Frequency

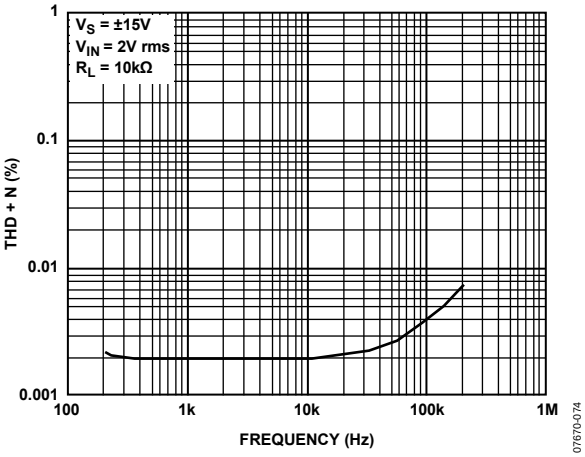


Figure 58. THD + N vs. Frequency

APPLICATIONS INFORMATION

NOTCH FILTER

A notch filter rejects a specific interfering frequency and can be implemented using a single op amp. Figure 59 shows a 60 Hz notch filter that uses the twin-T network with the ADA4062-x configured as a voltage follower. The ADA4062-x works as a buffer that provides high input resistance and low output impedance. The low bias current (2 pA typical) and high input resistance (10 TΩ typical) of the ADA4062-x enable large resistors and small capacitors to be used.

Alternatively, different combinations of resistor and capacitor values can be used to achieve the desired notch frequency. However, the major drawback to this circuit topology is the need to ensure that all the resistors and capacitors be closely matched. If they are not closely matched, the notch frequency offset and drift cause the circuit to attenuate at a frequency other than the ideal notch frequency.

Therefore, to achieve the desired performance, 1% or better component tolerances are usually required. In addition, a notch filter requires an op amp with a bandwidth of at least 100× to 200× the center frequency. Hence, using the ADA4062-x with a bandwidth of 1.4 MHz is excellent for a 60 Hz notch filter. Figure 60 shows the frequency response of the notch filter. At 60 Hz, the notch filter has about 50 dB attenuation of signal.

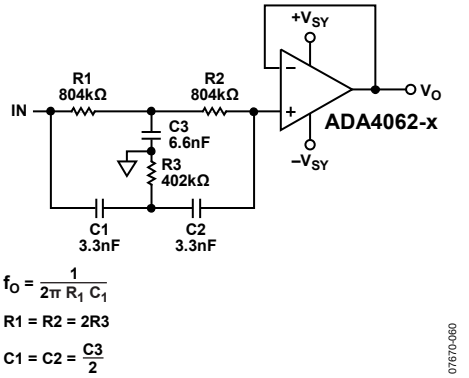


Figure 59. Notch Filter Circuit

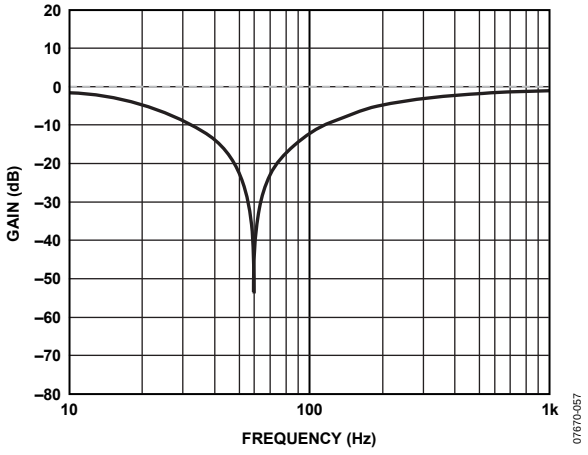


Figure 60. Frequency Response of the Notch Filter

HIGH-SIDE SIGNAL CONDITIONING

Many applications require the sensing of signals near the positive rail. The ADA4062-x can be used in high-side current sensing applications. Figure 61 shows a high-side signal conditioning circuit using the ADA4062-x. The ADA4062-x has an input common-mode range that includes the positive supply (−11.5 V ≤ V_{CM} ≤ +15 V). In the circuit, the voltage drop across a low value resistor, such as the 0.1 Ω shown in Figure 61, is amplified by a factor of 5 using the ADA4062-x.

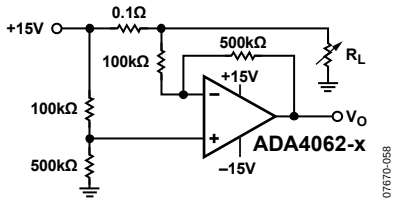


Figure 61. High-Side Signal Conditioning

MICROPOWER INSTRUMENTATION AMPLIFIER

The ADA4062-2 is a dual amplifier and is perfectly suited for applications that require lower supply currents. For supply voltages of ±15 V, the supply current per amplifier is 165 μA typical. The ADA4062-2 also offers a typical low offset voltage drift of 5 μV/°C and a very low bias current of 2 pA, which make it well suited for instrumentation amplifiers.

Figure 62 shows the classic 2-op-amp instrumentation amplifier with four resistors using the ADA4062-2. The key to high CMRR for this instrumentation amplifier are resistors that are well matched to both the resistive ratio and relative drift. For true difference amplification, matching of the resistor ratio is very important, where R3/R4 = R1/R2. Assuming perfectly matched resistors, the gain of the circuit is 1 + R2/R1, which is approximately 100. Tighter matching of two op amps in one package, as is the case with the ADA4062-2, offers a significant boost in performance over the classical 3-op-amp configuration. Overall, the circuit only requires about 330 μA of supply current.

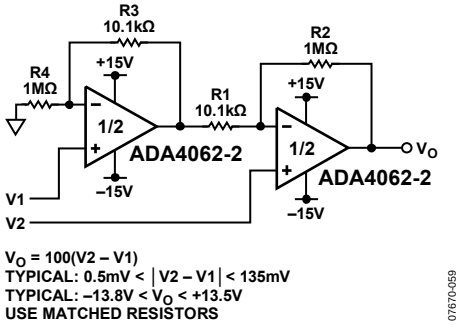


Figure 62. Micropower Instrumentation Amplifier

PHASE REVERSAL

Phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. When the voltage driving the input to these amplifiers exceeds the maximum input common-mode voltage range, the output of the amplifiers changes polarity. Most JFET input amplifiers have phase reversal if either input exceeds the input common-mode range.

For the ADA4062-x, the output does not phase reverse if one or both of the inputs exceeds the input voltage range but remains within the positive supply rail and 0.5 V above the negative supply rail. In other words, for an application with a supply voltage of ±15 V, the input voltage can be as high as +15 V without any output phase reversal. However, when the voltage of the inputs is driven beyond −14.5 V, phase reversal occurs due to saturation of the input stage leading to forward biasing of the gate-drain diode. Phase reversal in ADA4062-x can be prevented by using a Schottky diode to clamp the input terminals to each other. In the simple buffer circuit in Figure 63, D1 protects the op amp against phase reversal, and R limits the input current that flows into the op amp.

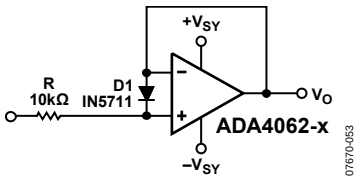


Figure 63. Phase Reversal Solution Circuit

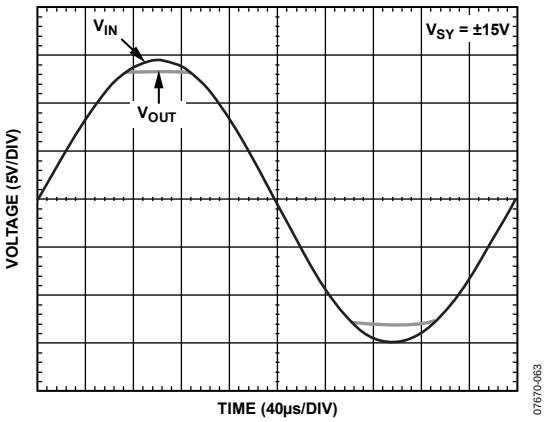


Figure 64. No Phase Reversal

SCHEMATIC

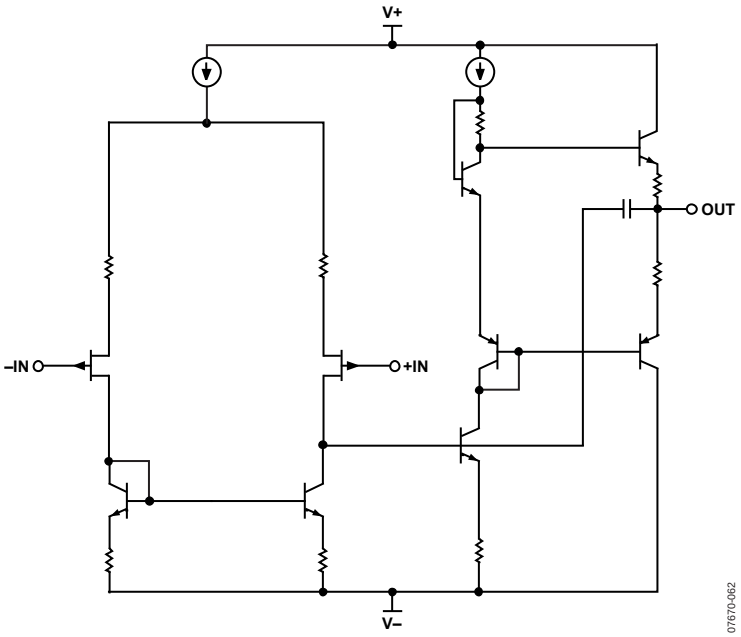
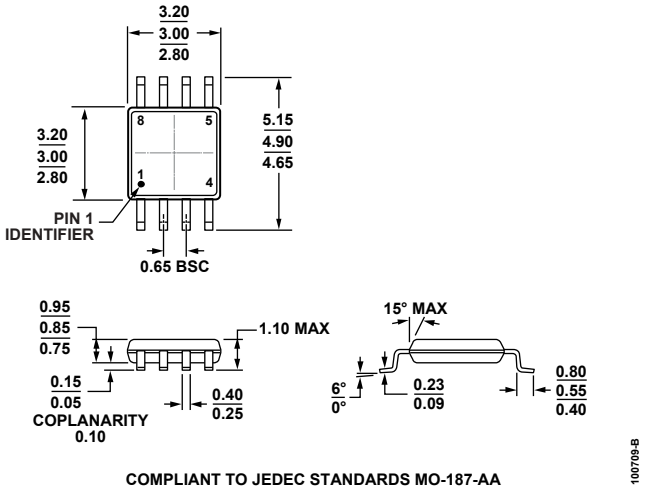


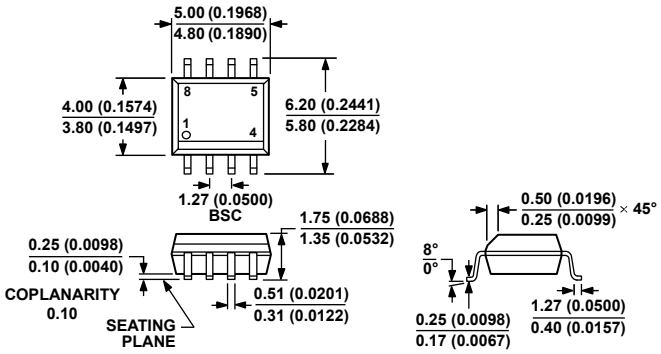
Figure 65. Simplified Schematic of the ADA4062-x

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 66. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 67. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

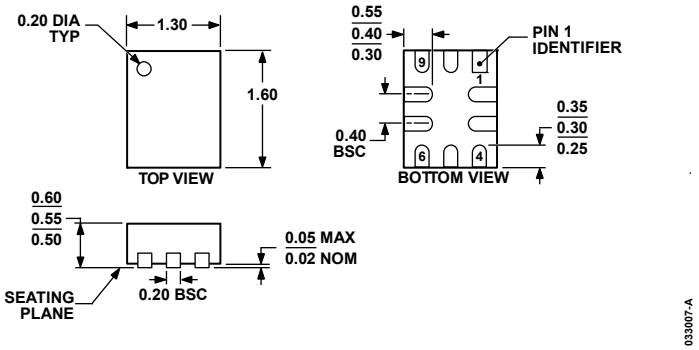
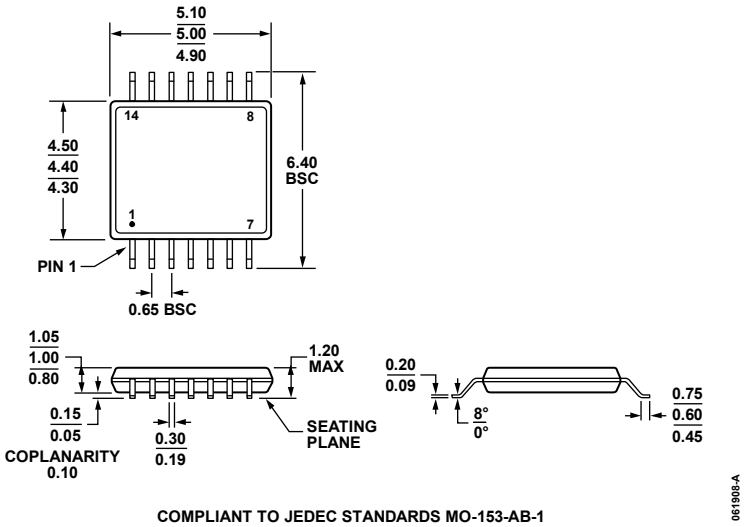
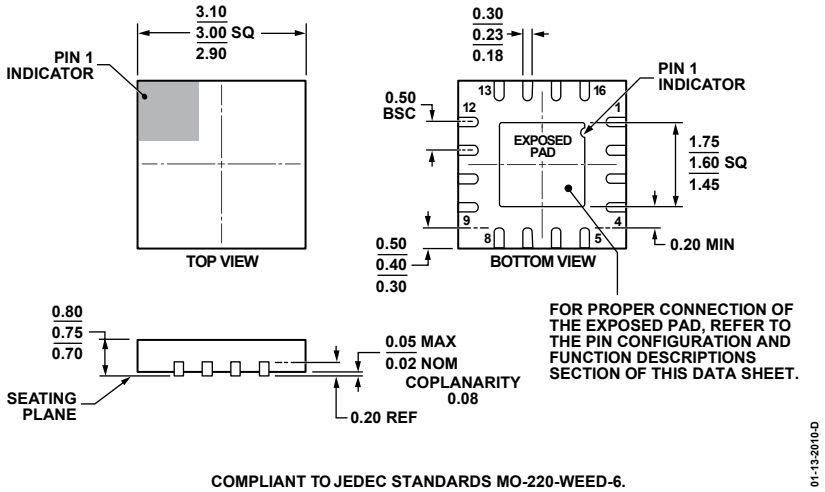


Figure 68. 10-Lead Lead Frame Chip Scale Package [LFCSP_UQ]
1.30 mm × 1.60 mm, Body, Ultra Thin Quad
(CP-10-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 69. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 70. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4062-2ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	A25
ADA4062-2ARMZ-RL	−40°C to +125°C	8-Lead MSOP	RM-8	A25
ADA4062-2ARMZ-RL7	−40°C to +125°C	8-Lead MSOP	RM-8	A25
ADA4062-2ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2BRZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2BRZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2BRZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2ACPZ-R2	−40°C to +125°C	10-Lead LFCSP_UQ	CP-10-10	J
ADA4062-2ACPZ-RL	−40°C to +125°C	10-Lead LFCSP_UQ	CP-10-10	J
ADA4062-2ACPZ-R7	−40°C to +125°C	10-Lead LFCSP_UQ	CP-10-10	J
ADA4062-4ARUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	
ADA4062-4ARUZ-RL	−40°C to +125°C	14-Lead TSSOP	RU-14	
ADA4062-4ACPZ-R2	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	A2K
ADA4062-4ACPZ-R7	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	A2K
ADA4062-4ACPZ-RL	−40°C to +125°C	16-Lead LFCSP_WQ	CP-16-22	A2K

[1] Z = RoHS Compliant Part.

D07670-0-2/10(B)