CMOS, ±5 V/+5 V, 4 Ω, Single SPDT Switch

ADG619-EP

FEATURES

- 14 Ω (maximum) on resistance
- 1.4 Ω (maximum) on-resistance flatness
- 2.7 V to 5.5 V single supply
- ±2.7 V to ±5.5 V dual supply
- Rail-to-rail operation
- 8-lead SOT-23
- Typical power consumption (<0.1 µW)
- TTL-/CMOS-compatible inputs
- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- One assembly and test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Automatic test equipment
- Power routing
- Communication systems
- Data acquisition systems
- Sample-and-hold systems
- Avionics
- Relay replacement
- Battery-powered systems

FUNCTIONAL BLOCK DIAGRAM

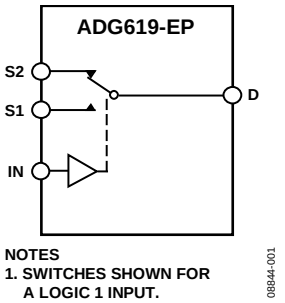

Figure 1.

GENERAL DESCRIPTION

The ADG619-EP is a monolithic, CMOS single-pole double-throw (SPDT) switch.

The ADG619-EP offers a low on resistance of 4 Ω, which is matched to within 0.7 Ω between channels. These switches also provide low power dissipation, yet result in high switching speeds. The ADG619-EP exhibits break-before-make switching action, thus preventing momentary shorting when switching channels.

The ADG619-EP is available in an 8-lead SOT-23 package.

Additional application and technical information can be found in the ADG619 data sheet.

PRODUCT HIGHLIGHTS

1. Low on resistance (R_{ON}): 4 Ω typical.
2. Dual ±2.7 V to ±5.5 V or single 2.7 V to 5.5 V supplies.
3. Low power dissipation.
4. Fast t_{ON}/t_{OFF}.
5. Tiny, 8-lead SOT-23 package.

Rev. 0

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REVISION HISTORY

11/10—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V. All specifications −55°C to +125°C, unless otherwise noted.

Table 1.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance (R_{ON})	4		Ω typ	V_S = ±4.5 V, I_{DS} = −10 mA; see Figure 9
	6.5	10	Ω max	
R_{ON} Match Between Channels (ΔR_{ON})	0.7		Ω typ	V_S = ±4.5 V, I_{DS} = −10 mA
	1.1	1.45	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	0.7		Ω typ	V_S = ±3.3 V, I_{DS} = −10 mA
	1.35	1.6	Ω max	
LEAKAGE CURRENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.01		nA typ	V_S = ±4.5 V, V_D = ∓ 4.5 V; see Figure 10
	±0.25	±3	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01		nA typ	V_S = V_D = ±4.5 V; see Figure 11
	±0.25	±25	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	80		ns typ	R_L = 300 Ω, C_L = 35 pF
	120	215	ns max	V_S = 3.3 V; see Figure 12
t_{OFF}	45		ns typ	R_L = 300 Ω, C_L = 35 pF
	75	105	ns max	V_S = 3.3 V; see Figure 12
Break-Before-Make Time Delay, t_{BBM}	40		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 3.3 V; see Figure 13
Charge Injection	110		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 14
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 15
Channel-to-Channel Crosstalk	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 16
Bandwidth −3 dB	190		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 17
C_S (Off)	25		pF typ	f = 1 MHz
C_D, C_S (On)	95		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	
I_{SS}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V. All specifications −55°C to +125°C, unless otherwise noted.

Table 2.

Parameter	+25°C	−55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance (R_{ON})	7		Ω typ	V_S = 0 V to 4.5 V, I_{DS} = −10 mA; see Figure 9
	10	14	Ω max	
R_{ON} Match Between Channels (ΔR_{ON})	0.8		Ω typ	V_S = 0 V to 4.5 V, I_{DS} = −10mA
	1.1	1.4	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	0.5		Ω typ	V_S = 1.5 V to 3.3 V, I_{DS} = −10 mA
		1.4	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source Off Leakage, I_S (Off)	±0.01		nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 10
	±0.25	±3	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01		nA typ	V_S = V_D = 1 V/4.5 V; see Figure 11
	±0.25	±25	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	120		ns typ	R_L = 300 Ω, C_L = 35 pF
	220	390	ns max	V_S = 3.3 V; see Figure 12
t_{OFF}	50		ns typ	R_L = 300 Ω, C_L = 35 pF
	75	135	ns max	V_S = 3.3 V; see Figure 12
Break-Before-Make Time Delay, t_{BBM}	70		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 3.3 V; see Figure 13
Charge Injection	6		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 14
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 15
Channel-to-Channel Crosstalk	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 16
Bandwidth −3 dB	190		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 17
C_S (OFF)	25		pF typ	f = 1 MHz
C_D, C_S (ON)	95		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	13 V
V_{DD} to GND	−0.3 V to +6.5 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	50 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal impedance	
θ_{JA}	229.6°C/W
θ_{JC}	91.99°C/W
Lead Soldering	
Reflow, Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at a time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

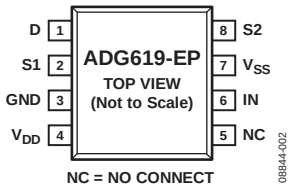


Figure 2. 8-Lead SOT-23 (RJ-8)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Drain Terminal. Can be an input or output.
2	S1	Source Terminal. Can be an input or output.
3	GND	Ground (0 V) Reference.
4	V_{DD}	Most Positive Power Supply.
5	NC	No Connect. Not internally connected.
6	IN	Logic Control Input.
7	V_{SS}	Most Negative Power Supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications.
8	S2	Source Terminal. Can be an input or output.

Table 5. Truth Table for the ADG619-EP

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

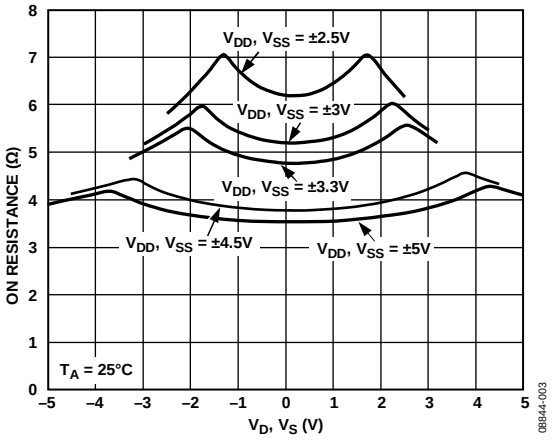


Figure 3. On Resistance vs. V_D, V_S (Dual Supply)

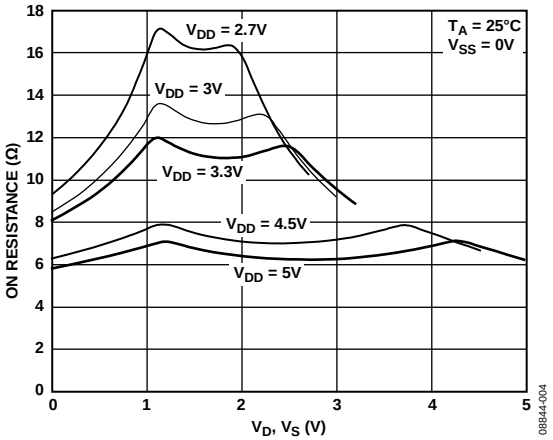


Figure 4. On Resistance vs. V_D, V_S (Single Supply)

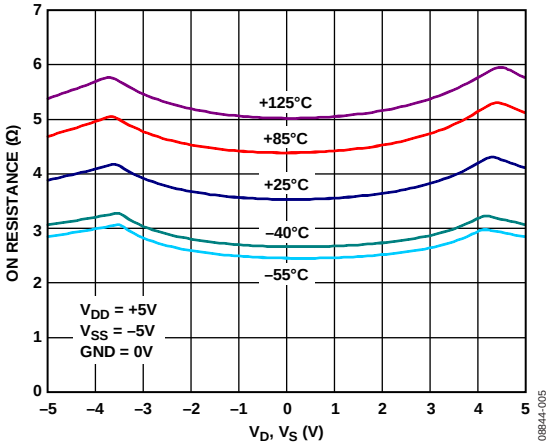


Figure 5. On Resistance vs. V_D, V_S for Different Temperatures (Dual Supply)

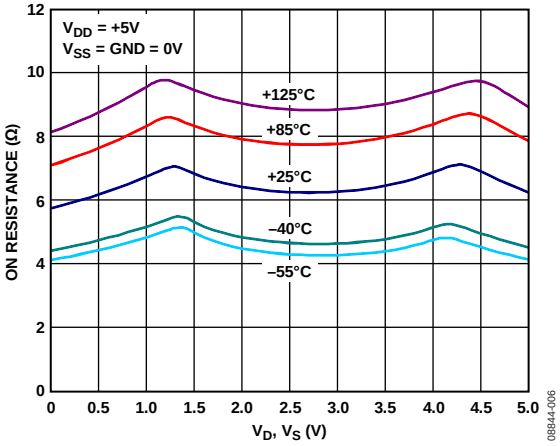


Figure 6. On Resistance vs. V_D, V_S for Different Temperatures (Single Supply)

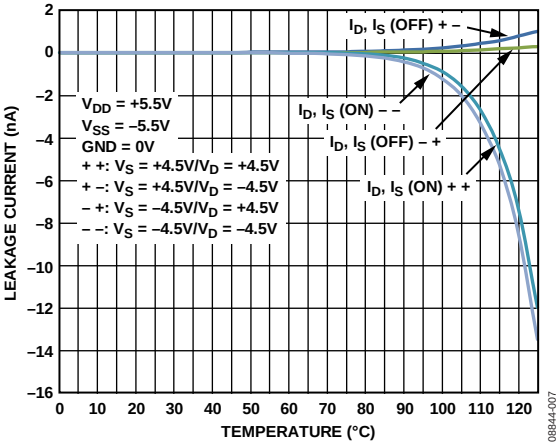


Figure 7. Leakage Currents vs. Temperature (Dual Supply)

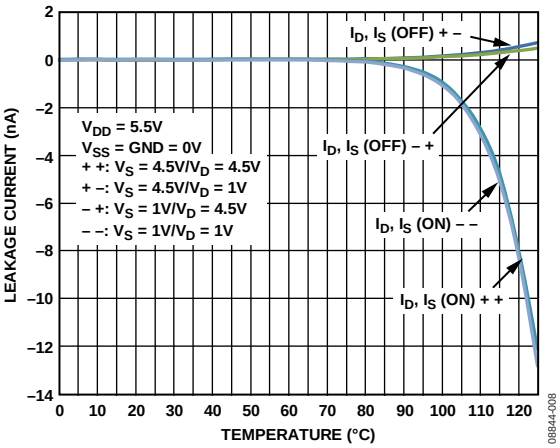


Figure 8. Leakage Currents vs. Temperature (Single Supply)

TEST CIRCUITS

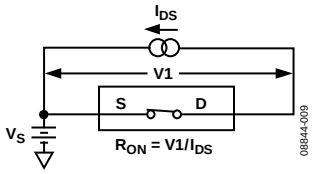


Figure 9. On Resistance

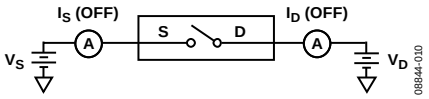


Figure 10. Off Leakage

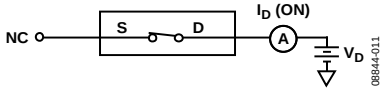


Figure 11. On Leakage

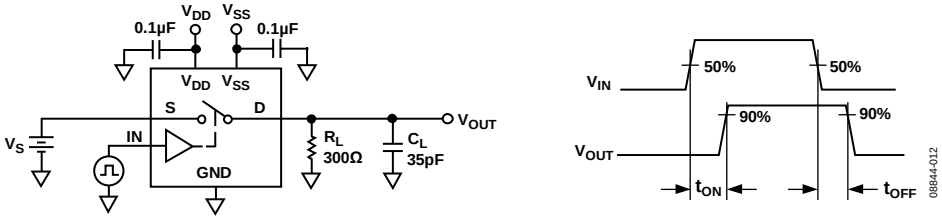


Figure 12. Switching Times

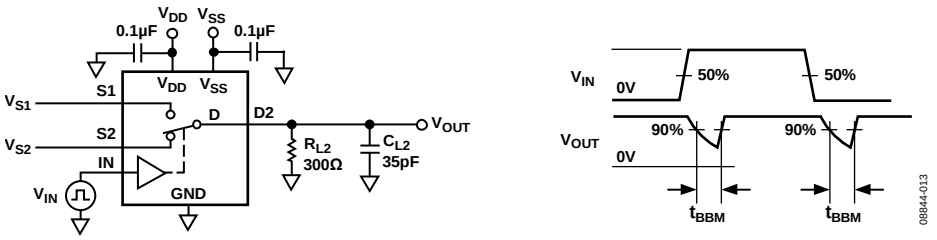


Figure 13. Break-Before-Make Time Delay, t_{BBM}

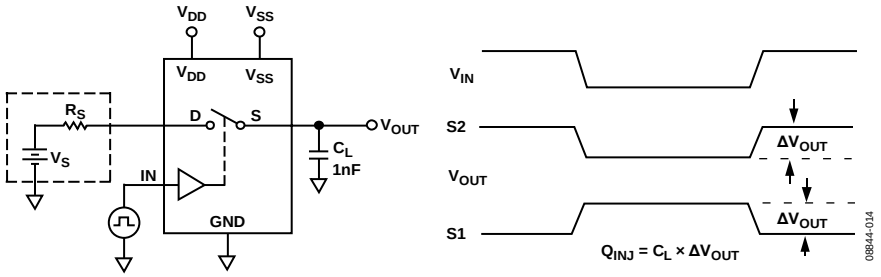


Figure 14. Charge Injection

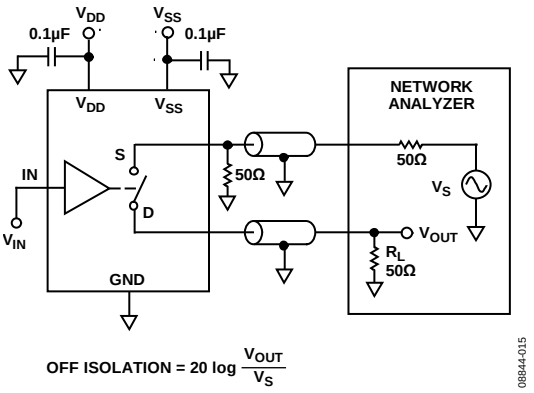


Figure 15. Off Isolation

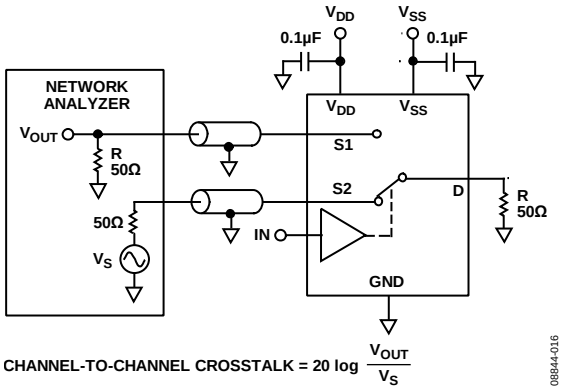


Figure 16. Channel-to-Channel Crosstalk

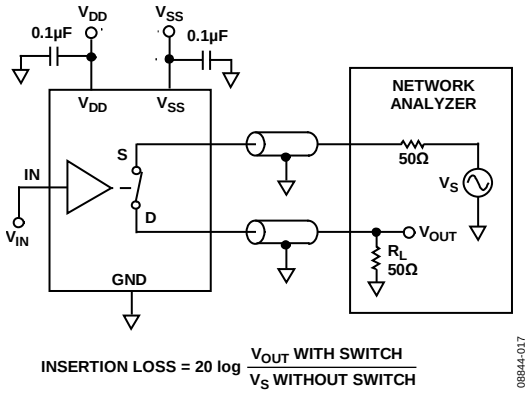
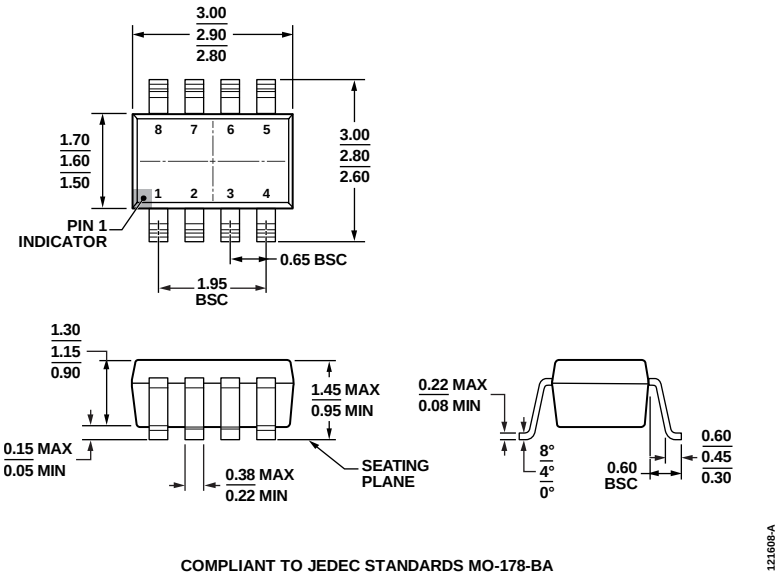


Figure 17. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 18. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding[2]
ADG619SRJZ-EP-RL7	−55°C to +125°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	S3V

[1] Z =RoHS Compliant Part.
[2] Branding on SOT-23 packages is limited to three characters due to space constraints

NOTES

NOTES

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