LTM4620A
High Efficiency, Dual 13A Step-Down Power µModule Regulator

DESCRIPTION

Demonstration circuit 1759A features the LTM®4620AEV, the high efficiency, high density, dual 13A, switch mode step-down power module regulator. The input voltage is from 5.5V to 16V. The output voltage is programmable from 0.6V to 5V. DC1759A can deliver 13A maximum current from each channel. As explained in the data sheet, output current derating is necessary for certain V_{IN}, V_{OUT}, and thermal conditions. The board operates in continuous conduction mode in heavy load conditions. For high efficiency at low load currents, the MODE jumper (JP1) selects pulse-skipping mode for noise sensitive applications or Burst Mode® operation in less noise sensitive applications. Two outputs can be connected in parallel for a single 26A output solution with optional jumper resistors. The board allows the user to program how its output ramps up and down through the TRACK/SS pin. The output can be set up to either coincidentally or ratiometrically track with another supply's output. Remote output voltage sensing is available for improved output voltage regulation at the load point. These features and the availability of the LTM4620AEV in a compact 15mm × 15mm × 4.41mm LGA package make it ideal for use in many high density point-of-load regulation applications. The LTM4620A data sheet must be read in conjunction with this demo manual for working on or modifying the demo circuit 1759A.

Design files for this circuit board are available at http://www.linear.com/demo

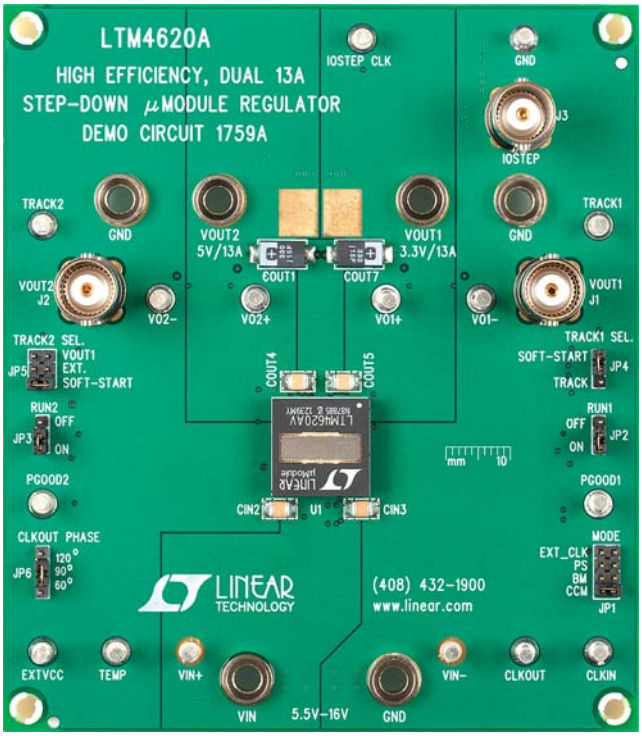


Figure 1. LTM4620A/DC1759A Demo Board

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Input Voltage Range		5.5V ~ 16V
Output Voltage V_{OUT1}	V_{IN} = 5.5V ~ 16V, I_{OUT1} = 0A ~ 13A, JP1: CCM	3.3V ±1.5%
Output Voltage V_{OUT2}	V_{IN} = 5.5V ~16V, I_{OUT2} = 0A ~ 13A, JP1: CCM	5V ±1.5%
Per-Channel Maximum Continuous Output Current	Derating is Necessary for Certain V_{IN}, V_{OUT} and Thermal Conditions, See Data Sheet for Detail.	13A (per-Channel)
Default Operating Frequency		750kHz
Resistor Programmable Frequency Range		250kHz to 780kHz
External Clock Sync. Frequency Range		400kHz to 780kHz
Efficiency of Channel 1	V_{IN} = 12V, V_{OUT1} = 3.3V, I_{OUT1} = 13A, f_{SW} = 750kHz	91.7% See Figure 3
Efficiency of Channel 2	V_{IN} = 12V, V_{OUT2} = 5V, I_{OUT2} = 13A, f_{SW} = 750kHz	93.8% See Figure 4
Load Transient of Channel 1	V_{IN} = 12V, V_{OUT1} = 3.3V, I_{SETP} = 6.5A ~ 13A	See Figure 5
Load Transient of Channel 2	V_{IN} = 12V, V_{OUT2} = 5V, I_{SETP} = 6.5A ~ 13A	See Figure 6

QUICK START PROCEDURE

Demonstration circuit 1759A is easy to set up to evaluate the performance of the LTM4620AEV. Please refer to Figure 2 for proper measurement setup and follow the procedure below:

1. Place jumpers in the following positions for a typical application:

JP1	JP2	JP3	JP4	JP5	JP6
MODE	**RUN1**	**RUN2**	**TRACK1 SEL.**	**TRACK2 SEL.**	**CLKOUT PHASE**
CCM	ON	ON	SOFT-START	SOFT-START	90°

2. With power off, connect the input power supply, load and meters as shown in Figure 2. Preset the load to 0A and V_{IN} supply to 12V.
3. Turn on the power supply at the input. The output voltage in channel 1 should be 3.3V ±1.5% (3.2505V ~ 3.3495V) and the output voltage in channel 2 should be 5V ±1.5% (4.925V ~ 5.075V).
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, output voltage ripple, efficiency and other parameters. Output ripple should be measured at J1 and J2 with BNC cables. 50Ω termination should be set on the oscilloscope or BNC cables.
5. (Optional) For optional load transient test, apply an adjustable pulse signal between IOSTEP CLK and GND test point. Pulse amplitude (3V ~ 3.5V) sets the load step current amplitude. The output transient current can be monitored at the BNC connector J3 (15mV/A). The pulse signal should have very small duty cycle (<1%) to limit the thermal stress on the transient load circuit. Switch the jumper resistors R34 or R35 (on the backside of boards) to apply load transient on channel 1 or channel 2 correspondingly.
6. (Optional) LTM4620A can be synchronized to an external clock signal. Place the JP1 jumper on EXT_CLK and apply a clock signal (0V ~ 5V, square wave) on the CLKIN test point.
7. (Optional) The outputs of LTM4620A can track another supply. The jumpers JP4 and JP5 allow choosing soft-start or output tracking. If tracking external voltage is selected, the corresponding test points, TRACK1 and TRACK2, need to be connected to a valid voltage signal.
8. (Optional) LTM4620A can be configured for a 2-phase single output at up to 26A on DC1759A. Install 0Ω resistors on R14, R17, R28, R39 and remove R7, R19. Output voltage is set by R25 based on equation V_{OUT} = 0.6V(1 + 60.4k/R25).

QUICK START PROCEDURE

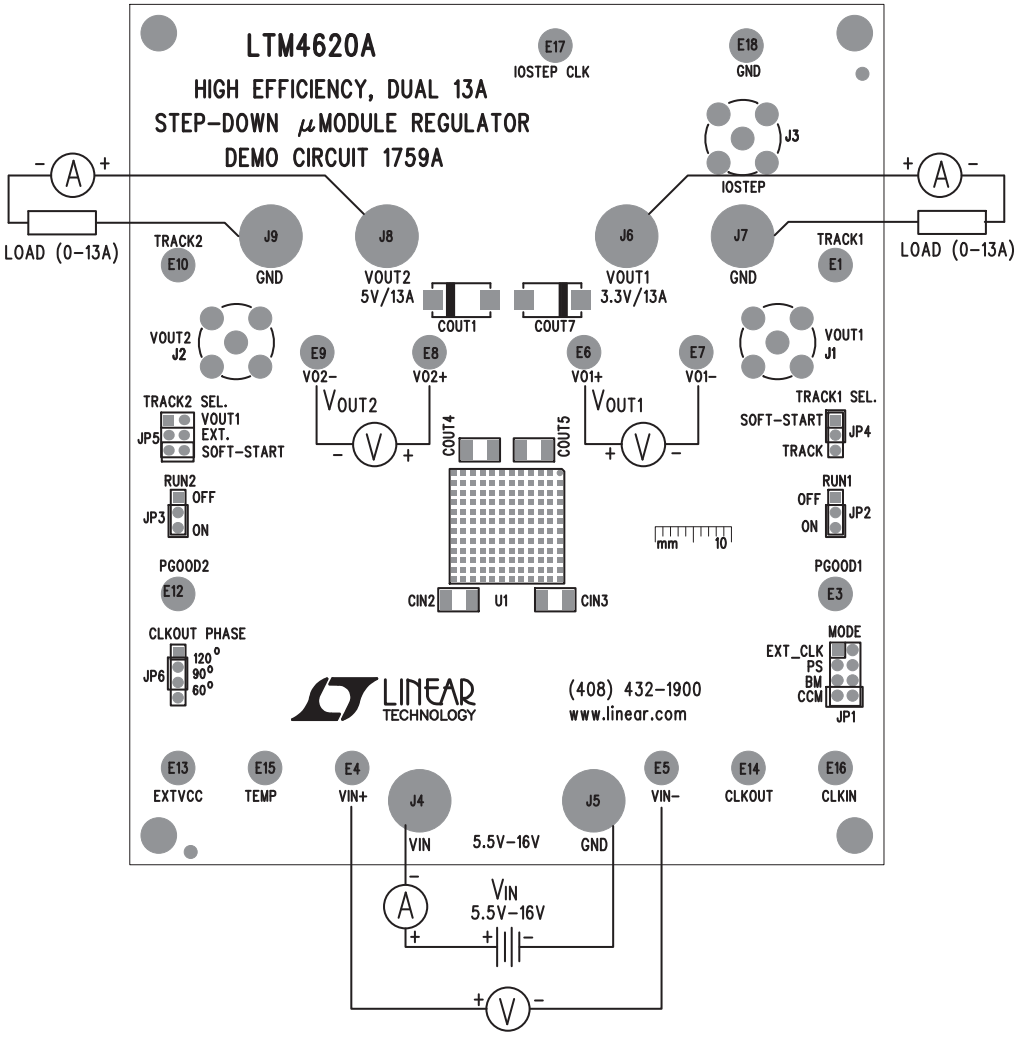


Figure 2. Test Setup of DC1759A

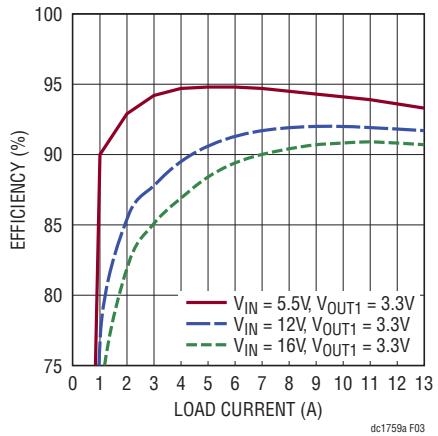


Figure 3. Measured Efficiency on Channel 1 (V_{OUT1} = 3.3V, f_{SW} = 750kHz, Channel 2 Disabled)

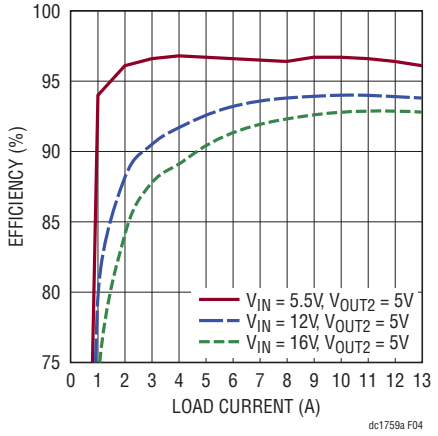


Figure 4. Measured Efficiency on Channel 2 (V_{OUT2} = 5V, f_{SW} = 750kHz, Channel 1 Disabled)

QUICK START PROCEDURE

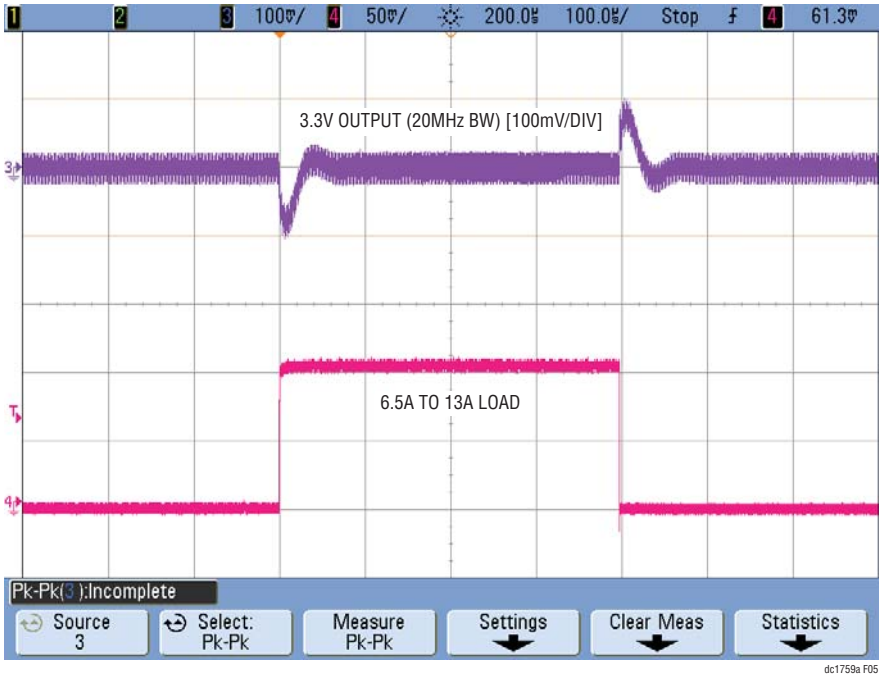


Figure 5. Measured Channel 1 6.5A to 13A Load Transient (V_{IN} = 12V, V_{OUT1} = 3.3V)

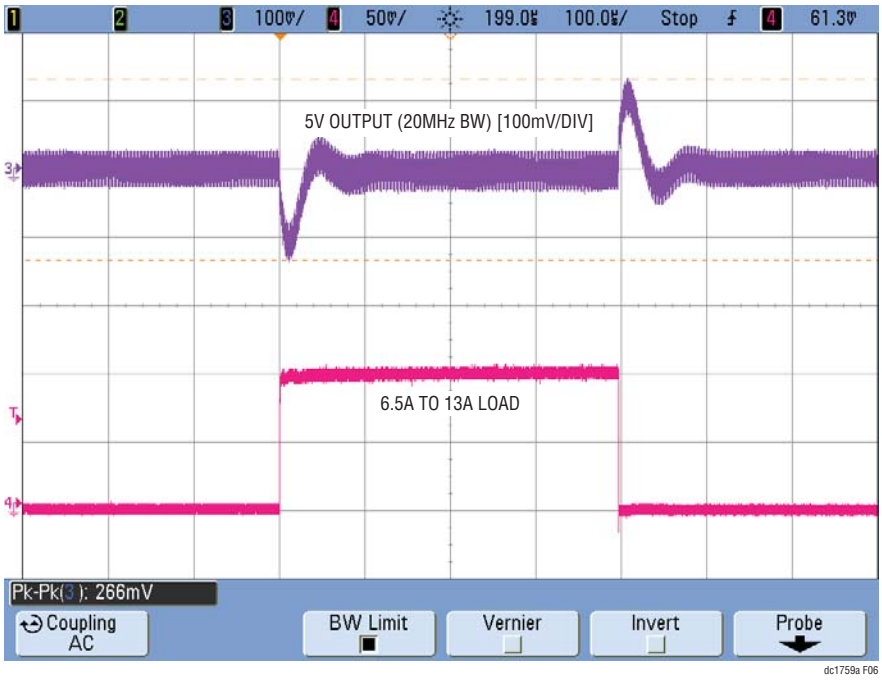


Figure 6. Measured Channel 2 6.5A to 13A Load Transient (V_{IN} = 12V, V_{OUT2} = 5V)

QUICK START PROCEDURE

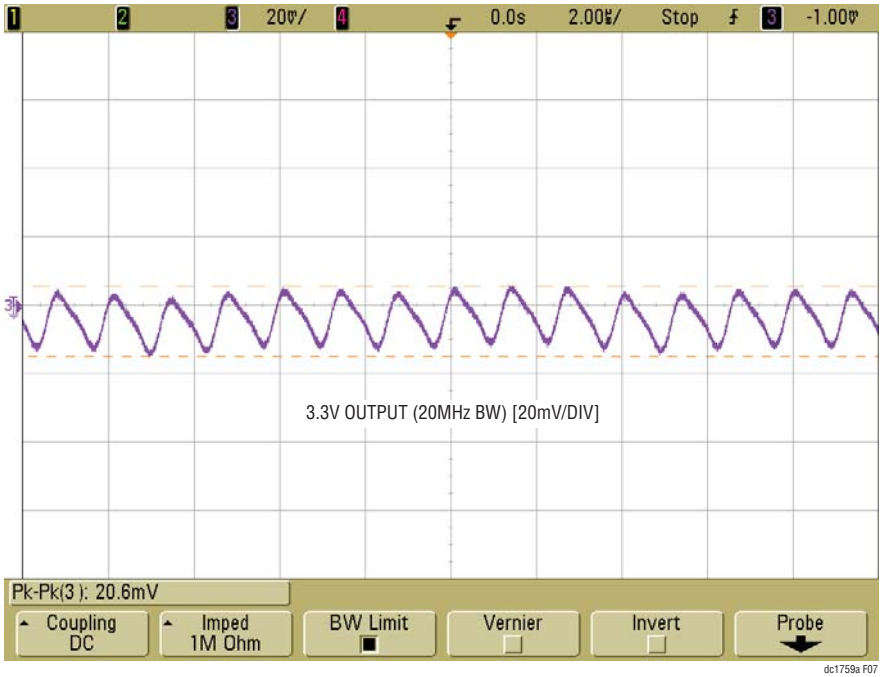


Figure 7. Measured Output Voltage Ripple at 12V Input, 3.3V/13A Output with Standard Demo Circuit Default Setup

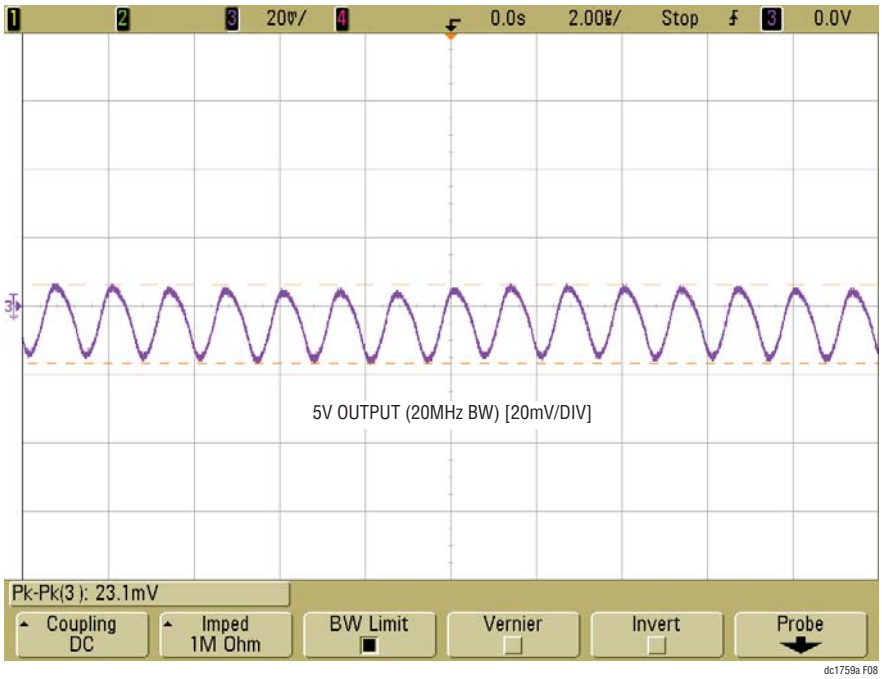


Figure 8. Measured Output Voltage Ripple at 12V Input, 5V/13A Output with Standard Demo Circuit Default Setup

QUICK START PROCEDURE

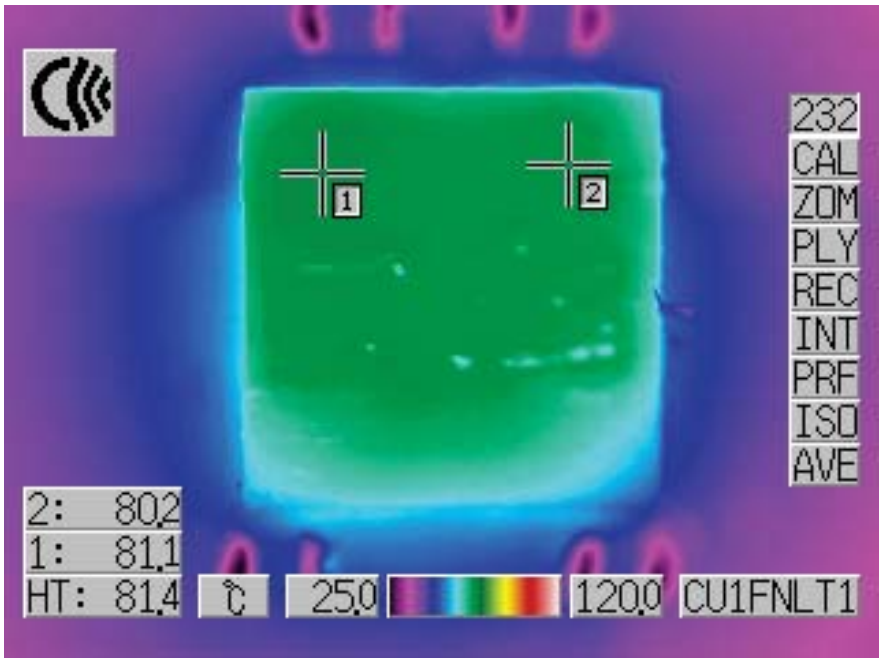
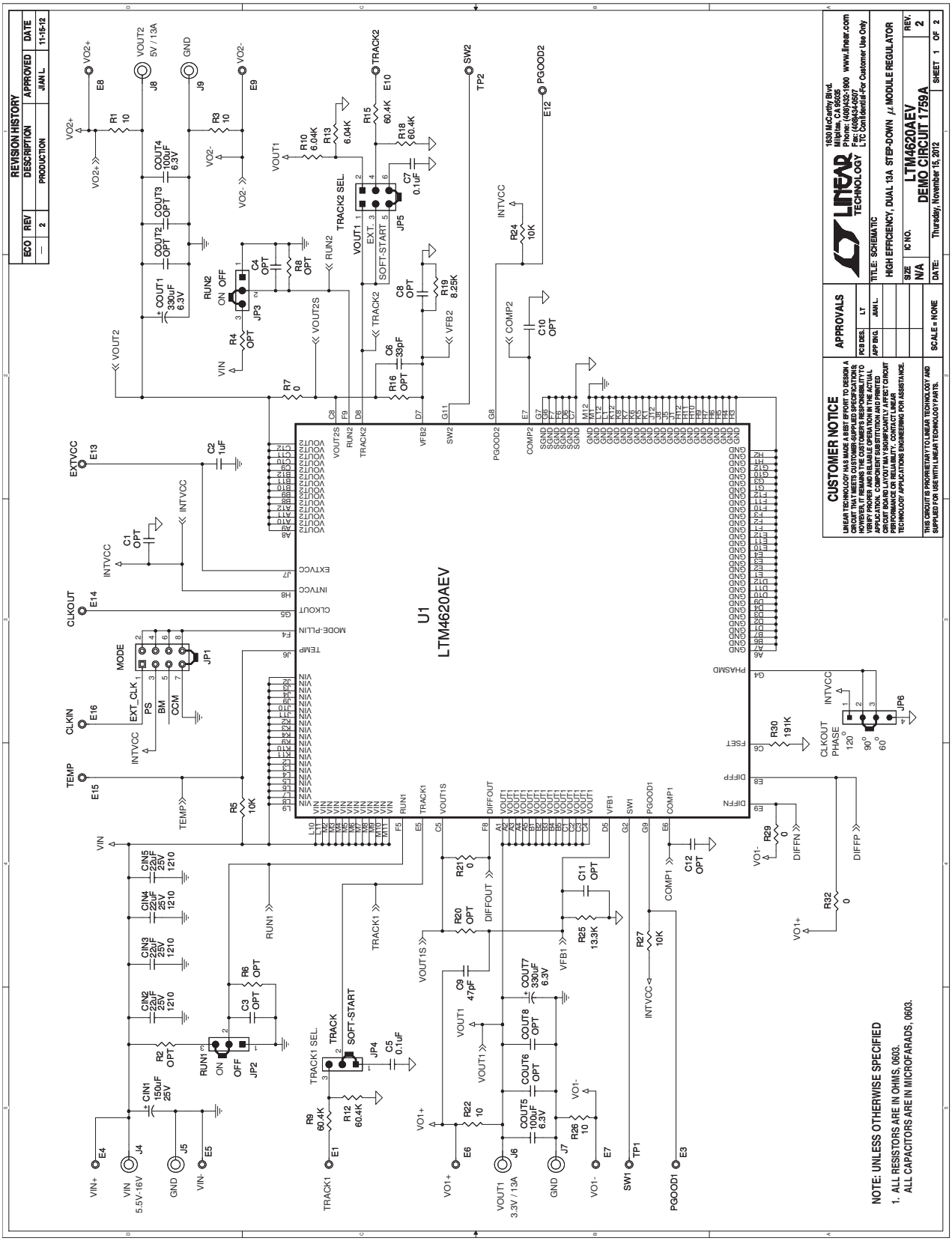


Figure 9. Thermal Capture at $12V_{IN}$, $3.3V_{OUT}$ at 13A and $5V_{OUT}$ at 13A (Ambient Temperature = 23°C, 200LFM Airflow and No Heat Sink)

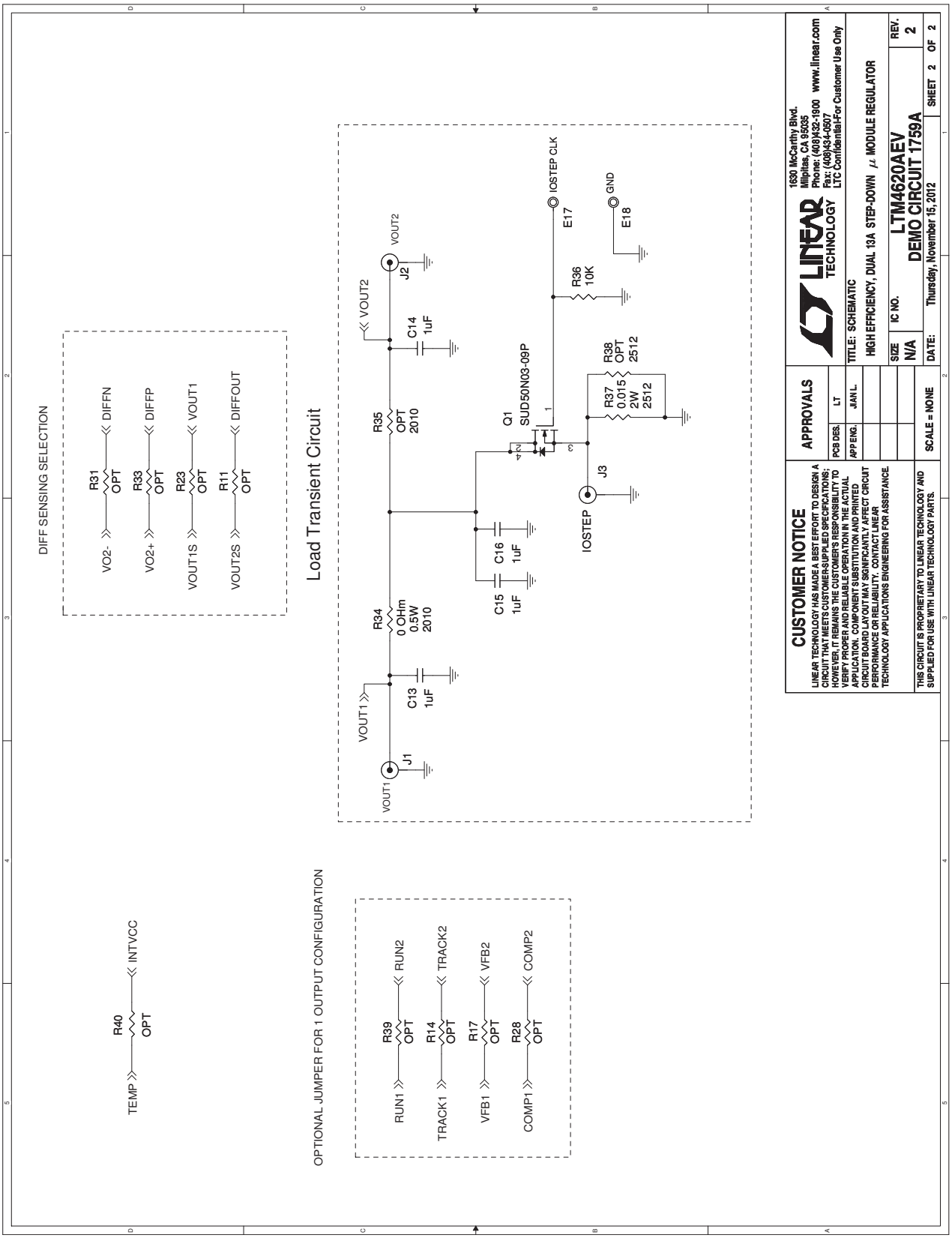
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN1	Cap., 150µF, 25V, Aluminum Electr.,	SUN ELECT., 25CE150AX
2	3	CIN2, CIN3, CIN4, CIN5	Cap., X5R, 22µF, 25V, 10%, 1210	MURATA, GRM32ER61E226KE15
3	2	COUT1, COUT7	Cap., 330µF, 6.3V, POSCAP 7343	SANYO, 6TPF330M9L
4	2	COUT4, COUT5	Cap., X5R, 100µF, 6.3V, 20% 1210	AVX, 12106D107MAT2A
5	1	C2	Cap., X7R, 1µF, 25V, 10%, 0805	AVX, 08053C105KAT2A
6	2	C5, C7	Cap., X5R, 0.1µF, 25V, 10%, 0603	AVX, 06033D104KAT
7	1	C6	Cap., 33pF, 10V, 10%, 0603	AVX, 0603ZC330KAT2A
8	1	C9	Cap., 47pF, 10V, 10%, 0603	AVX, 0603ZC470KAT2A
9	4	C13, C14, C15, C16	Cap., X7R, 1µF, 10V, 10%, 0603	AVX, 0603ZC105KAT
10	1	Q1	N-Channel 30-V Mosfet	VISHAY, SUD50N03-09P
11	4	R1, R3, R22, R26	Res., Chip, 10Ω, 1%, 0603	NIC, NRC06F10R0TRF
12	4	R5, R24, R27, R36	Res., Chip, 10k, 1%, 0603	YAGEO, RC0603FR-0710KL
13	4	R7, R21, R29, R32	Res., Chip, 0Ω, 1%, 0603	VISHAY, CRCW06030000Z0ED
14	4	R9, R12, R15, R18	Res., Chip, 60.4k, 1%, 0603	VISHAY, CRCW060360K4FKED
15	2	R10, R13	Res., Chip, 6.04k, 1%, 0603	YAGEO, RC060FR-0760K4L
16	1	R19	Res., Chip, 8.25k, 1%, 0603	VISHAY, CRCW06038K25FKED
17	1	R25	Res., Chip, 13.3k, 1%, 0603	VISHAY, CRCW060313K3FKED
18	1	R30	Res., Chip, 191k, 1%, 0603	VISHAY, CRCW0603191KFKED
19	1	R34	Res., Chip, 0Ω, 0.5W, 2010	TEPRO, RN6083
20	1	R37	Res., Chip, 0.015Ω, 2W, 2512	VISHAY, WSL2512R0150FEA
21	1	U1	LTM4620AEV 15X15X4.41-LGA	LINEAR TECH., LTM4620AEV
Additional Circuits				
22	0	COUT2, COUT3, COUT6, COUT8,	OPT 1210	OPT
23	0	C1	OPT 0805	OPT
24	0	C3, C4, C8, C10, C11, C12	OPT 0603	OPT
25	0	R2, R4, R6, R8, R11, R14, R16, R17, R20, R23, R28, R31, R33, R39, R40	OPT 0603	OPT
26	0	R35	OPT 2010	OPT
27	0	R38	OPT 2512	OPT
Hardware/Components (For Demo Board Only)				
28	16	E1, E3-E10, E12-E18	TESTPOINT, TURRET, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
29	3	J1, J2, J3	CONN, BNC, 5 PINS	CONNEX 112404
30	6	J4-J9	CONN, BANANA JACK, KEYSTONE-575-4	KEYSTONE 575-4
31	1	JP1	HEADER 4 PIN 0.079 DOUBLE ROW	SAMTEC, TMM104-02-L-D
32	1	JP6	HEADER 4 PIN 0.079 SINGLE ROW	SAMTEC, TMM104-02-L-S
33	3	JP2, JP3, JP4	HEADER 3 PIN 0.079 SINGLE ROW	SAMTEC, TMM103-02-L-S
34	1	JP5	HEADER 3 PIN 0.079 DOUBLE ROW	SAMTEC, TMM-103-02-L-D
35	4	MTGS at 4 corners	STAND-OFF, NYLON 0.50"	KEYSTONE, 8833(SNAP-ON)
36	6	XJP1-XJP6	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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