Ultralow EMI 28V_{IN}, 6A DC/DC µModule Regulator

FEATURES

- **Complete Low EMI Switch Mode Power Supply**
- **Wide Input Voltage Range: 4.5V to 28V**
- **6A DC Typical, 8A Peak Output Current**
- **0.6V to 5V Output Voltage Range**
- **EN55022 Class B Certified**
- **Output Voltage Tracking and Margining**
- **PLL Frequency Synchronization**
- **±1.75% Total DC Error**
- **Power Good Output**
- **Current Foldback Protection (Disabled at Start-Up)**
- **Parallel/Current Sharing**
- Current Mode Control
- Up to 93% Efficiency at 5V_{IN}, 3.3V_{OUT}
- Programmable Soft-Start
- Output Overvoltage Protection
- –55°C to 125°C Operating Temperature Range (LTM4606MP)
- SnPb or RoHS Compliant Finish
- 15mm × 15mm × 2.82mm LGA Package
  15mm × 15mm × 3.42mm BGA Package

APPLICATIONS

- ASICs or FPGA Transceivers
- Telecom, Servers and Networking Equipment
- Industrial Equipment
- RF Equipment

DESCRIPTION

The LTM®4606 is a complete EN55022 Class B certified noise high voltage 6A switching mode DC/DC power supply. Included in the package are the switching controller, power FETs, inductor, and all support components. The on-board input filter and noise cancellation circuits achieve low noise operation, thus effectively reducing the electromagnetic interference (EMI). Operating over an input voltage range of 4.5V to 28V, the LTM4606 supports an output voltage range of 0.6V to 5V, set by a single resistor. This high efficiency design delivers 6A continuous current (8A peak). Only bulk input and output capacitors are needed to finish the design.

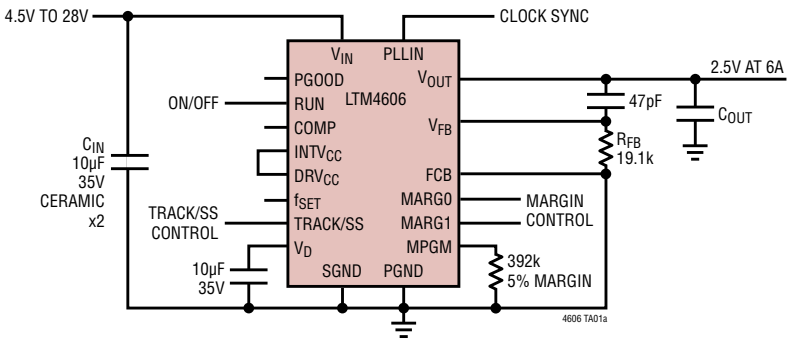
High switching frequency and an adaptive on-time current mode architecture enables a very fast transient response to line and load changes without sacrificing stability. The device supports output voltage tracking and output voltage margining.

Furthermore, the µModule® regulator can be synchronized with an external clock for reducing undesirable frequency harmonics and allows PolyPhase® operation for high load currents.

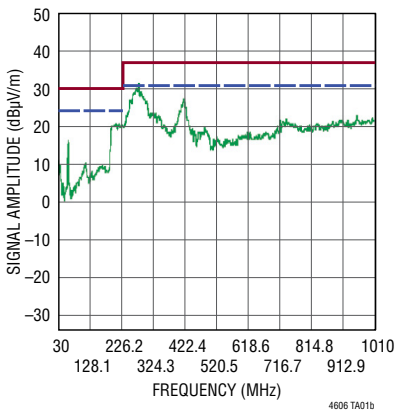
The LTM4606 is offered in space saving 15mm × 15mm × 2.82mm LGA and 15mm × 15mm × 3.42mm BGA packages. The LTM4606 is available with SnPb (BGA) or RoHS compliant terminal finish.

TYPICAL APPLICATION

Ultralow Noise 2.5V/6A Power Supply with 4.5V to 28V Input



Radiated Emission Scan at 12V_{IN}, 2.5V_{OUT}/6A



Rev. E

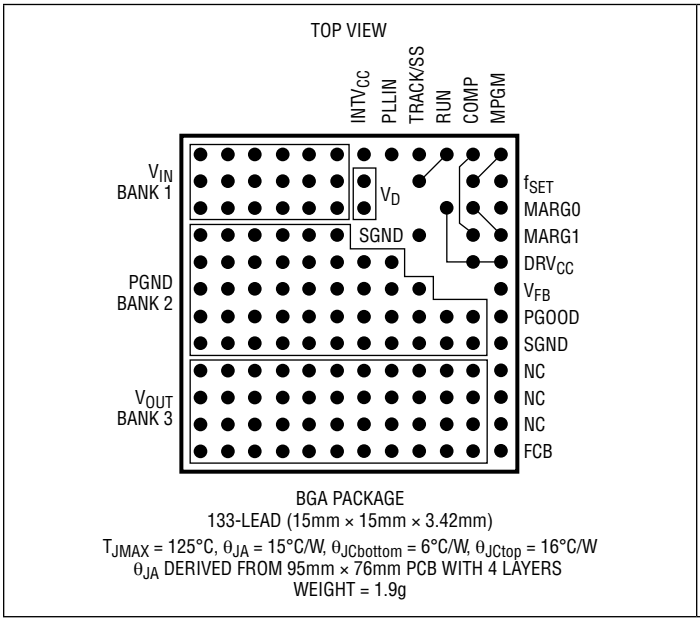
ABSOLUTE MAXIMUM RATINGS

(Note 1)

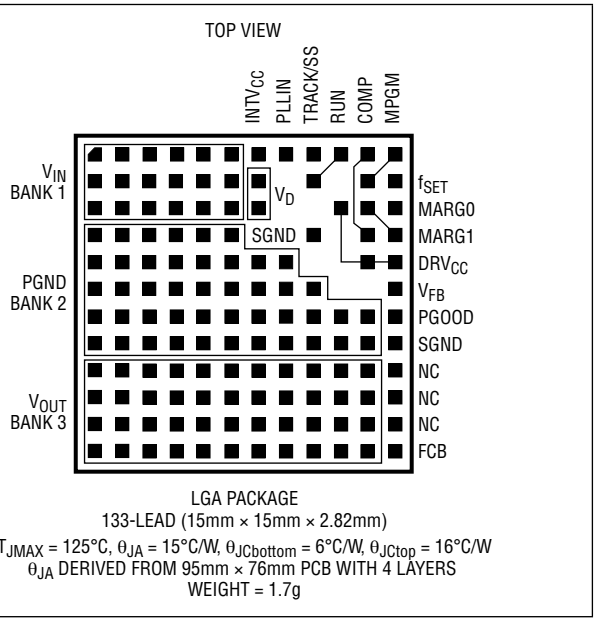
DRV_{CC}, V_{OUT} ..... –0.3V to 6V
PLLIN, FCB, TRACK/SS, MPGM, MARG0,
MARG1, PGOOD, RUN ..... –0.3V to $INTV_{CC}$ + 0.3V
V_{FB}, COMP ..... –0.3V to 2.7V
V_{IN}, V_D ..... –0.3V to 28V

Internal Operating Temperature Range (Note 2)
E and I Grades ..... –40°C to 125°C
MP Grade ..... –55°C to 125°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 125°C

PIN CONFIGURATION



BGA PACKAGE
133-LEAD (15mm × 15mm × 3.42mm)
T_{JMAX} = 125°C, θ_{JA} = 15°C/W, $\theta_{JCbottom}$ = 6°C/W, θ_{JCtop} = 16°C/W
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS
WEIGHT = 1.9g



LGA PACKAGE
133-LEAD (15mm × 15mm × 2.82mm)
T_{JMAX} = 125°C, θ_{JA} = 15°C/W, $\theta_{JCbottom}$ = 6°C/W, θ_{JCtop} = 16°C/W
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS
WEIGHT = 1.7g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4606EV#PBF	Au (RoHS)	LTM4606V	e4	LGA	3	–40°C to 125°C
LTM4606IV#PBF	Au (RoHS)	LTM4606V	e4	LGA	3	–40°C to 125°C
LTM4606MPV#PBF	Au (RoHS)	LTM4606MPV	e4	LGA	3	–55°C to 125°C
LTM4606EY#PBF	SAC305 (RoHS)	LTM4606Y	e1	BGA	3	–40°C to 125°C
LTM4606IY#PBF	SAC305 (RoHS)	LTM4606Y	e1	BGA	3	–40°C to 125°C
LTM4606IY	SnPb (63/37)	LTM4606Y	e0	BGA	3	–40°C to 125°C
LTM4606MPY#PBF	SAC305 (RoHS)	LTM4606Y	e1	BGA	3	–55°C to 125°C
LTM4606MPY	SnPb (63/37)	LTM4606Y	e0	BGA	3	–55°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted. Per typical application (front page) configuration, R_{FB} = 40.2k.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage		●	4.5		28	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF ×2, C_{OUT} = 200µF; FCB = 0 V_{IN} = 5V to 28V, I_{OUT} = 0A to 6A, (Note 4)	●	1.474	1.5	1.526	V
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	I_{OUT} = 0A			3.2	4	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 10µF ×2, C_{OUT} = 200µF, V_{OUT} = 1.5V V_{IN} = 5V V_{IN} = 12V			 0.6 0.7		 A A
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 5V, V_{OUT} = 1.5V, Switching Continuous V_{IN} = 12V, V_{OUT} = 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			27 25 22		mA mA µA
$I_{S(VIN)}$	Input Supply Current	 V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 6A V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 6A			 0.96 2.18		 A A
$INTV_{CC}$	V_{IN} = 12V, RUN > 2V	No Load		4.7	5	5.3	V
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)		0		6	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.5V, FCB = 0V, V_{IN} = 4.5V to 28V, I_{OUT} = 0A	●		0.05	0.3	%
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.5V, FCB = 0V, I_{OUT} = 0A to 6A V_{IN} = 12V (Note 4)	 ●			 0.3	 %
$V_{IN(AC)}$	Input Ripple Voltage	I_{OUT} = 0A, C_{IN} = 10µF X5R Ceramic ×3 and 100µF Electrolytic V_{IN} = 5V, V_{OUT} = 1.5V V_{IN} = 12V, V_{OUT} = 1.5V			 2 3		 mV_{P-P} mV_{P-P}
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 22µF X5R Ceramic ×3 and 100µF X5R Ceramic V_{IN} = 5V, V_{OUT} = 1.5V V_{IN} = 12V, V_{OUT} = 1.5V			 8 11		 mV_{P-P} mV_{P-P}
f_S	Output Ripple Voltage Frequency	I_{OUT} = 5A, V_{IN} = 12V, V_{OUT} = 1.5V			900		kHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 200µF, V_{OUT} = 1.5V, I_{OUT} = 0A, TRACK/SS = 10nF V_{IN} = 12V V_{IN} = 5V			 20 20		 mV mV
t_{START}	Turn-On Time	C_{OUT} = 200µF; V_{OUT} = 1.5V, TRACK/SS = Open I_{OUT} = 1A Resistive Load V_{IN} = 5V V_{IN} = 12V			 0.5 0.5		 ms ms
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 22µF Ceramic, 470µF ×2 V_{IN} = 12V V_{OUT} = 1.5V			35		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 12V			25		µs
$I_{OUT(PK)}$	Output Current Limit	C_{OUT} = 200µF V_{IN} = 5V, V_{OUT} = 1.5V V_{IN} = 12V, V_{OUT} = 1.5V			 10 10		 A A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted. Per typical application (front page) configuration, R_{FB} = 40.2k.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.591	0.6	0.609	V
V_{RUN}	RUN Pin On/Off Threshold			1	1.5	1.9	V
$I_{TRACK/SS}$	Soft-Start Charging Current	$V_{TRACK/SS}$ = 0V		–1	–1.5	–2	µA
V_{FCB}	Forced Continuous Threshold			0.57	0.6	0.63	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0V			–1	–2	µA
$t_{ON(MIN)}$	Minimum On Time	(Note 3)			50	100	ns
$t_{OFF(MIN)}$	Minimum Off Time	(Note 3)			250	400	ns
R_{PLLIN}	PLLIN Input Resistor				50		kΩ
I_{DRVCC}	Current into DRV_{CC} Pin	V_{OUT} = 1.5V, I_{OUT} = 1A, DRV_{CC} = 5V			15	25	mA
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins			60.098	60.4	60.702	kΩ
$V_{RUN(MAX)}$	Maximum RUN Pin Voltage	5.1V Zener Clamp			5		V
Margin Section							
V_{MPGM}	Margin Reference Voltage				1.18		V
V_{MARG0}, V_{MARG1}	MARG0, MARG1 Voltage Threshold				1.4		V
PGOOD							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		7	10	13	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–7	–10	–13	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			1.5		%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.15	0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

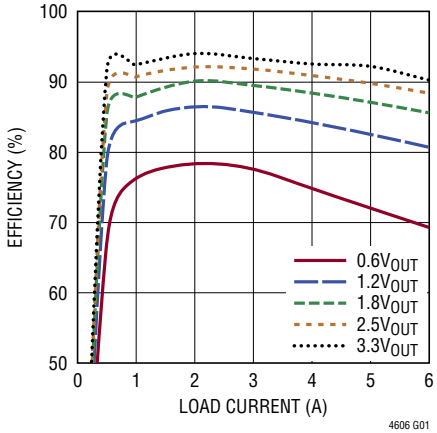
Note 2: The LTM4606E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4606I is guaranteed to meet specifications over the –40°C to 125°C internal operating temperature range. The LTM4606MP is guaranteed and tested over the –55°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: 100% tested at die level only.

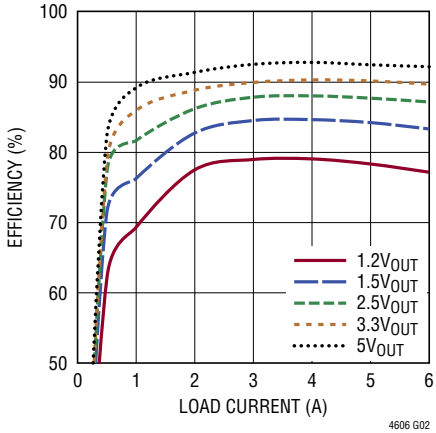
Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

TYPICAL PERFORMANCE CHARACTERISTICS

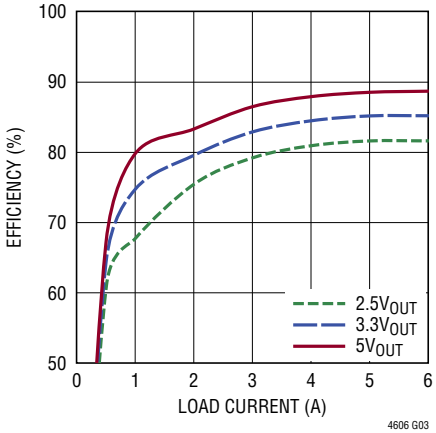
Efficiency vs Load Current with $5V_{IN}$ (FCB = 0)



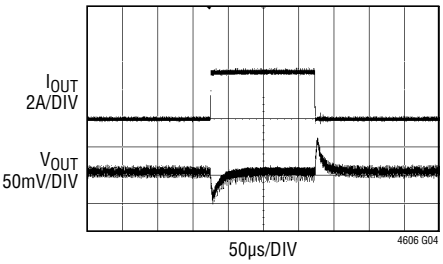
Efficiency vs Load Current with $12V_{IN}$ (FCB = 0)



Efficiency vs Load Current with $24V_{IN}$ (FCB = 0)

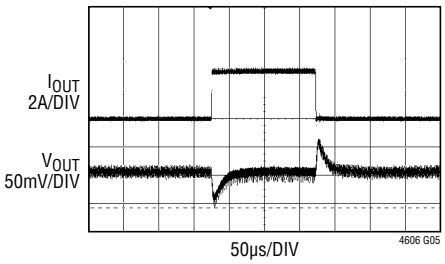


1.2V Transient Response



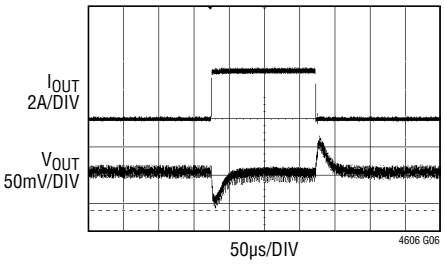
1.2V AT 3.5A/µs LOAD STEP
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC

1.5V Transient Response



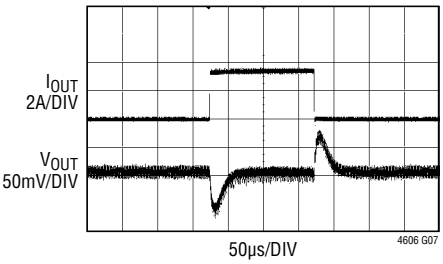
1.5V AT 3.5A/µs LOAD STEP
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC

1.8V Transient Response



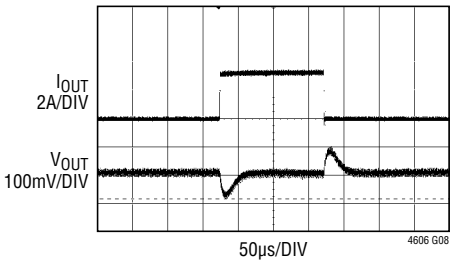
1.8V AT 3.5A/µs LOAD STEP
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC

2.5V Transient Response



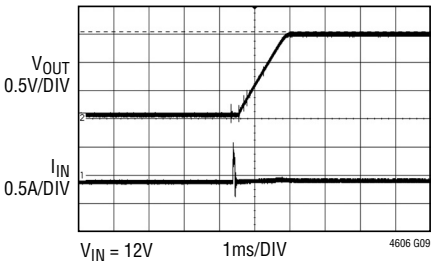
2.5V AT 3.5A/µs LOAD STEP
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC

3.3V Transient Response



3.3V AT 3.5A/µs LOAD STEP
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC

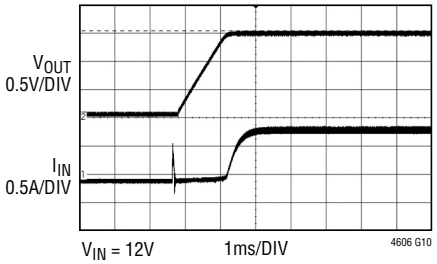
–55°C, Start-Up, I_{OUT} = 0A



V_{IN} = 12V
V_{OUT} = 1.5V
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC
SOFT-START = 3.9nF

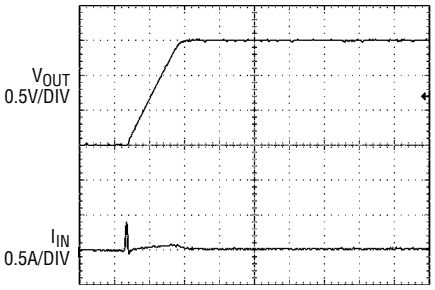
TYPICAL PERFORMANCE CHARACTERISTICS

–55°C, Start-Up, I_{OUT} = 6A



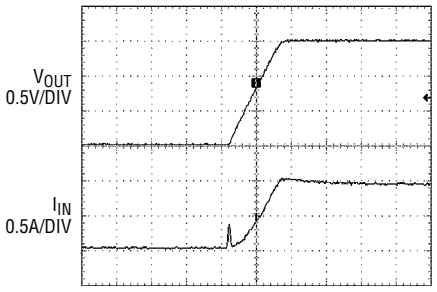
V_{IN} = 12V 1ms/DIV
V_{OUT} = 1.5V
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC
SOFT-START = 3.9nF

Start-Up, I_{OUT} = 0A



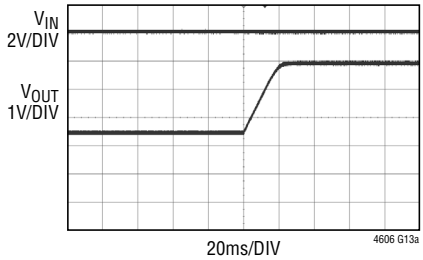
V_{IN} = 12V 1ms/DIV
V_{OUT} = 1.5V
C_{OUT} = 1× 22µF, 6.3V CERAMIC
1× 330µF, 4V SANYO POSCAP
SOFT-START = 3.9nF

Start-Up, I_{OUT} = 6A (Resistive Load)



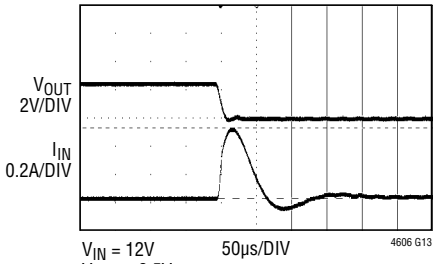
V_{IN} = 12V 1ms/DIV
V_{OUT} = 1.5V
C_{OUT} = 1× 22µF, 6.3V CERAMIC
1× 330µF, 4V SANYO POSCAP
SOFT-START = 3.9nF

Start Into Pre-Biased Output



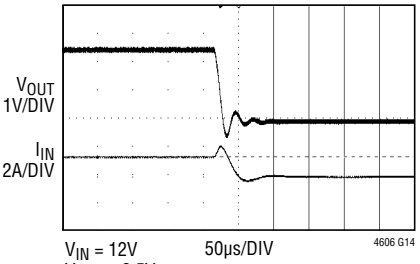
V_{IN} = 12V
V_{OUT} = 5V
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC
SOFT-START = 0.1µF

Short-Circuit Protection, I_{OUT} = 0A



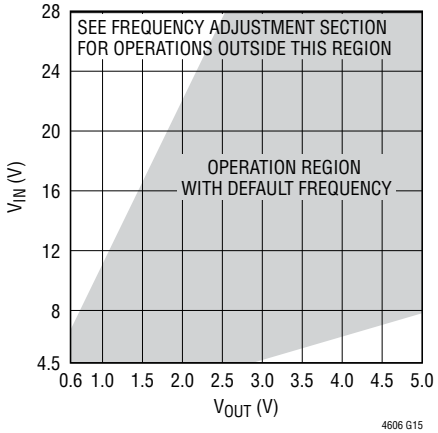
V_{IN} = 12V 50µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC
SOFT-START = 0.1µF

Short-Circuit Protection, I_{OUT} = 6A

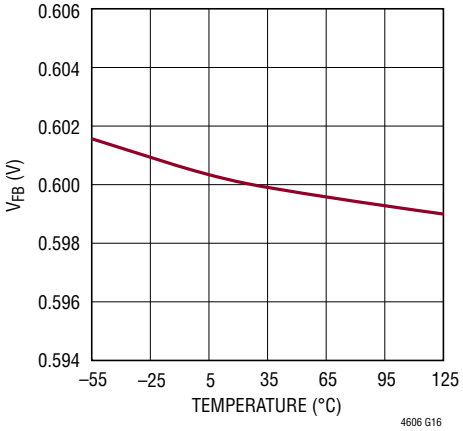


V_{IN} = 12V 50µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 2× 22µF, 10V CERAMIC
1× 100µF, 6.3V CERAMIC
SOFT-START = 0.1µF

V_{IN} to V_{OUT} Step-Down Operation Region

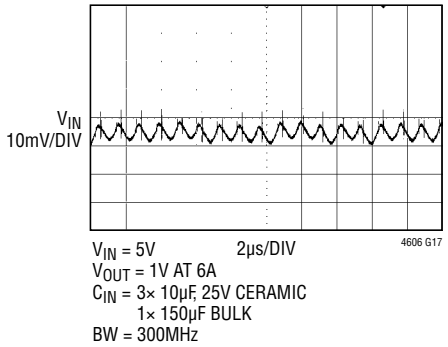


V_{FB} vs Temperature



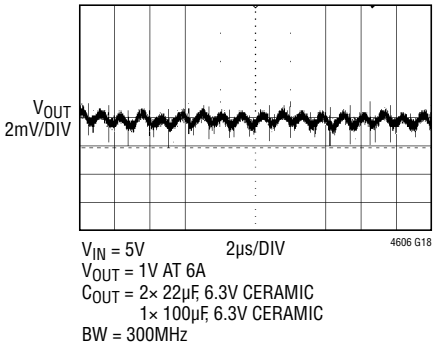
TYPICAL PERFORMANCE CHARACTERISTICS

Input Ripple



V_{IN} = 5V 2µs/DIV
V_{OUT} = 1V AT 6A
C_{IN} = 3× 10µF, 25V CERAMIC
1× 150µF BULK
BW = 300MHz

Output Ripple



V_{IN} = 5V 2µs/DIV
V_{OUT} = 1V AT 6A
C_{OUT} = 2× 22µF, 6.3V CERAMIC
1× 100µF, 6.3V CERAMIC
BW = 300MHz

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN} (Bank 1): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

V_{OUT} (Bank 3): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins (see Figure 17).

PGND (Bank 2): Power Ground Pins for Both Input and Output Returns.

V_D (Pins B7, C7): Top FET Drain Pins. Add more capacitors between V_D and ground to handle the input RMS current and reduce the input ripple further.

DRV_{CC} (Pins C10, E11, E12): These pins normally connect to $INTV_{CC}$ for powering the internal MOSFET drivers. They can be biased up to 6V from an external supply with about 50mA capability, or an external circuit as shown in Figure 18. This improves efficiency at the higher input voltages by reducing power dissipation in the module.

$INTV_{CC}$ (Pin A7): This pin is for additional decoupling of the 5V internal regulator.

PLLIN (Pin A8): External Clock Synchronization Input to the Phase Detector. This pin is internally terminated to SGND with a 50k resistor. Apply a clock with high level above 2V and below $INTV_{CC}$. See the Applications Information section.

FCB (Pin M12): Forced Continuous Input. Connect this pin to SGND to force continuous synchronization operation at low load, to $INTV_{CC}$ to enable discontinuous mode operation at low load or to a resistive divider from a secondary output when using a secondary winding.

TRACK/SS (Pin A9): Output Voltage Tracking and Soft-Start Pin. When the module is configured as a master output, then a soft-start capacitor is placed on this pin to ground to control the master ramp rate. A soft-start capacitor can be used for soft-start turn-on in a stand-alone regulator. Slave operation is performed by putting a resistor divider from the master output to ground, and connecting the center point of the divider to this pin. See the Applications Information section.

MPGM (Pins A12, B11): Programmable Margining Input. A resistor from these pins to ground sets a current that is equal to 1.18V/R. This current multiplied by 10kΩ will equal a value in millivolts that is a percentage of the 0.6V reference voltage. See the Applications Information section. To parallel LTM4606s, each requires an individual MPGM resistor. Do not tie MPGM pins together.

PIN FUNCTIONS

f_{SET} (Pin B12): Frequency set internally to 800kHz in continuous conducting mode at light load. An external resistor can be placed from this pin to ground to increase frequency. See the Applications Information section for frequency adjustment.

V_{FB} (Pin F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between the V_{FB} and SGND pins. See the Applications Information section.

MARG0 (Pin C12): LSB Logic Input for the Margining Function. Together with the MARG1 pin, the MARG0 pin will determine if a margin high, margin low, or no margin state is applied. The pin has an internal pull-down resistor of 50k. See the Applications Information section.

MARG1 (Pins C11, D12): MSB Logic Input for the Margining Function. Together with the MARG0 pin, the MARG1 pins will determine if a margin high, margin low, or no margin state is applied. The pins have an internal pull-down resistor of 50k. See the Applications Information section.

SGND (Pins D9, H12): Signal Ground Pins. These pins connect to PGND at output capacitor point. See Figure 17.

COMP (Pins A11, D11): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.7V corresponding to zero sense voltage (zero current).

PGOOD (Pin G12): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point, after a 25µs power bad mask timer expires.

RUN (Pins A10, B9): Run Control Pins. A voltage above 1.9V will turn on the module, and below 1V will turn off the module. A programmable UVLO function can be accomplished with a resistor divider from V_{IN} to ground. See Figure 1. This pin has a 5.1V Zener to ground. Maximum pin voltage is 5V. Limit current into the RUN pin to less than 1mA.

NC (Pins J12, K12, L12): These pads must be left floating (electrical open circuit) and are used for enhanced solder joint strength.

BLOCK DIAGRAM

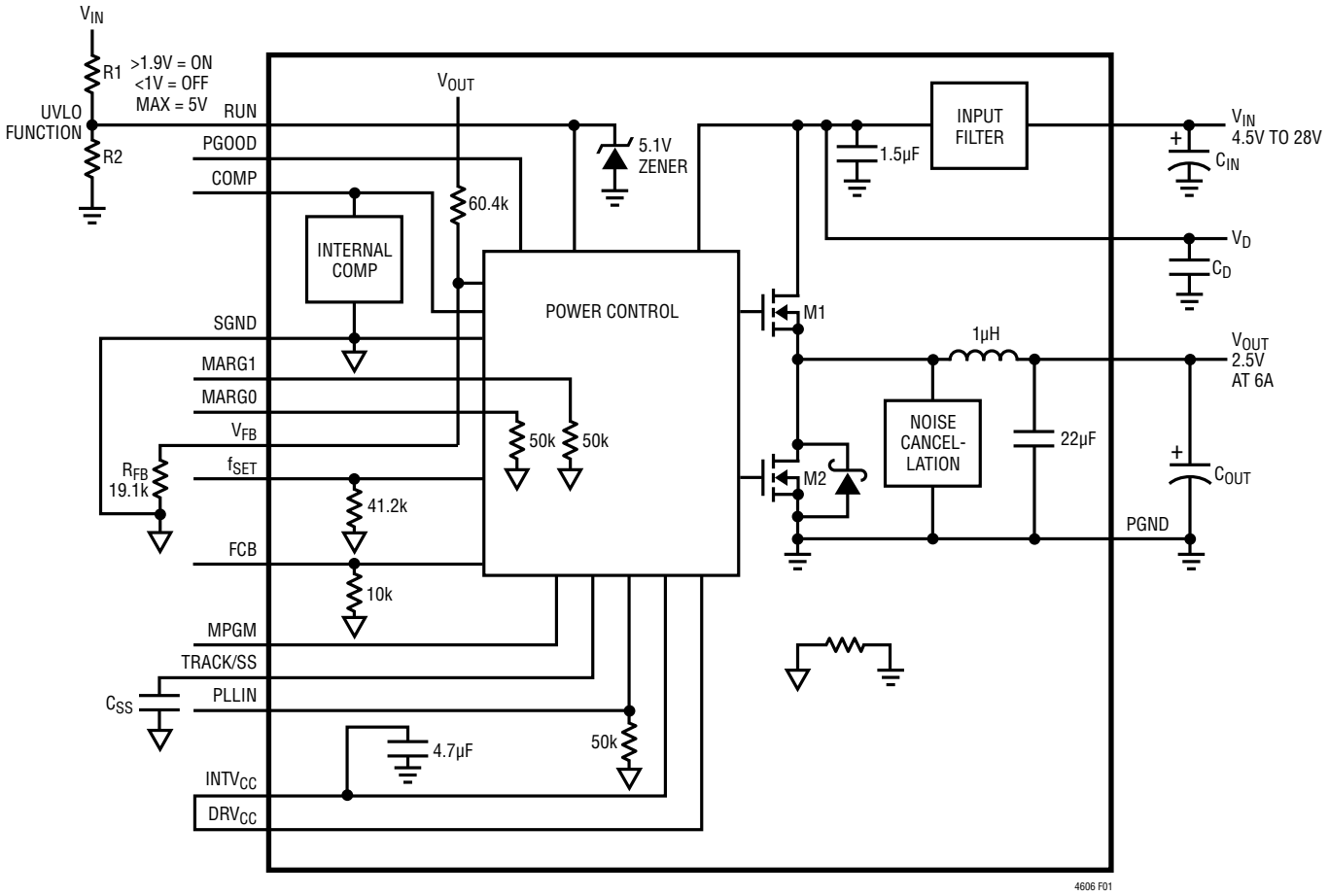


Figure 1. Simplified Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 28V, V_{OUT} = 2.5V)	I_{OUT} = 6A		10			µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.5V to 28V, V_{OUT} = 2.5V)	I_{OUT} = 6A		100	200		µF

OPERATION

Power Module Description

The LTM4606 is a standalone non-isolated switching mode DC/DC power supply. It can deliver up to 6A of DC output current with some external input and output capacitors. This module provides precisely regulated output voltage programmable via one external resistor from $0.6V_{DC}$ to $5.0V_{DC}$ over a 4.5V to 28V input voltage range. The typical application schematic is shown in Figure 20.

The LTM4606 has an integrated constant on-time current mode regulator, ultralow $R_{DS(ON)}$ FETs with fast switching speed and integrated Schottky diodes. With current mode control and internal feedback loop compensation, the LTM4606 module has sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limiting. Besides, foldback current limiting is provided in an overcurrent condition while V_{FB} drops. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET M1 is turned off and bottom FET M2 is turned on and held on until the overvoltage condition clears.

Input filter and noise cancellation circuits reduce the noise coupling to I/O sides, and ensure the electromagnetic interference (EMI) to meet EN55022 Class B limits.

Pulling the RUN pin below 1V forces the controller into its shutdown state, turning off both M1 and M2. At low load currents, discontinuous mode (DCM) operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by setting the FCB pin higher than 0.6V.

When the DRV_{CC} pin is connected to $INTV_{CC}$ an integrated 5V linear regulator powers the internal gate drivers. If a 5V external bias supply is applied on the DRV_{CC} pin, then an efficiency improvement will occur due to the reduced power loss in the internal linear regulator. This is especially true at the higher input voltage range.

The MPGM, MARG0 and MARG1 pins are used to support voltage margining, where the percentage of margin is programmed by the MPGM pin, and the MARG0 and MARG1 selected margining. The PLLIN pin provides frequency synchronization of the device to an external clock. The TRACK/SS pin is used for power supply tracking and soft-start programming.

APPLICATIONS INFORMATION

The typical LTM4606 application circuit is shown in Figure 20. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 2 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

Under the default frequency, there are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. These constraints are caused by the limitation of the minimum on and off time in the internal switches. Refer to the Frequency Adjustment section to change the switching frequency and get wider input and output ranges. See the Thermal Considerations and Output Current Derating section in this data sheet for the current restrictions.

Output Voltage Programming and Margining

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects the V_{OUT} and V_{FB} pins together. Adding a resistor R_{FB} from the V_{FB} pin to the SGND pin programs the output voltage:

$$V_{OUT} = 0.6V\frac{60.4k + R_{FB}}{R_{FB}} \text{ or equivalently,}$$

$$R_{FB} = \frac{60.4k}{\frac{V_{OUT}}{0.6V} - 1}$$

Table 1. R_{FB} Standard 1% Resistor Values vs V_{OUT}

R_{FB} (kΩ)	Open	60.4	40.2	30.1	25.5	19.1	13.3	8.25
V_{OUT} (V)	0.6	1.2	1.5	1.8	2	2.5	3.3	5

The MPGM pin programs a current that when multiplied by an internal 10k resistor sets up the 0.6V reference ± offset for margining. A 1.18V reference divided by the R_{PGM} resistor on the MPGM pin programs the current. Calculate $V_{OUT(MARGIN)}$:

$$V_{OUT(MARGIN)} = \frac{\%V_{OUT}}{100} \bullet V_{OUT}$$

where $\%V_{OUT}$ is the percentage of V_{OUT} you want to margin, and $V_{OUT(MARGIN)}$ is the margin quantity in volts:

$$R_{PGM} = \frac{V_{OUT}}{0.6V} \bullet \frac{1.18V}{V_{OUT(MARGIN)}} \bullet 10k$$

where R_{PGM} is the resistor value to place on the MPGM pin to ground.

The margining voltage, $V_{OUT(MARGIN)}$, will be added or subtracted from the nominal output voltage as determined by the state of the MARG0 and MARG1 pins. See the truth table below:

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

Input Capacitors and Input EMI Noise Attenuation

The LTM4606 is designed to achieve low input conducted EMI noise due to the fast switching of turn-on and turn-off. In the LTM4606, a high frequency inductor is integrated to the input line for noise attenuation. V_D and V_{IN} pins are available for external input capacitors to form a high frequency π filter. As shown in Figure 19, the ceramic capacitor C1 on the V_D pins is used to handle most of the RMS current into the converter, so careful attention is needed for capacitor C1 selection.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

APPLICATIONS INFORMATION

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η is the estimated efficiency of the power module. Note the capacitor ripple current ratings are often based on temperature and hours of life. This makes it advisable to properly derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always contact the capacitor manufacturer for derating requirements.

In a typical 6A output application, one or two very low ESR X5R or X7R, 10µF ceramic capacitors are recommended for C1. This decoupling capacitor should be placed directly adjacent to the module V_D pins in the PCB layout to minimize the trace inductance and high frequency AC noise. Each 10µF ceramic is typically good for 2 to 3 amps of RMS ripple current. Refer to your ceramics capacitor catalog for the RMS current ratings.

To attenuate high frequency noise, extra input capacitors should be connected to the V_{IN} pads and placed before the high frequency inductor to form the π filter. One of these low ESR ceramic capacitors is recommended to be placed close to the connection into the system board. A large bulk 100µF capacitor is only needed if the input source impedance is compromised by long inductive leads or traces. Figure 2 shows the radiated EMI test results to meet EN55022 Class B. For different applications, input capacitance may be varied to meet different radiated EMI limits.

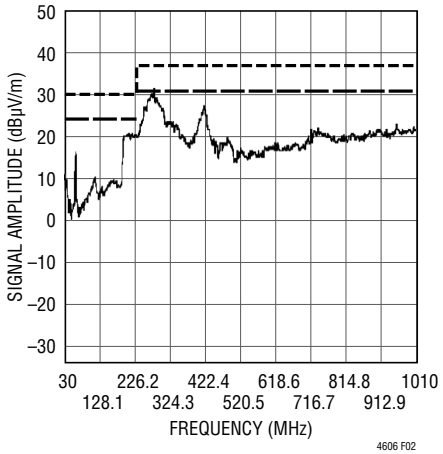


Figure 2. Radiated Emission Scan with $12V_{IN}$ to $2.5V_{OUT}$ at 6A (1×100µF X7R Ceramic C_{OUT})

Output Capacitors

The LTM4606 is designed for low output voltage ripple. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor. The typical capacitance is 200µF if all ceramic output capacitors are used. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. Table 2 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 3A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to maximize transient performance.

Multiphase operation with multiple LTM4606 devices in parallel will lower the effective output ripple current due to the phase interleaving operation. Refer to Figure 3 for the normalized output ripple current versus the duty cycle. Figure 3 provides a ratio of peak-to-peak output ripple current to the inductor ripple current as functions of duty cycle and the number of paralleled phases. Pick the corresponding duty cycle and the number of phases to get the correct output ripple current value. For example, each phase's inductor ripple current DIr at zero duty cycle is ~2.5A for a 12V to 2.5V design. The duty cycle is about 0.21. The 2-phase curve has a ratio of ~0.58 for a duty cycle of 0.21. This 0.58 ratio of output ripple current to the inductor ripple current DIr at 2.5A equals ~1.5A of the output ripple current (ΔI_L).

The output ripple voltage has two components that are related to the amount of bulk capacitance and effective series resistance (ESR) of the output bulk capacitance. The equation is:

$$\Delta V_{OUT(P-P)} \approx \left(\frac{\Delta I_L}{8 \bullet f \bullet N \bullet C_{OUT}} \right) + ESR \bullet \Delta I_L$$

where f is the frequency and N is the number of paralleled phases.

APPLICATIONS INFORMATION

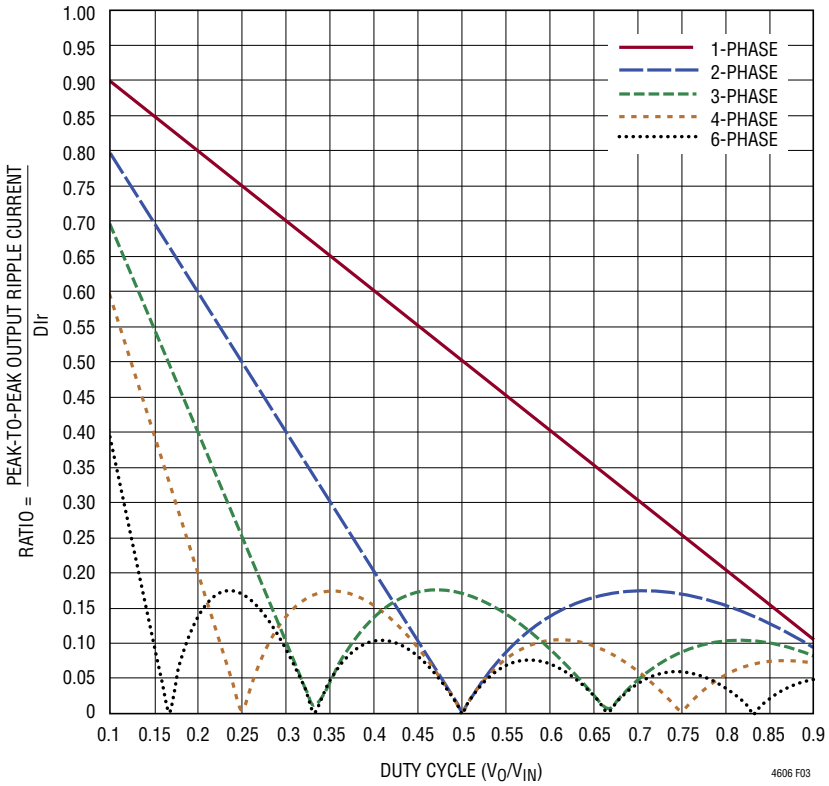


Figure 3. Normalized Output Ripple Current vs Duty Cycle, DIr = $V_O T/L_I$

Fault Conditions: Current Limit and Overcurrent Foldback

LTM4606 has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

To further limit current in the event of an overload condition, the LTM4606 provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to about one sixth of its full current limit value.

Soft-Start and Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on this pin will program the ramp rate of the output voltage. A 1.5µA current source will charge up the external soft-start capacitor to 80% of the 0.6V internal voltage reference plus or minus any margin delta. This will control the ramp of the internal reference and the output voltage. The total soft-start time can be calculated as:

$$t_{SOFTSTART} \cong 0.8 \bullet \left(0.6V \pm V_{OUT(MARGIN)}\right) \bullet \frac{C_{SS}}{1.5\mu A}$$

When the RUN pin falls below 1.5V, then the TRACK/SS pin is reset to allow for proper soft-start control when the regulator is enabled again. Current foldback and forced continuous mode are disabled during the soft-start process. The soft-start function can also be used to control the output ramp up time, so that another regulator can be easily tracked to it.

APPLICATIONS INFORMATION

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 4 shows an example of coincident tracking where the master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider. Ratiometric modes of tracking can be achieved by selecting different resistor values to change the output tracking ratio. The master output must be greater than the slave output for the tracking to work. Figure 5 shows the coincident output tracking characteristics.

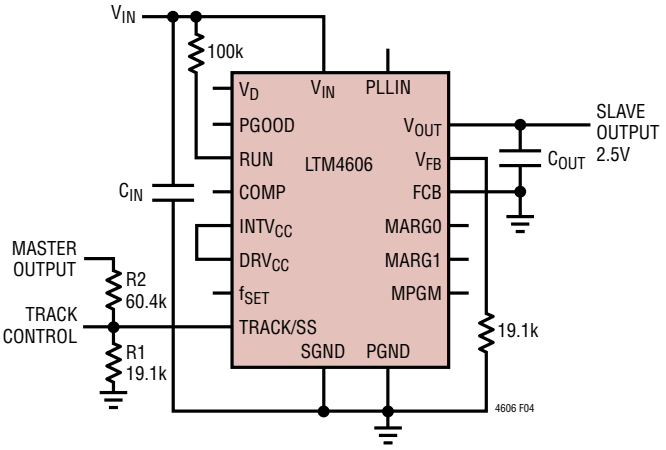


Figure 4. Coincident Tracking Schematic

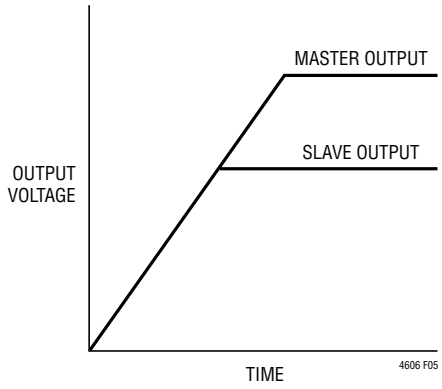


Figure 5. Coincident Output Tracking Characteristics

Run Enable

The RUN pin is used to enable the power module. The pin has an internal 5.1V Zener to ground. The pin can be driven with a logic input not to exceed 5V.

The RUN pin can also be used as an undervoltage lock out (UVLO) function by connecting a resistor divider from the input supply to the RUN pin:

$$V_{UVLO} = \frac{R1+R2}{R2} \bullet 1.5V$$

See Figure 1, Simplified Block Diagram.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point and tracks with margining.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for most output voltages. Table 2 is provided for most application requirements. LTpowerCAD® is available for other control loop optimization.

FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.6V threshold enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. FCB pin below the 0.6V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintain low output ripple.

APPLICATIONS INFORMATION

PLLIN

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of the external clock. The frequency range is ±30% around the operating frequency. A pulse detection circuit is used to detect a clock on the PLLIN pin to turn on the phase lock loop. The pulse width of the clock has to be at least 400ns and the amplitude at least 2V. The PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. During the start-up of the regulator, the phase-locked loop function is disabled.

$INTV_{CC}$ and DRV_{CC} Connection

An internal low dropout regulator produces an internal 5V supply that powers the control circuitry and DRV_{CC} for driving the internal power MOSFETs. Therefore, if the system does not have a 5V power rail, the LTM4606 can be directly powered by V_{IN}. The gate driver current through the LDO is about 20mA. The internal LDO power dissipation can be calculated as:

$$P_{LDO\_LOSS} = 20mA \bullet (V_{IN} - 5V)$$

The LTM4606 also provides an external gate driver voltage pin DRV_{CC}. If there is a 5V rail in the system, it is recommended to connect DRV_{CC} pin to the external 5V rail. This is especially true for higher input voltages. Do not apply more than 6V to the DRV_{CC} pin. A 5V output can be used to power the DRV_{CC} pin with an external circuit as shown in Figure 18.

Parallel Operation of the Module

The LTM4606 device is an inherently current mode controlled device. Parallel modules will have very good current sharing. This will balance the thermals on the design. The voltage feedback equation changes with the variable N as modules are paralleled:

$$V_{OUT} = 0.6V \frac{\frac{60.4k}{N} + R_{FB}}{R_{FB}}$$

N is the number of paralleled modules.

Thermal Considerations and Output Current Derating

In different applications, LTM4606 operates in a variety of thermal environments. The maximum output current is limited by the environment thermal condition. Sufficient cooling should be provided to help ensure reliable operation. When the cooling is limited, proper output current derating is necessary, considering ambient temperature, airflow, input/output condition, and the need for increased reliability.

The power loss curves in Figures 6 and 7 can be used in coordination with the load current derating curves in Figures 8 to 15 for calculating an approximate θ_{JA} for the module. The graphs delineate between no heat sink, and a BGA heat sink. Each of the load current derating curves will lower the maximum load current as a function of the increased ambient temperature to keep the maximum junction temperature of the power module at 125°C maximum. Each of the derating curves and the power loss curve that corresponds to the correct output voltage can be used to solve for the approximate θ_{JA} of the condition. Each figure has three curves that are taken at three different air flow conditions. Table 3 and Table 4 provide the approximate θ_{JA} for Figures 8 to 15. A complete explanation of the thermal characteristics is provided in the thermal Application Note AN110.

Safety Considerations

The LTM4606 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Radiated EMI Noise

High radiated EMI noise is a disadvantage for switching regulators by nature. Fast switching turn-on and turn-off make large di/dt change in the converters, which act as the radiation sources in most systems. The LTM4606 integrates the feature to minimize the radiated EMI noise for applications with low noise requirements. Optimized gate driver for the MOSFET and noise cancellation network are installed inside the LTM4606 to achieve low radiated EMI noise. Figure 16 shows a typical example for LTM4606 to meet the Class B of EN55022 radiated emission limit.

APPLICATIONS INFORMATION

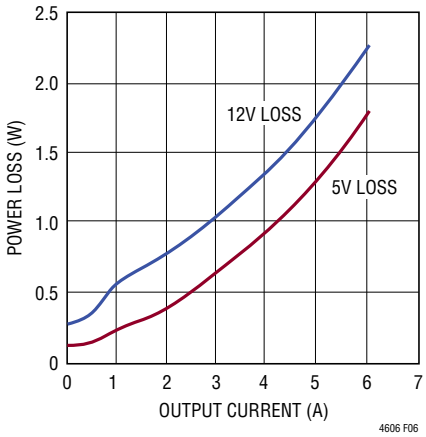


Figure 6. 1.5V Power Loss

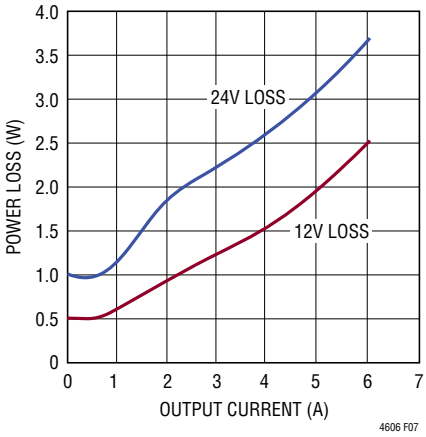


Figure 7. 3.3V Power Loss

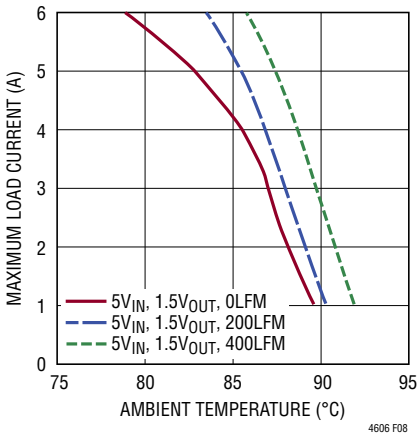


Figure 8. No Heat Sink

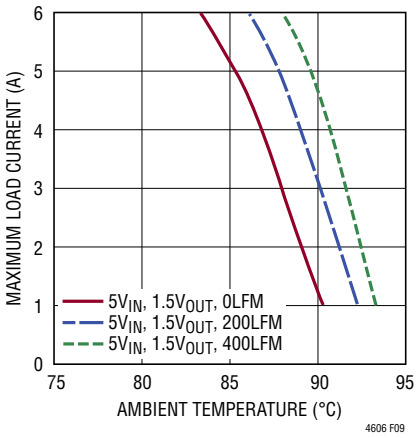


Figure 9. BGA Heat Sink

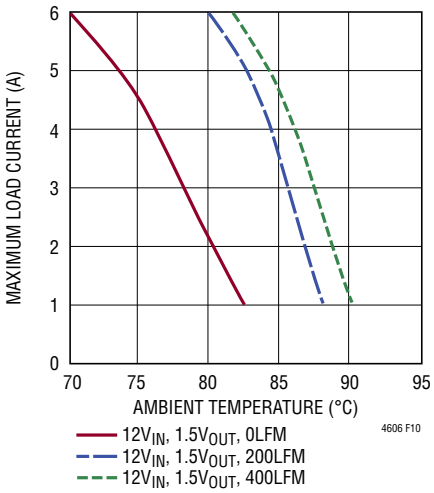


Figure 10. No Heat Sink

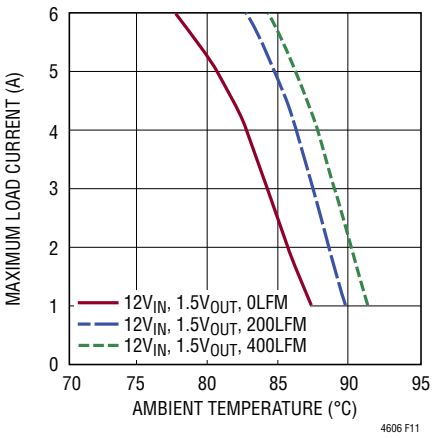


Figure 11. BGA Heat Sink

APPLICATIONS INFORMATION

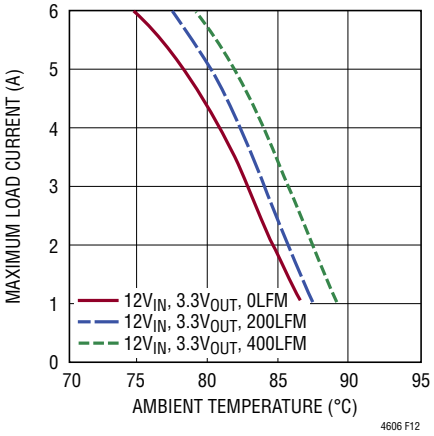


Figure 12. No Heat Sink

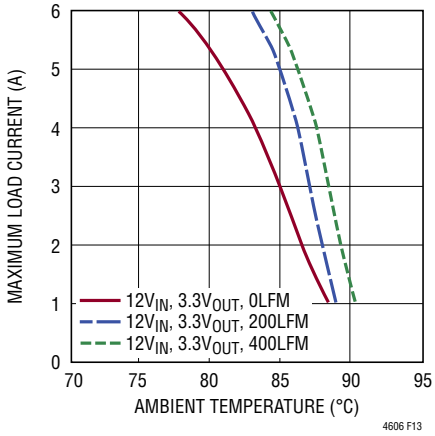


Figure 13. BGA Heat Sink

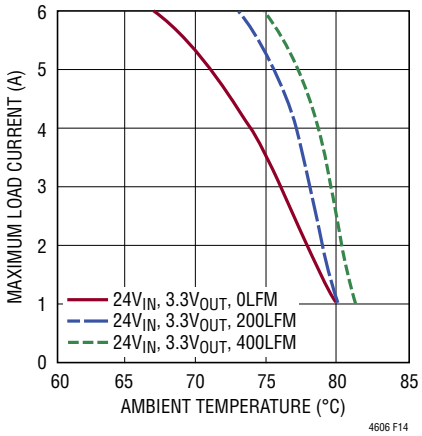


Figure 14. No Heat Sink

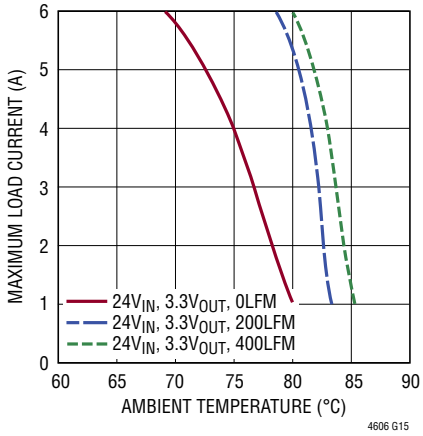


Figure 15. BGA Heat Sink

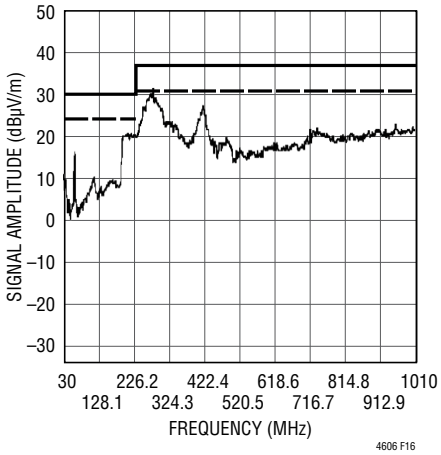


Figure 16. Radiated Emission Scan with $12V_{IN}$ to $2.5V_{OUT}$ at 6A (1×100µF X7R Ceramic C_{OUT})

APPLICATIONS INFORMATION

Table 2. Output Voltage Response vs Component Matrix (Refer to Figure 20)

TYPICAL MEASURED VALUES

C_{OUT1} VENDORS	PART NUMBER	C_{OUT2} VENDORS	PART NUMBER
TAIYO YUDEN	JMK316BJ226ML-T501 (22µF, 6.3V)	SANYO POSCAP	6TPE220MIL (220µF, 6.3V)
TAIYO YUDEN	JMK325BJ476MM-T (47µF, 6.3V)	SANYO POSCAP	2R5TPE330M9 (330µF, 2.5V)
TDK	C3225X5R0J476M (47µF, 6.3V)	SANYO POSCAP	4TPE330MCL (330µF, 4V)

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	V_{IN} (V)	DROOP (mV)	PEAK TO PEAK (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)
1.2	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	5	34	68	30	3	60.4
1.2	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	5	22	40	26	3	60.4
1.2	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	5	20	40	24	3	60.4
1.2	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	5	32	60	18	3	60.4
1.2	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	34	68	30	3	60.4
1.2	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	12	22	40	26	3	60.4
1.2	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	20	39	24	3	60.4
1.2	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	12	29.5	55	18	3	60.4
1.5	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	5	35	70	30	3	40.2
1.5	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	5	25	48	30	3	40.2
1.5	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	5	24	47.5	26	3	40.2
1.5	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	5	36	68	26	3	40.2
1.5	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	35	70	30	3	40.2
1.5	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	12	25	48	30	3	40.2
1.5	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	24	45	26	3	40.2
1.5	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	12	32.6	61.9	26	3	40.2
1.8	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	5	38	76	37	3	30.1
1.8	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	5	29.5	57.5	30	3	30.1
1.8	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	5	28	55	26	3	30.1
1.8	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	5	43	80	26	3	30.1
1.8	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	38	76	37	3	30.1
1.8	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	12	28	55	30	3	30.1
1.8	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	27	52	26	3	30.1
1.8	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	12	36.4	70	26	3	30.1
2.5	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	5	38	78	40	3	19.1
2.5	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 4V	5	37.6	74	34	3	19.1
2.5	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	5	39.5	78.1	28	3	19.1
2.5	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	5	66	119	12	3	19.1
2.5	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	38	78	40	3	19.1
2.5	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 4V	12	34.5	66.3	34	3	19.1
2.5	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	35.8	68.8	28	3	19.1
2.5	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	12	50	98	18	3	19.1
3.3	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	7	42	86	40	3	13.3
3.3	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 4V	7	47	89	32	3	13.3
3.3	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	7	50	94	28	3	13.3
3.3	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	7	75	141	14	3	13.3
3.3	2 × 10µF 35V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	42	86	40	3	13.3
3.3	2 × 10µF 35V	150µF 35V	1 × 47µF 6.3V	330µF 4V	12	47	88	32	3	13.3
3.3	2 × 10µF 35V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	50	94	28	3	13.3
3.3	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	12	69	131	22	3	13.3
5	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	12	110	215	20	3	8.25
5	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	15	110	215	20	3	8.25
5	2 × 10µF 35V	150µF 35V	4 × 47µF 6.3V	NONE	20	110	217	20	3	8.25

APPLICATIONS INFORMATION

Table 3. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 8, Figure 10	5, 12	Figure 6	0	None	13.5
Figure 8, Figure 10	5, 12	Figure 6	200	None	10
Figure 8, Figure 10	5, 12	Figure 6	400	None	9
Figure 9, Figure 11	5, 12	Figure 6	0	BGA Heat Sink	9.5
Figure 9, Figure 11	5, 12	Figure 6	200	BGA Heat Sink	7
Figure 9, Figure 11	5, 12	Figure 6	400	BGA Heat Sink	5

Table 4. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 12, Figure 14	12, 24	Figure 7	0	None	13.5
Figure 12, Figure 14	12, 24	Figure 7	200	None	11
Figure 12, Figure 14	12, 24	Figure 7	400	None	10
Figure 13, Figure 15	12, 24	Figure 7	0	BGA Heat Sink	10
Figure 13, Figure 15	12, 24	Figure 7	200	BGA Heat Sink	7
Figure 13, Figure 15	12, 24	Figure 7	400	BGA Heat Sink	5

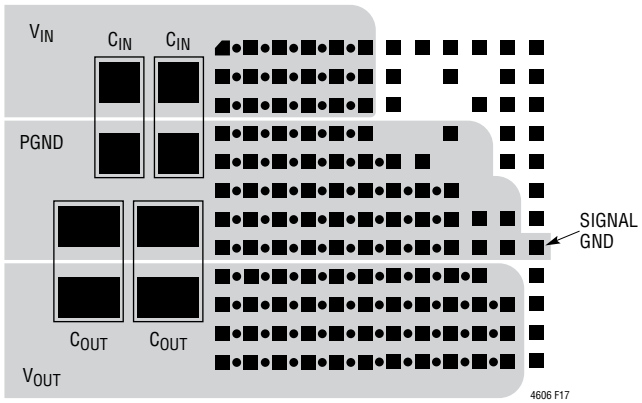
Heat Sink Manufacturer	PART NUMBER	WEBSITE
AAVID Thermalloy	375424B00034G	www.aavidthermalloy.com
Cool Innovations	4-050503P to 4-050508P	www.cooinnovations.com

Layout Checklist/Example

The high integration of LTM4606 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, PGND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_D, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- Use round corners for the PCB copper layer to minimize the radiated noise.
- To minimize the EMI noise and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers on different locations.
- Do not put vias directly on pads, unless they are capped.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.
- Place one or more high frequency ceramic capacitors close to the connection into the system board.

Figure 17 gives a good example of the recommended layout.



(LGA Shown, for BGA Use Circle Pads)

Figure 17. Recommended PCB Layout

APPLICATIONS INFORMATION

Frequency Adjustment

The LTM4606 is designed to typically operate at 800kHz across most input conditions. The f_{SET} pin is typically left open. The switching frequency has been optimized for maintaining constant output ripple noise over most operating ranges. The 800kHz switching frequency and the 400ns minimum off time can limit operation at higher duty cycles like 5V to 3.3V, and produce excessive inductor ripple currents for lower duty cycle applications like 28V to 5V.

Example for 5V Output

LTM4606 minimum on-time = 100ns
$t_{ON} = ((V_{OUT} \bullet 10pF)/I_{fSET})$, for $V_{OUT} > 4.8V$ use 4.8V

LTM4606 minimum off-time = 400ns
$t_{OFF} = t - t_{ON}$, where t = 1/Frequency

Duty Cycle = t_{ON}/t or V_{OUT}/V_{IN}

Equations for setting frequency:

$I_{fSET} = (V_{IN}/(3 \bullet R_{fSET}))$, where the internal R_{fSET} is 41.2k. For 28V input operation, $I_{fSET} = 227\mu A$. $t_{ON} = ((4.8 \bullet 10pF)/I_{fSET})$, $t_{ON} = 211ns$. Frequency = $(V_{OUT}/(V_{IN} \bullet t_{ON}))$ = (5V/(28 • 211ns)) ~ 850kHz. The inductor ripple current begins to get high at the higher input voltages due to a larger voltage across the inductor. The current ripple is ~5A at 20% duty cycle for the integrated 1µH inductor. The inductor ripple current can be lowered at the higher input voltages by adding an external resistor from f_{SET} to ground to increase the switching frequency. A 4A ripple current is chosen, and the total peak current is equal to 1/2 of the 4A ripple current plus the output current. For 5V output, current is limited to 5A, so the total peak current is less than 7A. This is below the 8A peak specified value. A 150k resistor is placed from f_{SET} to ground, and the parallel combination of 150k and 41.2k equates to 32.3k. The I_{fSET} calculation with 32.3k and 28V input voltage equals 289µA. This equates to a t_{ON} of 166ns. This will increase the switching frequency from 850kHz to ~1MHz for the 28V to 5V conversion. The minimum on time is above 100ns at 28V input. Since the switching frequency is approximately constant over input and output conditions, then the lower input voltage range is limited to 8V for the 1MHz operation due to the 400ns minimum off time. Equation: $t_{ON} = (V_{OUT}/V_{IN}) \bullet (1/\text{Frequency})$ equates to a 375ns on time, and a 400ns off time. Figure 18 shows an operating range of 10V to 28V for 1MHz operation with a 150k resistor to ground, and an 8V to 16V operating range for f_{SET} floating. These modifications are made to provide wider input voltage ranges for the 5V output designs while limiting the inductor ripple current, and maintaining the 400ns minimum off-time.

Example for 3.3V Output

LTM4606 minimum on-time = 100ns
$t_{ON} = ((V_{OUT} \bullet 10pF)/I_{fSET})$

LTM4606 minimum off-time = 400ns
$t_{OFF} = t - t_{ON}$, where t = 1/Frequency

Duty Cycle (DC) = t_{ON}/t or V_{OUT}/V_{IN}

Equations for setting frequency:

$I_{fSET} = (V_{IN}/(3 \bullet R_{fSET}))$, for 28V input operation, I_{fSET} = 227µA, $t_{ON} = ((3.3 \bullet 10pF)/I_{fSET})$, $t_{ON} = 145ns$, where the internal R_{fSET} is 41.2k. Frequency = $(V_{OUT}/(V_{IN} \bullet t_{ON}))$ = (3.3V/(28 • 145ns)) ~ 810kHz. The minimum on-time and minimum-off time are within specification at 146ns and 1089ns. But the 4.5V minimum input for converting 3.3V output will not meet the minimum off-time specification of 400ns. $t_{ON} = 905ns$, Frequency = 810kHz, $t_{OFF} = 329ns$.

Solution

Lower the switching frequency at lower input voltages to allow for higher duty cycles, and meet the 400ns minimum off-time at 4.5V input voltage. The off-time should be about 500ns with 100ns guard band. The duty cycle for (3.3V/4.5V) = ~73%. Frequency = $(1 - DC)/t_{OFF}$ or (1 – 0.73)/500ns = 540kHz. The switching frequency needs to be lowered to 540kHz at 4.5V input. t_{ON} = DC/frequency, or 1.35µs. The f_{SET} pin voltage compliance is 1/3 of V_{IN}, and the I_{fSET} current equates to 36µA with the internal 41.2k. The I_{fSET} current needs to be 24µA for 540kHz operation. A resistor can be placed from V_{OUT} to f_{SET} to lower the effective I_{fSET} current out of the f_{SET} pin to 24µA. The f_{SET} pin is 4.5V/3 =1.5V and V_{OUT} = 3.3V, therefore a 150k resistor will source 12µA into the f_{SET} node and lower the I_{fSET} current to 24µA. This enables the 540kHz operation and the 4.5V to 28V input operation for down converting to 3.3V output as shown in Figure 19. The frequency will scale from 540kHz to 950kHz over this input range. This provides for an effective output current of 5A over the input range.

TYPICAL APPLICATIONS

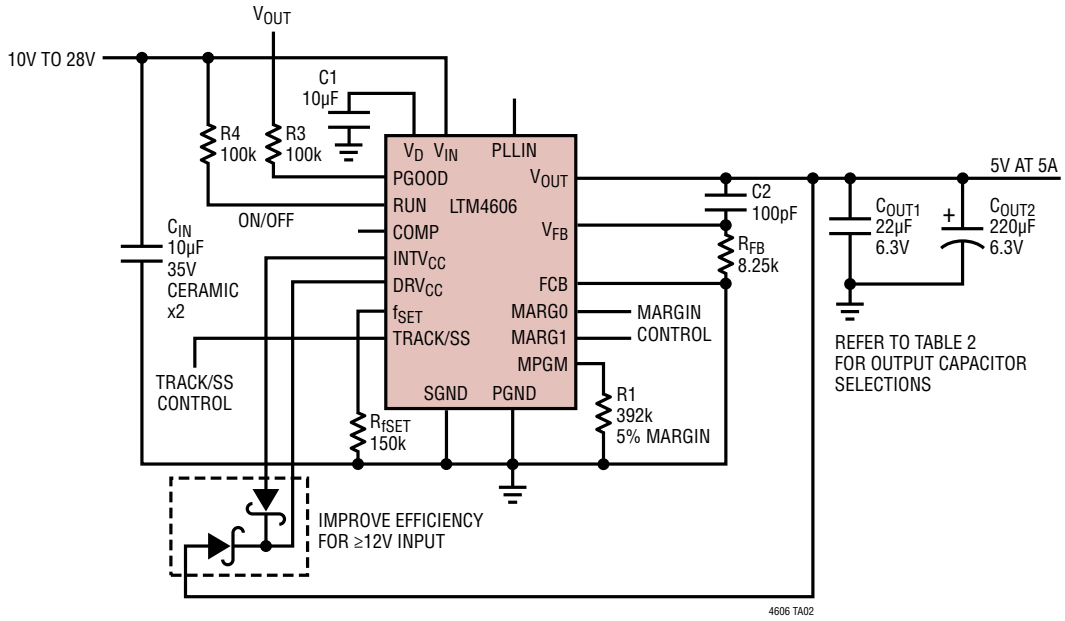


Figure 18. 10V to 28V_{IN}, 5V at 5A Design

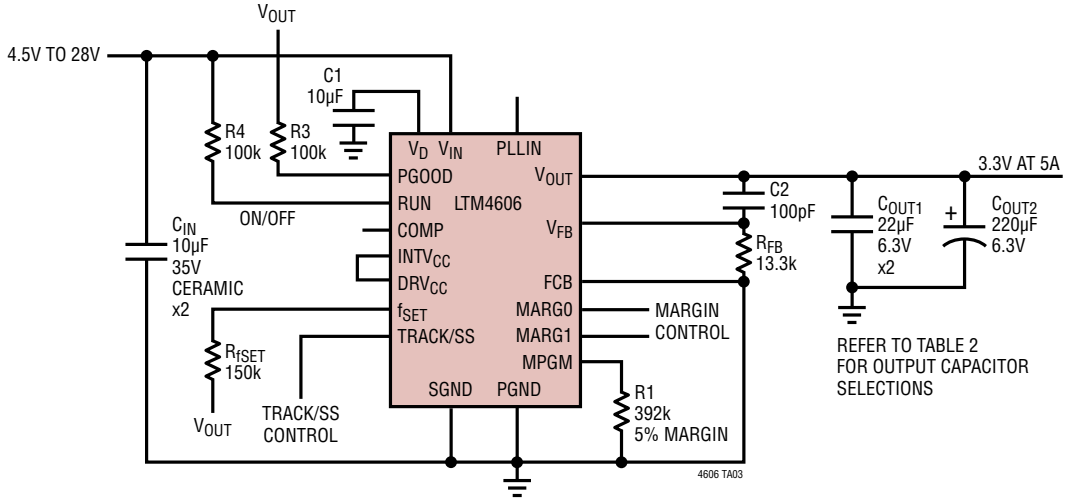


Figure 19. 3.3V at 5A Design

TYPICAL APPLICATIONS

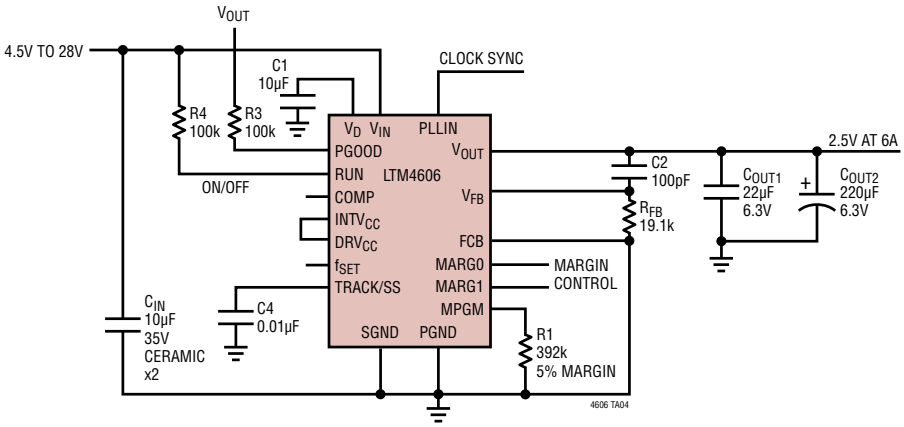


Figure 20. Typical 4.5V to 28V_{IN}, 2.5V at 6A Design

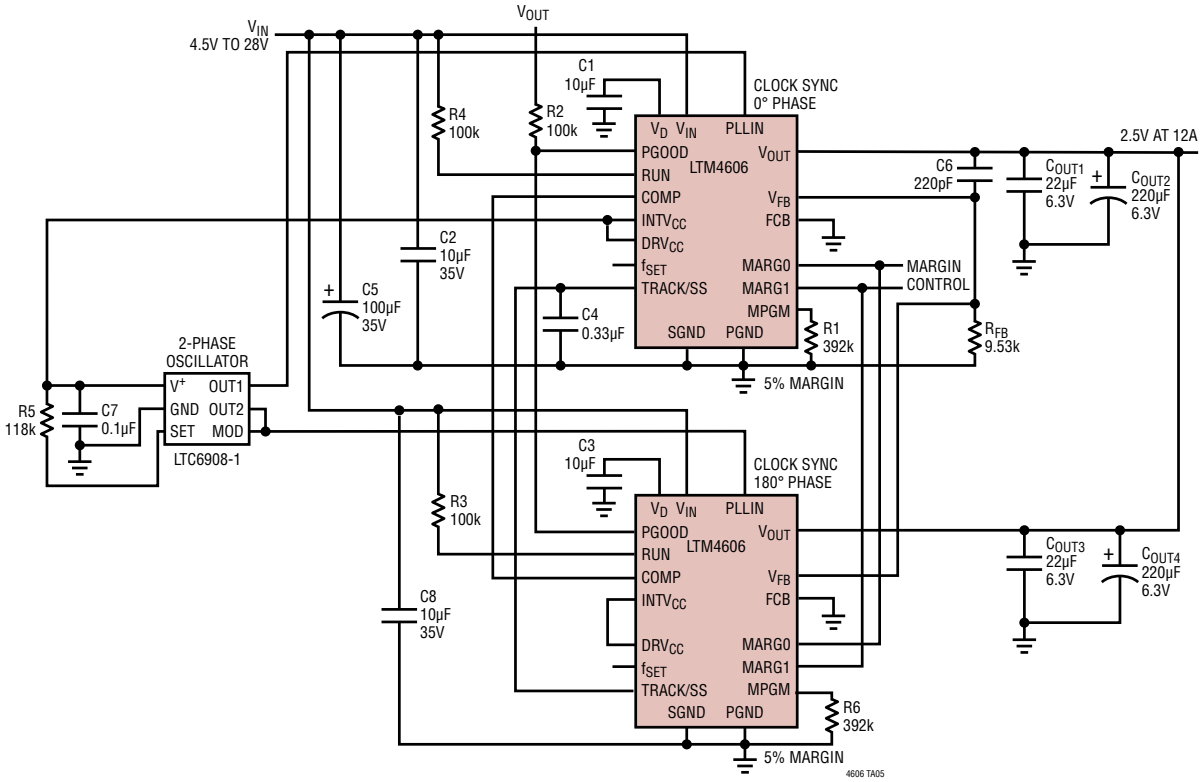


Figure 21. 2-Phase, Parallel 2.5V at 12A Design

TYPICAL APPLICATIONS

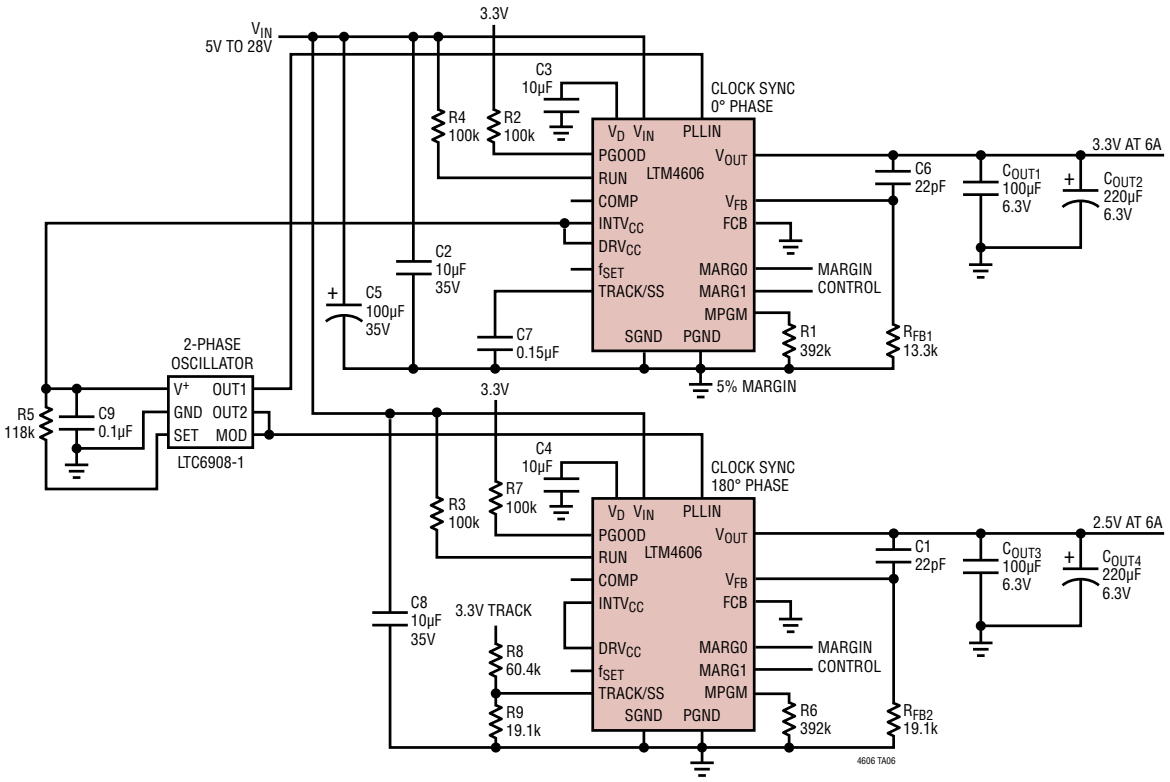


Figure 22. 2-Phase, 3.3V and 2.5V Outputs at 6A with Tracking and Margining

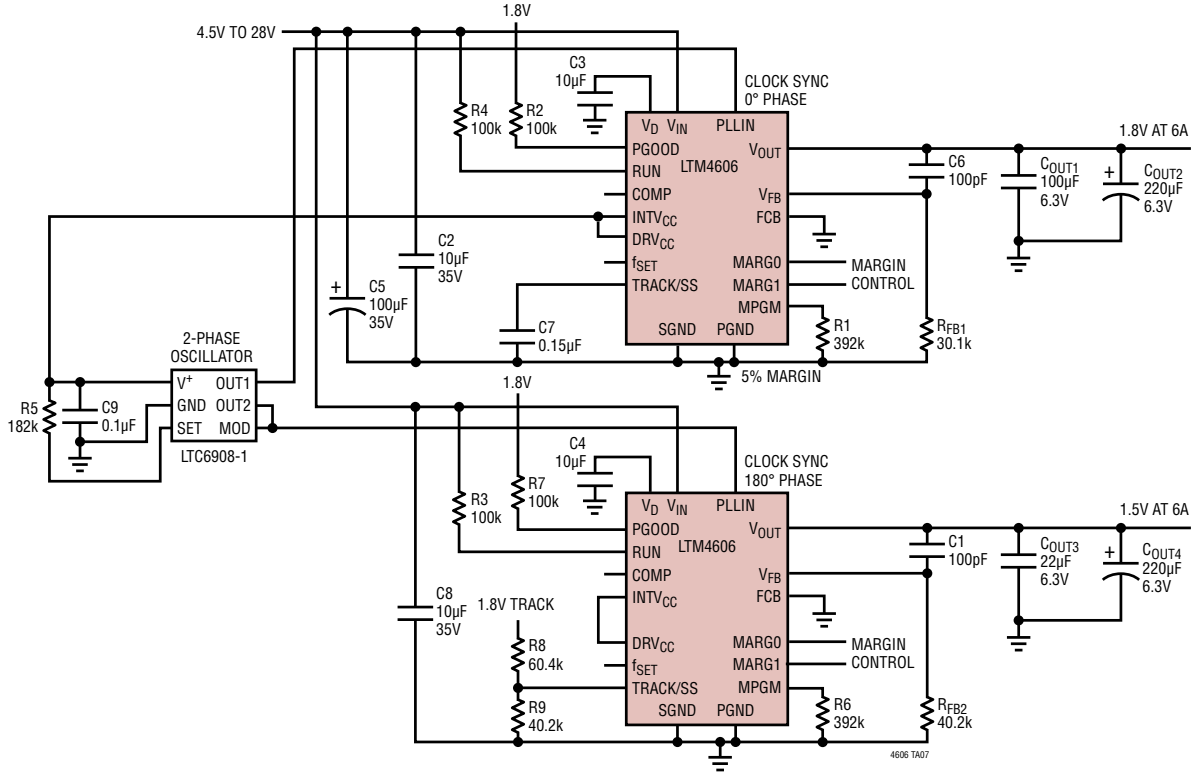


Figure 23. 2-Phase, 1.8V and 1.5V Outputs at 6A with Tracking and Margining

PACKAGE DESCRIPTION

Pin Assignment Tables
(Arranged by Pin Function)

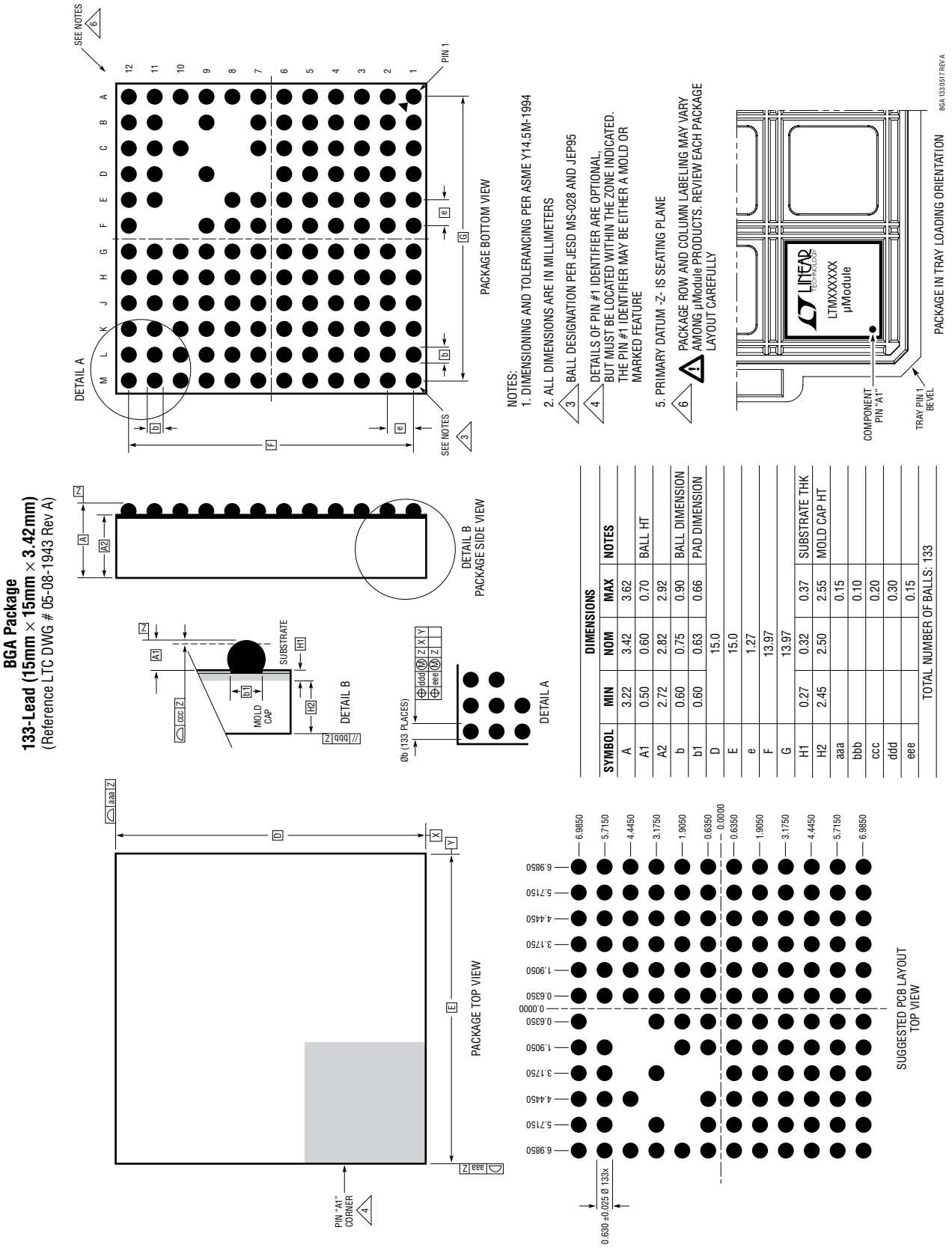
PIN NAME	
A1	V_{IN}
A2	V_{IN}
A3	V_{IN}
A4	V_{IN}
A5	V_{IN}
A6	V_{IN}
B1	V_{IN}
B2	V_{IN}
B3	V_{IN}
B4	V_{IN}
B5	V_{IN}
B6	V_{IN}
C1	V_{IN}
C2	V_{IN}
C3	V_{IN}
C4	V_{IN}
C5	V_{IN}
C6	V_{IN}

PIN NAME	
D1	PGND
D2	PGND
D3	PGND
D4	PGND
D5	PGND
D6	PGND
E1	PGND
E2	PGND
E3	PGND
E4	PGND
E5	PGND
E6	PGND
E7	PGND
E8	PGND
F1	PGND
F2	PGND
F3	PGND
F4	PGND
F5	PGND
F6	PGND
F7	PGND
F8	PGND
F9	PGND
G1	PGND
G2	PGND
G3	PGND
G4	PGND
G5	PGND
G6	PGND
G7	PGND
G8	PGND
G9	PGND
G10	PGND
G11	PGND
H1	PGND
H2	PGND
H3	PGND
H4	PGND
H5	PGND
H6	PGND
H7	PGND
H8	PGND
H9	PGND
H10	PGND
H11	PGND

PIN NAME	
J1	V_{OUT}
J2	V_{OUT}
J3	V_{OUT}
J4	V_{OUT}
J5	V_{OUT}
J6	V_{OUT}
J7	V_{OUT}
J8	V_{OUT}
J9	V_{OUT}
J10	V_{OUT}
J11	V_{OUT}
K1	V_{OUT}
K2	V_{OUT}
K3	V_{OUT}
K4	V_{OUT}
K5	V_{OUT}
K6	V_{OUT}
K7	V_{OUT}
K8	V_{OUT}
K9	V_{OUT}
K10	V_{OUT}
K11	V_{OUT}
L1	V_{OUT}
L2	V_{OUT}
L3	V_{OUT}
L4	V_{OUT}
L5	V_{OUT}
L6	V_{OUT}
L7	V_{OUT}
L8	V_{OUT}
L9	V_{OUT}
L10	V_{OUT}
L11	V_{OUT}
M1	V_{OUT}
M2	V_{OUT}
M3	V_{OUT}
M4	V_{OUT}
M5	V_{OUT}
M6	V_{OUT}
M7	V_{OUT}
M8	V_{OUT}
M9	V_{OUT}
M10	V_{OUT}
M11	V_{OUT}

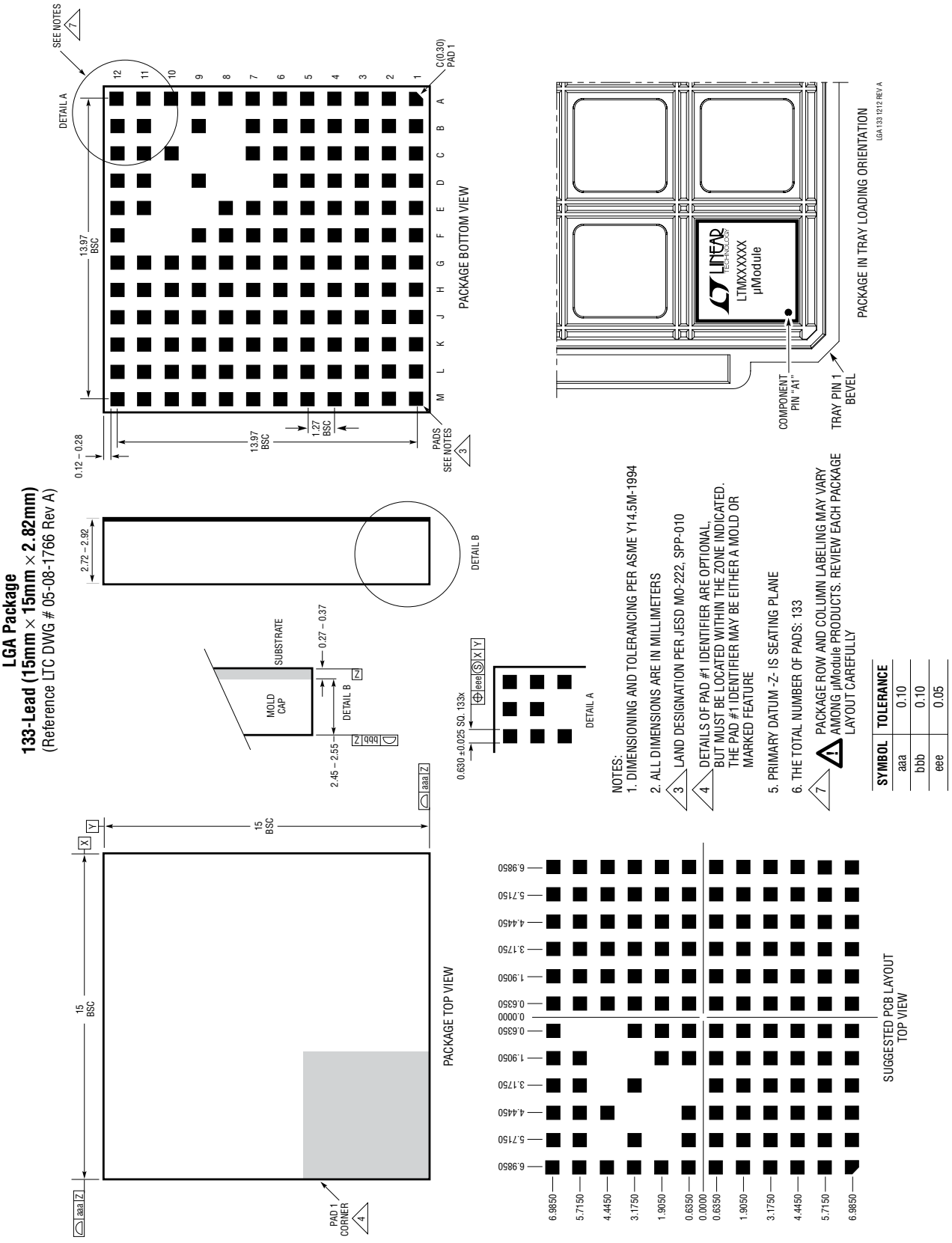
PIN NAME	
A7	$INTV_{CC}$
A8	PLLIN
A9	TRACK/SS
A10	RUN
A11	COMP
A12	MPGM
B7	V_D
B8	-
B9	RUN
B10	-
B11	MPGM
B12	f_{SET}
C7	V_D
C8	-
C9	-
C10	DRV_{CC}
C11	MARG1
C12	MARG0
D7	-
D8	-
D9	SGND
D10	-
D11	COMP
D12	MARG1
E9	-
E10	-
E11	DRV_{CC}
E12	DRV_{CC}
F10	-
F11	-
F12	V_{FB}
G12	PGOOD
H12	SGND
J12	NC
K12	NC
L12	NC
M12	FCB

PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	BALL HT
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.0		
E		15.0		
e		1.27		
F		13.97		
G		13.97		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	2.45	2.50	2.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 133				

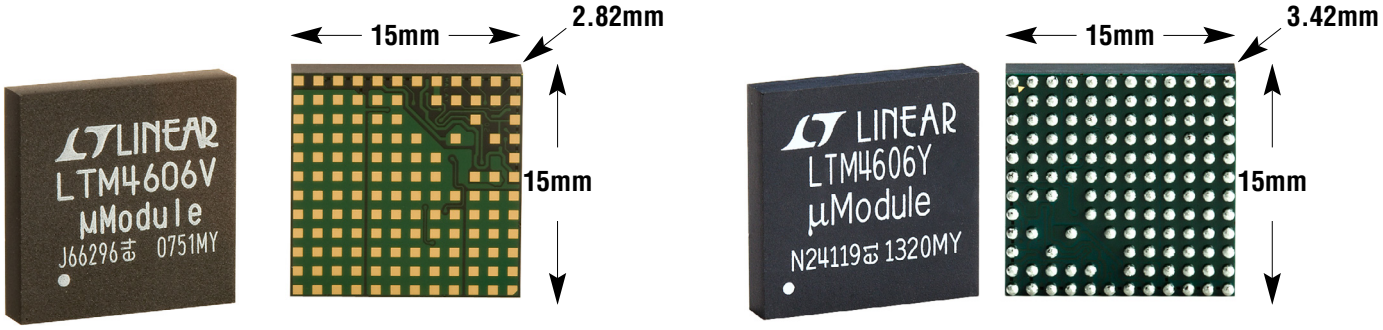
PACKAGE DESCRIPTION



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/10	Change to Features.	1
		Change to Absolute Maximum Ratings.	2
		Changes to Electrical Characteristics.	2, 3
		Changes to Related Parts.	25
B	3/11	Text updated throughout the data sheet.	1-28
		Graph replaced on the front page, Figure 2, and Figure 16.	1, 12, 17
		Added value of 1µH to inductor on Figure 1.	9
		Updated Related Parts.	28
C	10/13	Add BGA Package Option.	1, 2, 19, 25, 28
		Add Start Into Pre-Bias Output Graph.	6
		Clarify Voltage Margining function.	11
		Add Recommended External Heat Sink Vendors.	19
		Update LGA Package Outline Drawing.	26
D	2/14	Added SnPb package option.	1, 2
E	6/21	Added MPV to part marking.	2

PACKAGE PHOTOGRAPH



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4601/ LTM4601A	12A DC/DC µModule Regulator with PLL, Output Tracking/Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4601-1/LTM4601A-1 Version Has No Remote Sensing, LGA Package
LTM4618	6A DC/DC µModule Regulator with PLL, Output Tracking	4.5V ≤ V_{IN} ≤ 26.5V, 0.8V ≤ V_{OUT} ≤ 5V, Synchronizable, 9mm × 15mm × 4.3mm LGA Package
LTM4604A	Low V_{IN} 4A DC/DC µModule Regulator	2.375V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.3mm LGA Package
LTM4608A	Low V_{IN} 8A DC/DC µModule Regulator	2.375V ≤ V_{IN} ≤ 5.5V, 0.6V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.8mm LGA Package
LTM4612	Low Noise 5A, 15V_{OUT} DC/DC µModule Regulator	Low Noise, with PLL, Output Tracking and Margining, LTM4606 Pin-Compatible
LTM4613	Low Noise 8A, 15V_{OUT} DC/DC µModule Regulator	Low Noise, with PLL, Output Tracking and Margining, EN55022B Compliant
LTM4627	15A DC/DC µModule Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5V, ±1.5% Total DC Output Accuracy, 15mm × 15mm × 4.32mm LGA Package
EN55022 Class B Certified DC/DC µModule Regulators		
LTM8020	High V_{IN} 0.2A DC/DC Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 36V, 1.25V ≤ V_{OUT} ≤ 5V, 6.25mm × 6.25mm × 2.3mm LGA Package
LTM8021	High V_{IN} 0.5A DC/DC Step-Down µModule Regulator	3V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 5V, 6.25mm × 11.25mm × 2.8mm LGA Package
LTM8022/ LTM8023	36V_{IN}, 1A and 2A DC/DC µModule Regulators	Pin Compatible, 4.5V ≤ V_{IN} ≤ 36V, 9mm × 11.25mm × 2.8mm LGA Package
LTM8031/ LTM8032	1A, 2A EMC DC/DC µModule Regulators	EN55022 Class B Compliant, 3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, Pin Compatible, 9mm × 15mm × 2.82mm LGA Package
LTM8033	3A EMC DC/DC µModule Regulator	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 24V, 11.25mm × 15mm × 4.32mm LGA Package