Micropower Ring Tone Generator

FEATURES

- **Allows Dynamic Control of Output Frequency, Cadence, Amplitude and DC Offset**
- **Active Tracking Supply Configuration Allows Linear Generation of Ring Tone Signal**
- **No High Voltage Post-Filtering Required**
- **Capacitive Isolation Eliminates Optocouplers**
- Low Distortion Output Meets International PTT Requirements
- Differential Input Signal for Noise Immunity
- User Adjustable Active Output Current Limit
- Powered Directly From High Voltage Ringer Supply—No Additional Supplies Necessary
- Supply Current: <1mA
- 2% Signal Amplitude Reference
- Available in 14-Pin SO and DIP Packages

APPLICATIONS

- Wireless Local Loop Telephones
- Key System/PBX Equipment
- Fiber to the Curb Telecom Equipment

DESCRIPTION

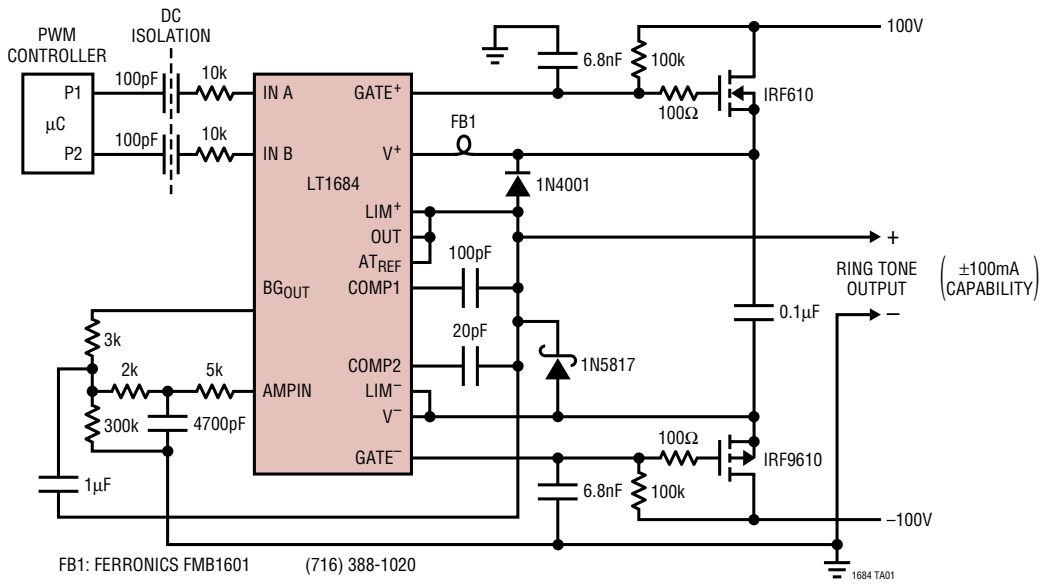
The LT®1684 is a telecommunication ring tone generator. The IC takes a user-generated pulse width modulated (PWM) input and converts it to a high voltage sine wave suitable for telephone ringing applications.

The LT1684 receives capacitor-isolated differential PWM input signals encoded with desired ring output cadence, frequency, and amplitude information. The LT1684 normalizes the pulse amplitude to ±1.25V for an accurate signal voltage reference. The cadence, frequency and amplitude information is extracted using a multiple-pole active filter/amplifier, producing the output ring tone signal.

The LT1684 uses its own ring tone output as a reference for generating local supply rails using complementary high voltage external MOSFETs as dynamic level-shifting devices. This “active tracking” supply mode of operation allows linear generation of the high voltage ring tone signal, reducing the need for large high voltage filtering elements.

TYPICAL APPLICATION

Electrically Isolated Ring Tone Generator



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltages:

Active Tracking Differential Voltage
(GATE$^+$ – GATE$^-$) ..... –0.3V to 42V
Local Supply Differential Voltage
(V^+ – V^-) ..... –0.3V to 36V
Local Supply
Voltage V^+ ..... (GATE$^+$ – 7.0V) to (GATE$^+$ + 0.3V)
Local Supply
Voltage V^- ..... (GATE$^-$ – 0.3V) to (GATE$^-$ + 7.0V)
PWM Input Differential Voltage
(IN A – IN B) ..... –7.0V to 7.0V
PWM Input Voltage
Common Mode ..... (V^- – 0.3V) to (V^+ + 0.3V)
LIM$^+$ Current Limit
Pin Voltage ..... (OUT – 0.3V) to (V^+ + 0.3V)
LIM$^-$ Current Limit
Pin Voltage ..... (V^- – 0.3V) to (OUT + 0.3V)
All Other Pin Voltages ..... (V^- – 0.3V) to (V^+ + 0.3V)

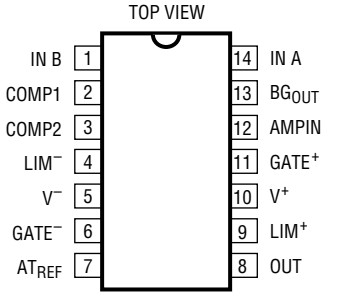
Currents:

LIM$^+$, LIM$^-$ Current ..... –350mA
OUT Current 350mA
BG_{OUT} Current ..... ±10mA
PWM (IN A, IN B) Current ..... ±5mA
GATE$^+$, GATE$^-$ Current ..... ±20mA
COMP1 Current ..... ±1mA
COMP2 Current ..... ±1mA
AT_{REF} Current ..... ±20mA

Temperatures:

Operating Junction Temperature Range
Commercial Grade ..... 0°C to 125°C
Industrial Grade ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
14-LEAD PDIP

S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 75°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 115°C/W (S)

ORDER PART NUMBER
LT1684CN
LT1684CS
LT1684IN
LT1684IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V^+ – V^–$ = 20V, Voltages referenced to pin OUT, $V_{OUT} = V_{ATREF}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Protection							
I_S	DC Supply Current (Note 2)	IN A – IN B ≥ 1.6V	●		680	950	µA
$\|V^+\|$ $\|V^–\|$	Local Supply Voltages	$V_{GATE}+ \geq V^+$ $V_{GATE}– \leq V^–$	●	6.5	10		V
$V_{GATE}+$	Active Tracking Supply FET Bias Voltage	$I_{GATE}+ = –100µA$, AT_{REF} = 0V	●	13.2	14.0	14.8	V
$V_{GATE}–$	Active Tracking Supply FET Bias Voltage	$I_{GATE}– = 100µA$, AT_{REF} = 0V	●	–14.8	–14.0	–13.2	V
PWM Receiver							
f_{PWM}	Input Carrier Frequency				10		kHz
V_{IN}	Minimum Valid Differential Input	IN A – IN B or IN B – IN A	●	1.6			V
	Differential Input Threshold | IN A – IN B |		●	0.50	0.70	1.00	V
R_{IN}	Differential Input Overdrive Impedance (Note 3, 5)	$V_{IN} > V_{TH}$ + 100mV	●	7	10		kΩ
$R_{INA,INB}$	Single-Ended Input Impedance (Note 5)	To Pin OUT	●	50			kΩ
BG Buffer							
V_{BGOUT}	BG_{OUT} Normalized Voltage	Magnitude $\|V_{BGOUT}\|$	 ●	1.235 1.225	1.250 1.250	1.265 1.275	V V
$V_{BGOUTOS}$	Output Offset Voltage $[(V_{BGOUT}+) + (V_{BGOUT}–)]/2$		 ●	–7 –10		7 10	mV mV
$I_{BGOUTSC}$	BG_{OUT} Short-Circuit Current		●	±2	±4.5		mA
R_{BGOUT}	BG_{OUT} Output Impedance	$–2mA \leq I_{BGOUT} \leq 2mA$			0.2		Ω
t_r	BG_{OUT} Rise Time (10% to 90%)	R_{OUT} = 5k, C_{OUT} = 10pF	●		160	300	ns
t_f	BG_{OUT} Fall Time (10% to 90%)	R_{OUT} = 5k, C_{OUT} = 10pF	●		260	400	ns
Δt_{r-f}	BG_{OUT} RiseTime – Fall Time		●	–200	–100	0	ns
t_{pr}	BG_{OUT} Propagation Delay PWM Input Transition to 10% Output (Rising Edge)	R_{OUT} = 5k, C_{OUT} = 10pF	●		340	500	ns
t_{pf}	BG_{OUT} Propagation Delay PWM Input Transition to 90% Output (Falling Edge)	R_{OUT} = 5k, C_{OUT} = 10pF	●		440	600	ns
Δt_p	BG_{OUT} Propagation Delay Rising Edge – Falling Edge		●	–200	–100	100	ns
Output Amplifier							
V_{OUTOS}	OUT Offset Voltage	V_{AMPIN} = 0v, I_{OUT} = 0A R_{AMPIN} = 10k (Note 4)	 ●	–6 –8		6 8	mV mV
R_{OUT}	OUT Output Impedance	$–10mA \geq I_{LIM}+ \geq –100mA$, LIM^+ Shorted to OUT $10mA \leq I_{OUT} \leq 100mA$, $LIM^–$ Shorted to $V^–$			0.01 0.15		Ω Ω
I_{OUTSC}	OUT Short-Circuit Current	LIM^+ Shorted to OUT $LIM^–$ Shorted to $V^–$	●	±100	±190		mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: IC Supply current specification represents unloaded condition and does not include external FET gate pull up/down currents ($GATE^+$, $GATE^–$ pins). Actual total IC bias currents will be higher and vary with operating conditions. See Applications Information.

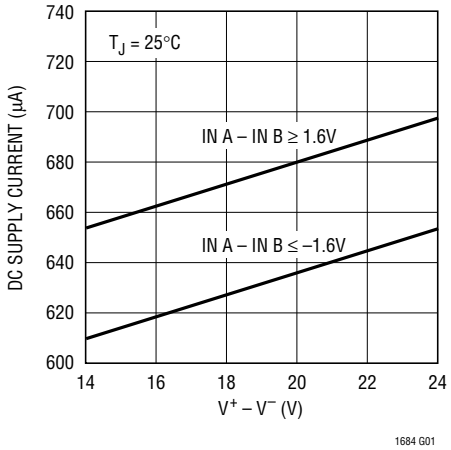
Note 3: PWM inputs are high impedance through ±100mV beyond the input thresholds.

Note 4: 10k resistor from pin AMPIN to ground.

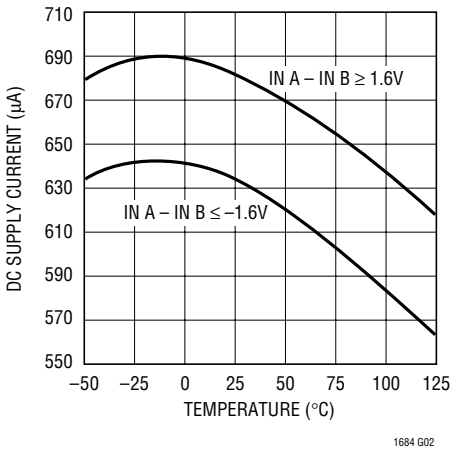
Note 5: Guaranteed but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

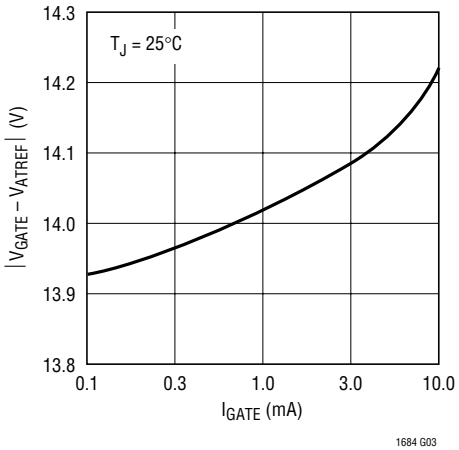
DC Supply Current vs V⁺ – V⁻



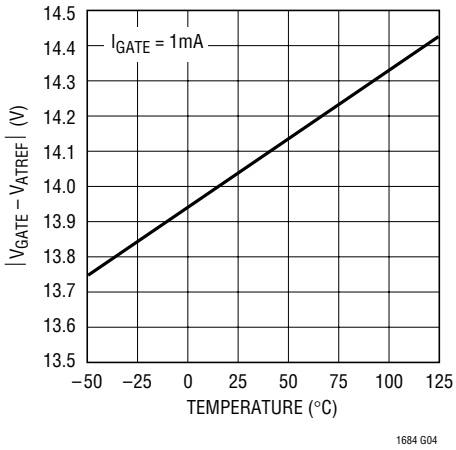
DC Supply Current vs Temperature



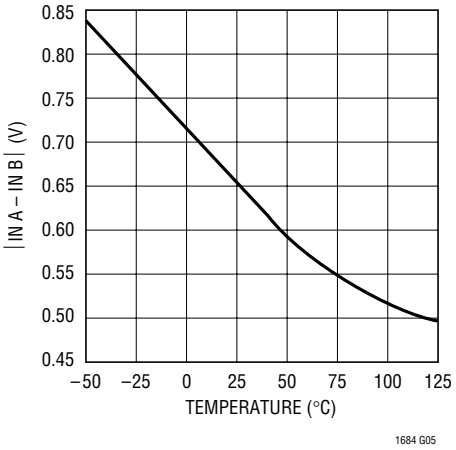
$V_{GATE} – V_{ATREF}$ Voltage Magnitudes vs I_{GATE}



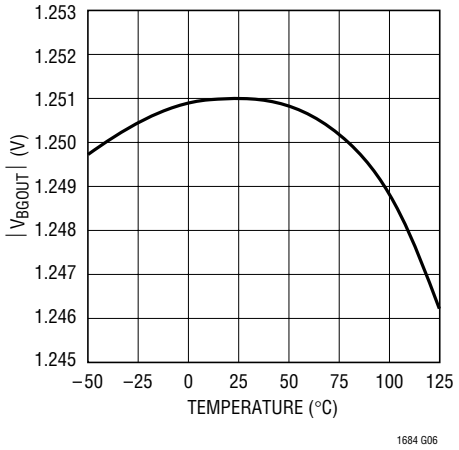
$V_{GATE} – V_{ATREF}$ Voltage Magnitudes vs Temperature



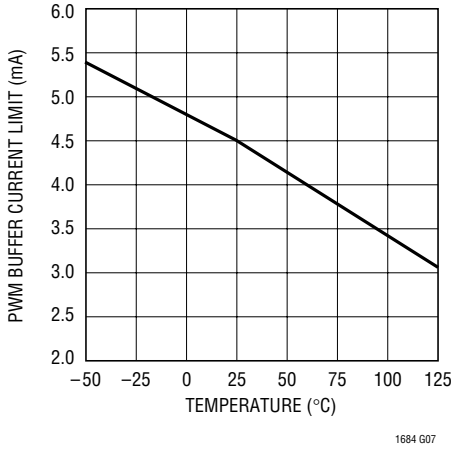
PWM Input Thresholds vs Temperature



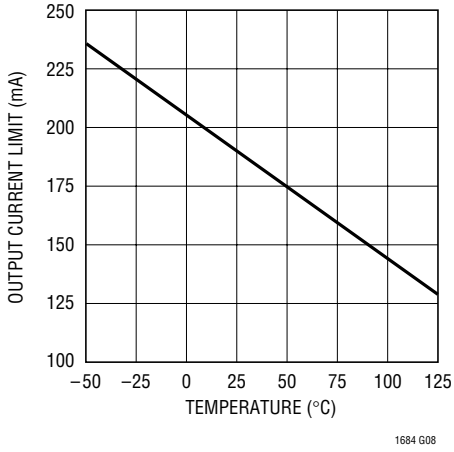
V_{BGOUT} Magnitude vs Temperature



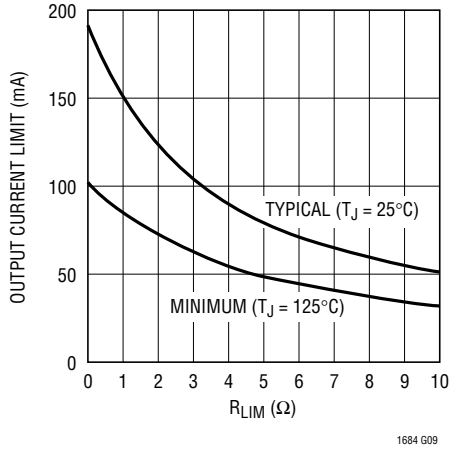
PWM Buffer (Pin BG_{OUT}) Current Limit vs Temperature



Output Amplifier Current Limit vs Temperature (R_{LIM} = 0Ω)



Output Amplifier Current Limit vs External Limiting Resistor Values



PIN FUNCTIONS

IN B (Pin 1): PWM Negative Input. Input is isolated from digital source by ~100pF series capacitor. A 10k resistor can be connected to the IN B pin in series with the isolation capacitor for transient protection. The PWM receiver implements a diode forward drop of input hysteresis (relative to IN A). This hysteresis and internal signal limiting assure common mode glitch rejection with isolation capacitor mismatches up to 2:1. For maximum performance, however, effort should be made to match the two PWM input isolation capacitors. Pin IN B is differentially clamped to pin IN A through back-to-back diodes. This results in a high impedance differential input through ±100mV beyond the input thresholds. 5k internal input resistors yield a 10k (nominal) differential overdrive impedance.

COMP1 (Pin 2): Output Amplifier Primary Compensation. Connect a 100pF capacitor from pin COMP1 to pin OUT.

COMP2 (Pin 3): Output Amplifier Secondary Compensation. Connect a 20pF capacitor from pin COMP2 to pin OUT.

LIM$^-$ (Pin 4): Output Amplifier Current Sink Limit. Pin implements $I_{OUT} \bullet R = V_{BE}$ current clamp. Internal clamp resistor has a typical value of 3.5Ω. For maximum current drive capability (190mA typical) short pin to pin V^-. Reduction of current sink capability is achieved by placing additional resistance from pin LIM$^-$ to pin V^-. (i.e. An external 3.5Ω resistance from pin LIM$^-$ to pin V^- will reduce the current sinking capability of the output amplifier by approximately 50%.)

V$^-$ (Pin 5): Local Negative Supply. Typically connected to the source of the active tracking supply P-channel MOSFET. V^- rail voltage is GATE$^-$ self-bias voltage less the MOSFET V_{GS}. Typical P-channel MOSFET characteristics provide $AT_{REF} - V^- \approx 10V$.

GATE$^-$ (Pin 6): Negative Power Supply FET Gate Drive. Pin sources current from pull-down resistor to bias gate of active tracking supply P-channel MOSFET. Self-biases to a typical value of –14V, referenced to pin AT_{REF}. Pull-down resistor value is determined such that current sourced from the GATE$^-$ pin remains greater than 50μA at minimum output signal voltage and less than 10mA at maximum output signal voltage.

AT_{REF} (Pin 7): Active Tracking Supply Reference. Typically connected to pin OUT. Pin bias current is the difference between the magnitudes of GATE$^+$ pin bias and GATE$^-$ pin bias ($I_{ATREF} = |I_{GATE+}| - |I_{GATE-}|$).

OUT (Pin 8): Ring Tone Output Pin. Output of active filter amplifier/buffer. Used as reference voltage for internal functions of IC. Usually shorted to pin AT_{REF} to generate reference for active tracking supply circuitry. Connect a 1A (1N4001-type) diode between V^+ and OUT and a 1A Schottky diode from V^- to OUT for line transient protection.

LIM$^+$ (Pin 9): Output Amplifier Current Source Limit. Pin implements $I_{OUT} \bullet R = V_{BE}$ current clamp. Internal clamp resistor has a typical value of 3.5Ω. For maximum current drive capability (190mA typical) short pin LIM$^+$ to pin OUT. Reduction of current source capability is achieved by placing additional resistance from pin LIM$^+$ to pin OUT. (i.e. An external 3.5Ω resistance from pin LIM$^+$ to pin OUT will reduce the current sourcing capability of the output amplifier by approximately 50%.)

V$^+$ (Pin 10): Local Positive Supply. Typically connected to the source of the active tracking supply N-channel MOSFET. This condition should be made using a ferrite bead. Operating V^+ rail voltage is GATE$^+$ self-bias voltage less the MOSFET V_{GS}. Typical N-channel MOSFET characteristics provide $V^+ - AT_{REF} \approx 10V$.

GATE$^+$ (Pin 11): Positive Power Supply FET Gate Drive. Pin sinks current from pull-up resistor to bias gate of active tracking supply N-channel MOSFET. Self-biases to a typical value of 14V, referenced to pin AT_{REF}. Pull-up resistor value is determined such that sink current into GATE$^+$ pin remains greater than 50μA at maximum output signal voltage and less than 10mA at minimum output signal voltage.

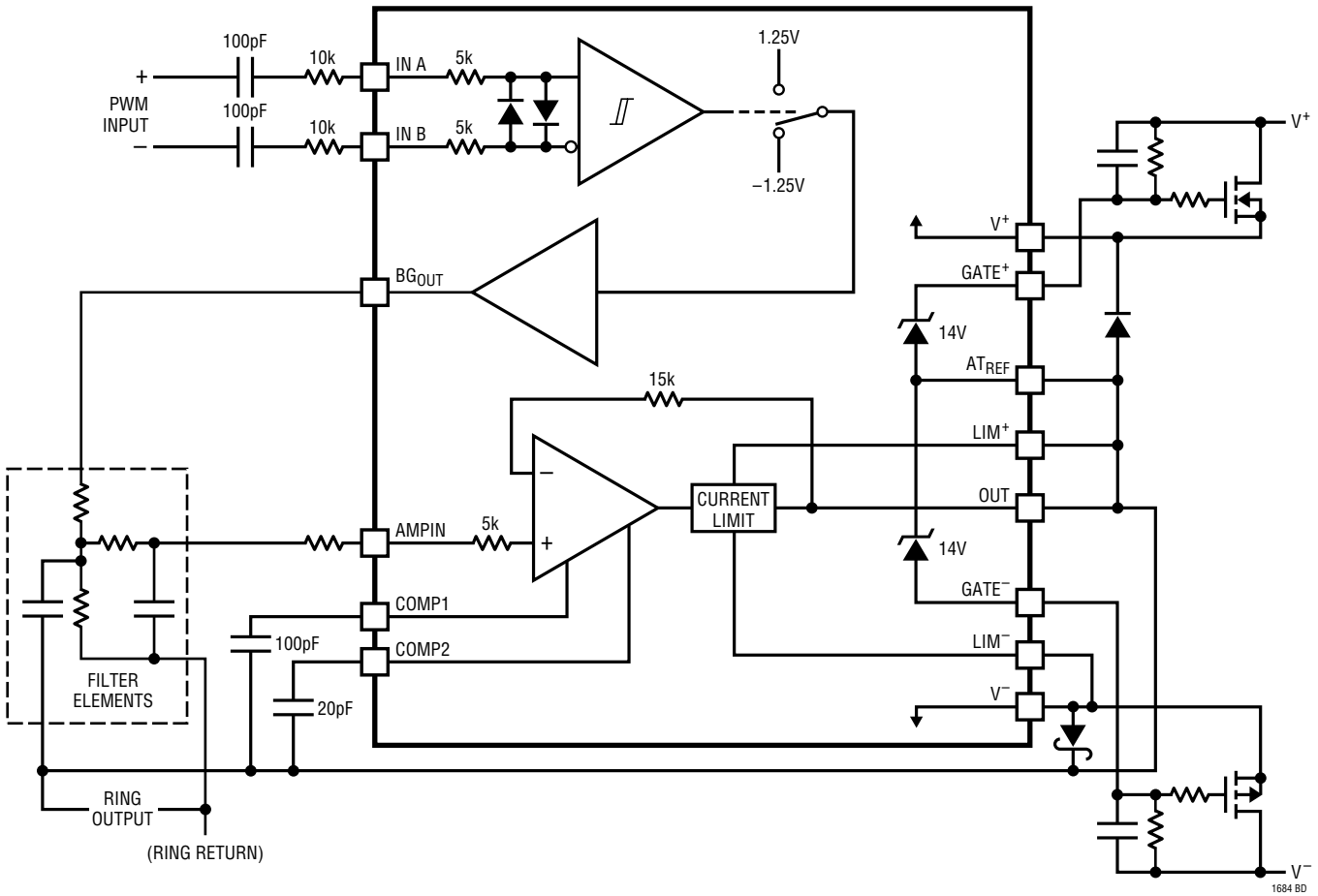
AMPIN (Pin 12): Output Amplifier Input. Connected to external filter components through series protection resistor (usually 5k). Thevenin DC resistance of external filter and protection components should be 10k for optimum amplifier offset performance. See Applications Information section.

PIN FUNCTIONS

BG_{OUT} (Pin 13): Normalized PWM Buffered Output. PWM differential input is amplitude normalized to ±1.25V (referenced to the OUT pin). This signal is used to drive the active filter/amplifier. Filter resistor values must be chosen to limit the maximum current load on this pin to less than 2mA. The output is current limit protected to a typical value of ±4.5mA.

IN A (Pin 14): PWM Positive Input. Input is isolated from digital source by ~100pF series capacitor. A 10k resistor should be connected to the IN A pin in series with the isolation capacitor for transient protection. The PWM receiver implements a diode forward drop of input hysteresis (relative to IN B). This hysteresis and internal signal limiting assure common mode glitch rejection with isolation capacitor mismatches up to 2:1. For maximum performance, however, effort should be made to match the two PWM input isolation capacitors. Pin IN A is differentially clamped to pin IN B through back-to back isolation-base diodes. This results in a high impedance differential input ±100mV beyond the input thresholds. 5k internal input resistors yield a 10k (nominal) differential overdrive impedance.

FUNCTIONAL BLOCK DIAGRAM



LT1684 Block Diagram

OPERATION (Refer to Functional Block Diagram)

BASIC THEORY OF OPERATION

The LT1684 operates using a user-provided pulse-width-modulated (PWM) digital signal as input*. The low frequency modulation component of this signal represents the desired output waveform. Changing the PWM input can thus dynamically control the frequency, cadence, amplitude and DC offset of the desired output. This method of sine wave generation can accomodate all popular ring tone frequencies including 17Hz, 20Hz, 25Hz and 50Hz.

The LT1684 receives the PWM input by a capacitor-isolated differential input at pins IN A and IN B. This signal is amplitude normalized by a bandgap reference and output single-ended on the BG_{OUT} pin such that the PWM carrier is ±1.25V about the voltage on the OUT pin.

The low frequency component of the normalized PWM signal is recovered using an active filter circuit constructed using an onboard driver amplifier. This amplifier also provides current drive for the final ring tone output.

The ring tone output is used as the reference for a floating active biasing scheme by pin AT_{REF}. As the ring tone output rises and falls through its typical range of hundreds of volts, the LT1684 "tracks" the output signal, maintaining local supply voltages across the IC of approximately ±10V.

Input Receiver/Reference Buffer

The differential receiver for the PWM input signal requires minimum differential input levels of 1.6V to assure valid change-of-state. The receiver inputs are capacitor coupled, isolating the LT1684 from the PWM generator. The receiver is leading edge triggered.

The input receiver controls a switched-state output that forces an amplitude normalized voltage (referenced to the OUT pin) of ±1.25V that follows the PWM input. This switched voltage is driven off-chip on pin BG_{OUT}. When the IN A input is driven higher than IN B (by the required 1.6V), the reference drives BG_{OUT} to +1.25V above OUT. When IN B input is driven higher than IN A, BG_{OUT} is forced to –1.25V relative to OUT.

The amplitude normalized representation of the input PWM signal is used as the input for the active filter element and output driver.

Output Amplifier/Driver

The normalized PWM signal output on the BG_{OUT} pin is converted to the final ring tone signal by an active filter. This filter consists of an onboard amplifier and a few external components. Although many different types of filters can be constructed, a 2-pole Multiple Feedback (MFB) configuration generally provides adequate performance and is desirable due to its simplicity and effectiveness.

The low frequency component of the ±1.25V PWM signal contains the desired ring tone frequency and cadence information. The MFB active filter strips this information from the PWM signal and amplifies this low frequency component to generate the final desired output.

Active Tracking Supplies

Implementation of the active tracking supply technique enables linear generation of the ring tone output, and takes advantage of the intrinsic supply noise immunity of a linear amplifier, reducing the need for large high voltage filtering elements.

Two external power MOSFETs act as voltage level-shifting devices and generate the power supply voltages for the LT1684. The LT1684 uses its own output as a voltage reference for the FET level shifters, "suspending" itself (by these generated supply voltages) about the signal output. In this manner, the LT1684 can linearly generate a signal hundreds of volts in amplitude at its output, while maintaining ±10V local supply rails across the IC itself.

* Contact Linear Technology for code.

APPLICATIONS INFORMATION

Encoded PWM Signal Input Basics

The LT1684 accepts a user-supplied PWM carrier that represents the desired output ring tone signal. This PWM input is normalized by the LT1684 such that ring tone output amplitudes can be accurately encoded into the PWM input.

The LT1684 accepts a differential input to maximize rejection of system transients and ground noise. If no differential signal is readily available from the PWM controller, a simple inverter/buffer block can be used to create the differential signal required.

Each differential input is internally connected through a 5k series resistor to back-to-back isolation-base diodes. These devices internally clamp the differential input signal to ±100mV greater than the input comparator hysteresis range. The input comparator toggles with a differential hysteresis equal to that of a standard diode forward voltage (0.7V nominal). As such, the differential impedance of the input remains high throughout the input hysteresis region, then reduces to a nominal value of 10k (7k minimum) as the input is overdriven beyond the comparator input threshold. A minimum differential input of 1.6V is specified to assure valid switching.

The PWM signal can be visualized in terms of instantaneous ring tone amplitude, normalized to the LT1684 amplitude reference. For a given desired output voltage V_{OUTN}, the input pulse train required follows the relation:

$V_{OUTN} = 2 \bullet V_{REF} \bullet (DC - 0.5)$, or

$DC = [V_{OUTN} / (2 \bullet V_{REF})] + 0.5$, where:

V_{REF} = 1.25V normalized peak voltage

DC = PWM input duty cycle

A 10% to 90% duty cycle range is a practical limit for a 10kHz input carrier. This corresponds to normalized signal amplitude of ±1V. Duty cycles exceeding this range can cause increased output signal distortion as signal energy is lost due to finite rise and fall times becoming a significant percentage of the signal pulses. The associated reduction in the pulse energy manifests itself as a "soft clipping" of the output signal resulting in an increase in harmonic distortion.

The normalized PWM signal is amplified to the desired output signal level by the active filter/amplifier stage. Thus, dividing the desired peak output amplitude by the peak normalized encoded amplitude (V_{OUT}/V_{OUTN}) yields the required DC gain of the active filter.

System Considerations

Assuming use of a 10% to 90% maximum PWM range, the peak normalized signal will be:

$V_{PWM}(pk) = \pm 0.8 \bullet V_{REF} = \pm 1.0V$, and:

$V_{OUT}(pk) = V_{PWM}(pk) \bullet$ Filter DC Gain

Thus, the DC gain of the output filter equals the desired peak voltage of the output ring tone signal.

The frequency characteristics of the lowpass output filter must reflect the allowable carrier ripple on the output signal. For example, a 10kHz carrier system could use a 2-pole Butterworth lowpass with a cutoff frequency of 100Hz. This filter provides 40dB of input signal rejection at 10kHz yielding $25mV_{P-P}$ output ripple. If the DC gain of the output filter/amplifier was 100, the output ripple voltage would be riding on a ±100V sine wave, and therefore be about –78dB relative to the output ring signal.

APPLICATIONS INFORMATION

For applications that are extremely output ripple sensitive, additional carrier rejection can be accomplished by modifying the output filter/amplifier characteristics such as implementing elliptical filter characteristics with a lower cutoff frequency or implementation of additional poles.

Filter Design and Component Selection

The ring tone information represented in the low frequency component of the input PWM signal is retrieved using an active filter. This filter also generates the appropriate low frequency gain required to produce the high voltage output signal and references the output to ground (or other system reference). The frequency and gain characteristics of this circuit element are both configurable by the appropriate choice of external passive filter elements. Because of the active tracking supply mode of operation, conventional active filter topologies cannot be used. Most amplifier/filter topologies can, however, be "transformed" into active tracking supply topologies.

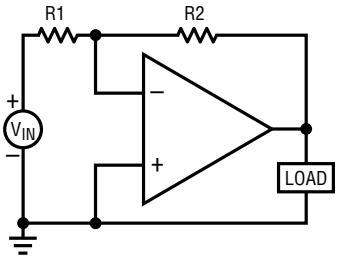
A conventional amplifier circuit topology can be "transformed" into an active tracking supply amplifier circuit by:

a) Inverting the amplifier signal polarity (swap amplifier + and – connections) and input source polarity.

b) Referencing all signals to the output except the feedback elements, which are referenced to ground (swap output and ground).

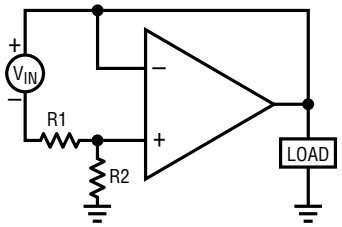
A variety of amplifier/filter configurations can be realized using the transformation technique. A 2-pole filter is generally adequate for most ringer applications. Due to the relative simplicity of infinite-gain Multiple Feedback (MFB) configurations, these filters are good candidates for ringer applications. Component selection and active tracking supply transformation will be described for the following 2-pole MFB infinite-gain lowpass filter.

Conventional Amplifier Configuration

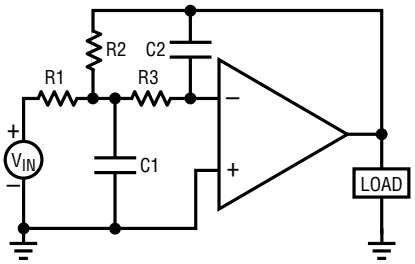


TRANSFORMATION

Active Tracking Supply Amplifier

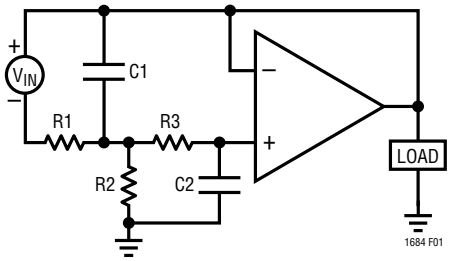


Lowpass Mulitple Feedback Active Filter



TRANSFORMATION

Active Tracking Supply Lowpass Multiple Feedback Filter



APPLICATIONS INFORMATION

The component selections for the active tracking supply lowpass MFB filter configuration follow the relations:

$$C_2 = mC_1 \qquad m \leq 1 / [4Q^2(1+|H_0|)]$$

$$R_2 = \frac{1 \pm [1-4mQ^2(1+|H_0|)]^{1/2}}{2\omega_n C_1 mQ}$$

$$R_1 = R_2 / |H_0|$$

$$R_3 = \frac{1}{\omega_n^2 C_1^2 R_2 m}$$

Example:

Conditions: Output ring tone peak voltage = 100V

Ring frequency = 20Hz

Input duty cycle range = 10% to 90%

Filter Q = 0.707

Set: $f_n = \omega_n / 2\pi = 100Hz$

Choose: **$C_1 = 1.0\mu F$** (a convenient value)

Then: $m \leq [4(0.7)^2(1+100)]^{-1} \approx .005$

$C_2 = mC_1$ **C2 = 4700pF**

(sets m = 0.0047)

$$R_2 = \frac{1 \pm [1-4(0.0047)(0.707)^2(101)]^{1/2}}{(4\pi 100)(1e-6)(.0047)(0.707)}$$

$R_2 = 300k$

$R_1 = 300k/100$

$R_1 = 3.0k$

$R_3 = [(2\pi 100)^2(1e-6)^2(300k)(0.0047)]^{-1}$

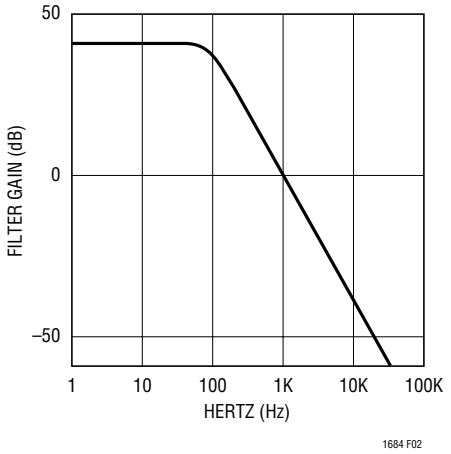
$R_3 = 2k$

This filter configuration yields a DC Gain of 100, a corner frequency of just under 100Hz with gain reduction of only 0.1% at 20Hz, and a 10kHz carrier rejection of greater than 40dB at the output.

Active Tracking Supply Components

Given the previous discussion, implementation of an active tracking supply system may seem almost trivial.

Active Tracking Supply Lowpass Multiple Feedback Filter Transfer Characteristic (A_V vs f_n)



However, bootstrapping an amplifier system about its own output creates a complex myriad of inherent stability and response issues. Attempting such a configuration with generic "jelly-bean" components is not recommended for the faint of heart or type-A personalities. The LT1684, however, makes for a simplistic approach to active tracking component selection.

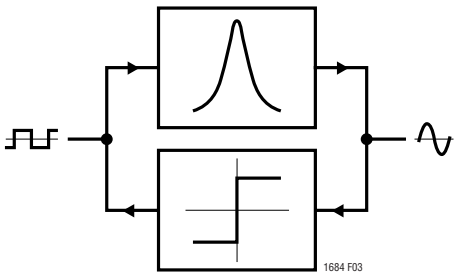
The high voltage MOSFET transistors used in the circuit must have an operating V_{DS} specified at greater than the corresponding high voltage supply rail plus the opposite maximum excursion of the output signal. For example, if a system is designed with a 240V supply (+120V, –120V) and outputs a ring signal that has a 100V peak amplitude, the MOSFET V_{DS} ratings must be greater than 240/2 + 100 = 220V.

Active Filter Tuned Oscillator— No PWM Input Required

A simple yet effective method of producing a high quality sine wave is to place a high-Q bandpass filter and a hard limited gain element in a positive feedback loop. This circuit will oscillate at the bandpass frequency, producing a sine wave at the filter output. The product of the fundamental component of the limiter and the filter gain at the bandpass frequency determines the output amplitude. This type of circuit is commonly referred to as an active filter tuned oscillator.

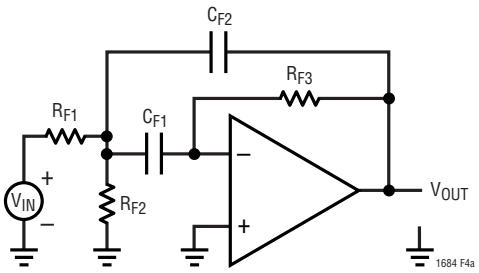
APPLICATIONS INFORMATION

Active Filter Tuned Oscillator Block Diagram

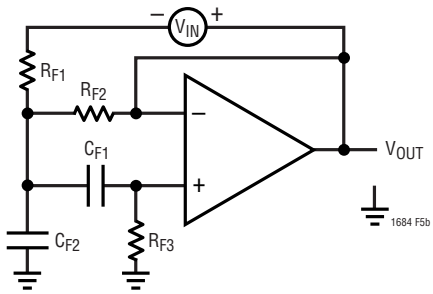


The LT1684 can be implemented easily into a telephone ringer circuit based on the active filter tuned oscillator topology, eliminating the need for a user-supplied PWM input signal. The LT1684's active filter amplifier can be used as a high-Q bandpass filter element by configuring it as an active tracking supply bandpass. The LT1684's controlled output receiver/buffer is also convenient for use as the hard limiter. Because the LT1684 receiver/buffer requires a true differential input for proper operation, a dual comparator IC such as the LT1017 must be bootstrapped along with the LT1684 to provide differential control signals. The LT1017 and LT1684 receiver/buffer combine to create a high gain hard limiter whose output is controlled to ±1.25V. The LT1684 active bandpass filter is then connected as a positive feedback element with the limiter component, which completes the active filter tuned oscillator topology.

Bandpass MFB Filter



Active Tracking Bandpass MFB Filter



The active bandpass filter circuit is easily configured using a basic MFB bandpass configuration, however, the active tracking supply technique used by the LT1684 requires "transformation" of this topology. This "transformation" swaps the amplifier signal polarity, references all signals to the output, and references all feedback elements to ground as described previously in the Filter Design and Component Selection section.

The design equations for the active tracking bandpass filter are the same as the pretransformation MFB topology, such that if $C_{F1} = C_{F2} = C$:

$$R_{F1} = Q/(\omega_0 \bullet C \bullet |H_0|)$$

$$R_{F2} = Q/(2Q^2 - |H_0|)(\omega_0 \bullet C)$$

$$R_{F3} = 2Q/(\omega_0 \bullet C)$$

Example:

Conditions: Output peak voltage = 95V

Ring frequency = 20Hz

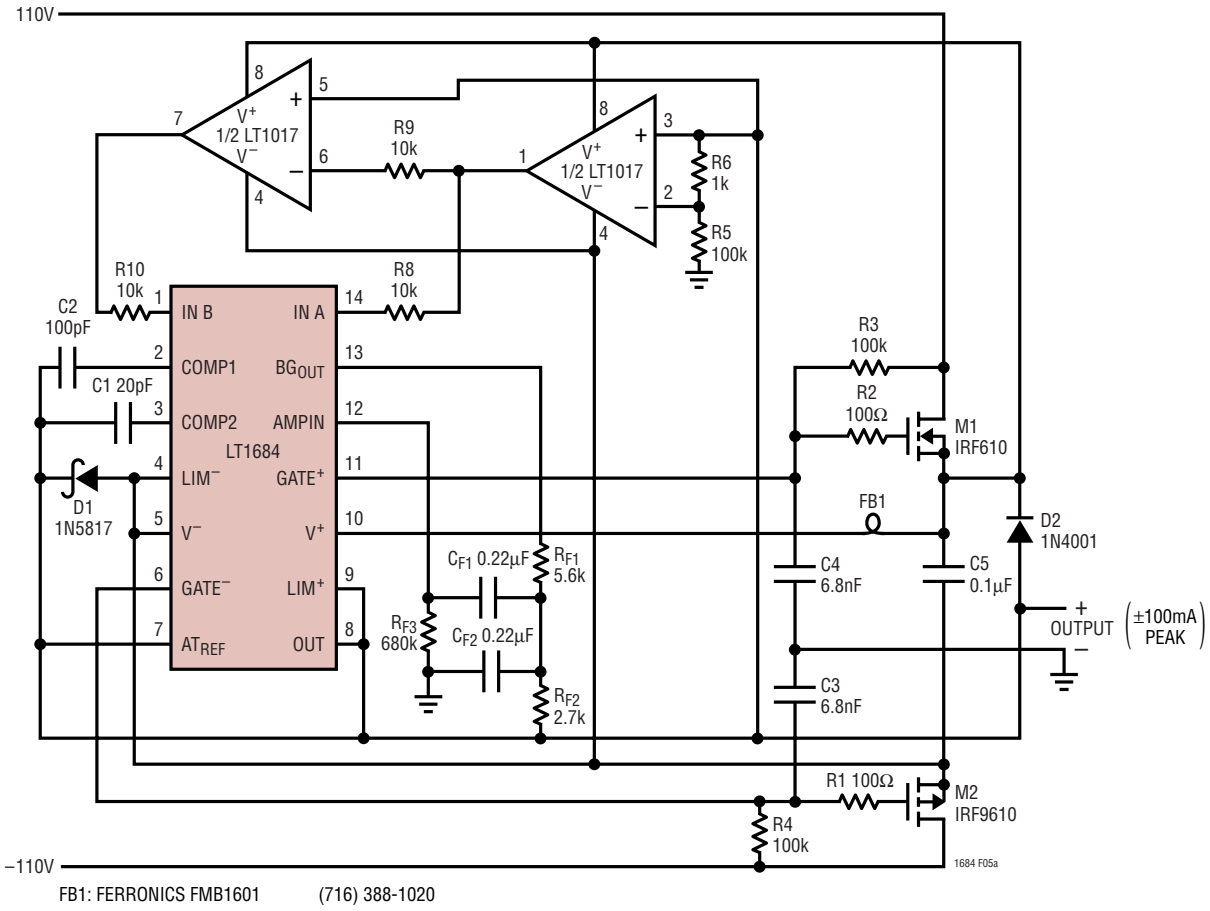
Bandpass Q = 9.4

A square wave with peak amplitude A has a fundamental component with amplitude 4A/π, where A = 1.25V. Therefore, the desired filter's bandpass gain $|H_0| = 95/(4 \bullet 1.25/\pi) \sim 60$. Given capacitor values C = 0.22µF (a convenient value) and desired filter characteristics of: Q = 9.4, $|H_0| = 60$, $\omega_0 = 2\pi(20Hz)$, then: R_{F1} = 5.6k, R_{F2} = 2.7k, R_{F3} = 680k. The amplitude, frequency and envelope response time of the output signal can be adjusted by simply changing the values of resistors R_{F1} to R_{F3} accordingly.

This produces a high voltage, high quality 20Hz sine wave at the filter output with a peak amplitude of 95V. Differential amplitude and frequency characteristics are achieved by simply changing a few resistor values. The output of the LT1684 is internally current limited to a minimum of ±100mA peak, allowing this ring tone generation circuit to be used with loads up to 7 REN with no degradation of the output waveform.

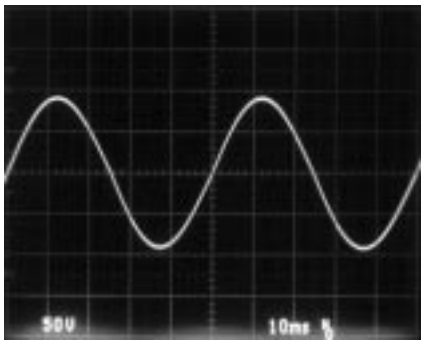
APPLICATIONS INFORMATION

Active Filter Tuned Oscillator Ring Tone Generator



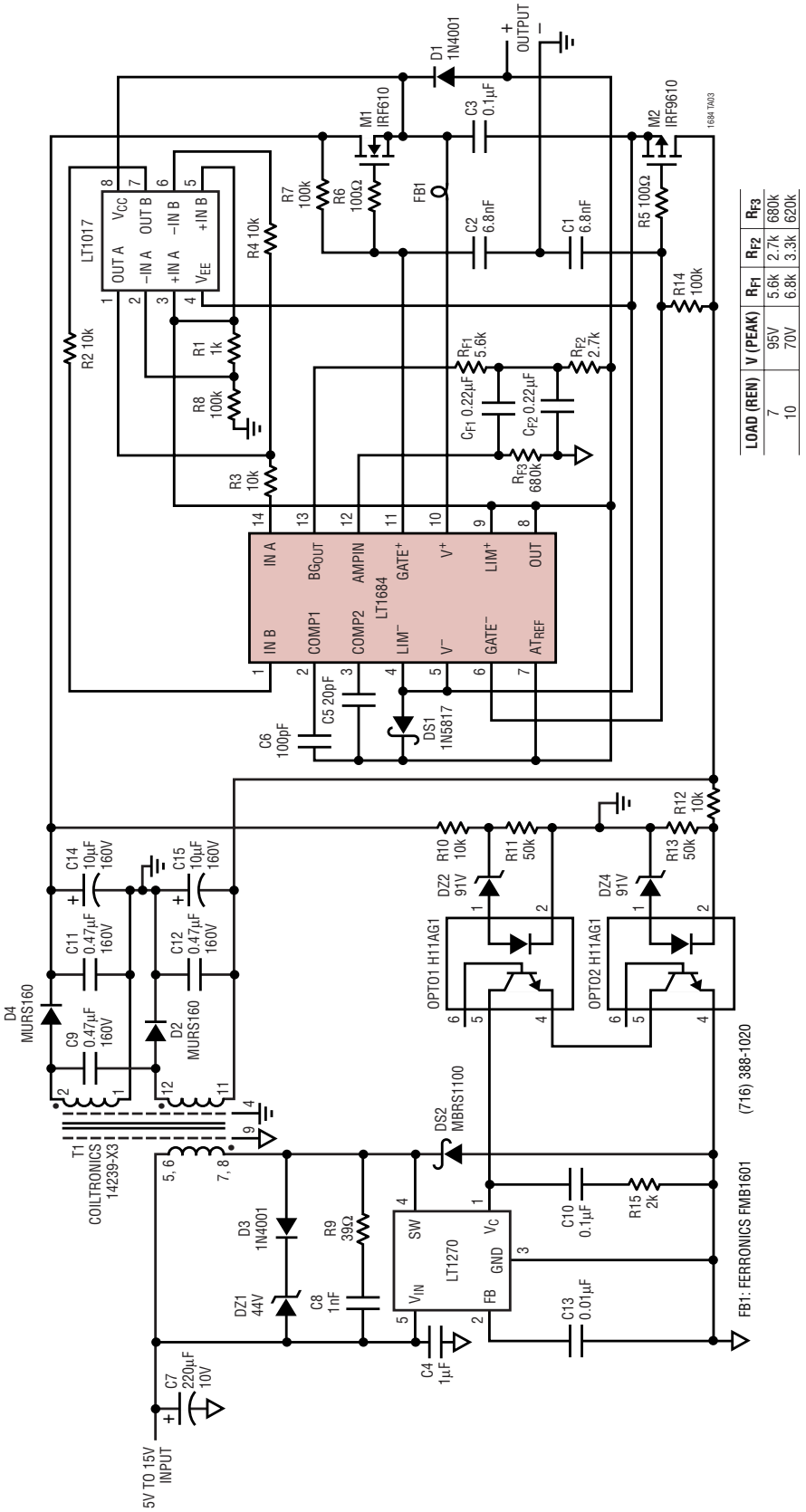
FB1: FERRONICS FMB1601 (716) 388-1020

Ringer Output



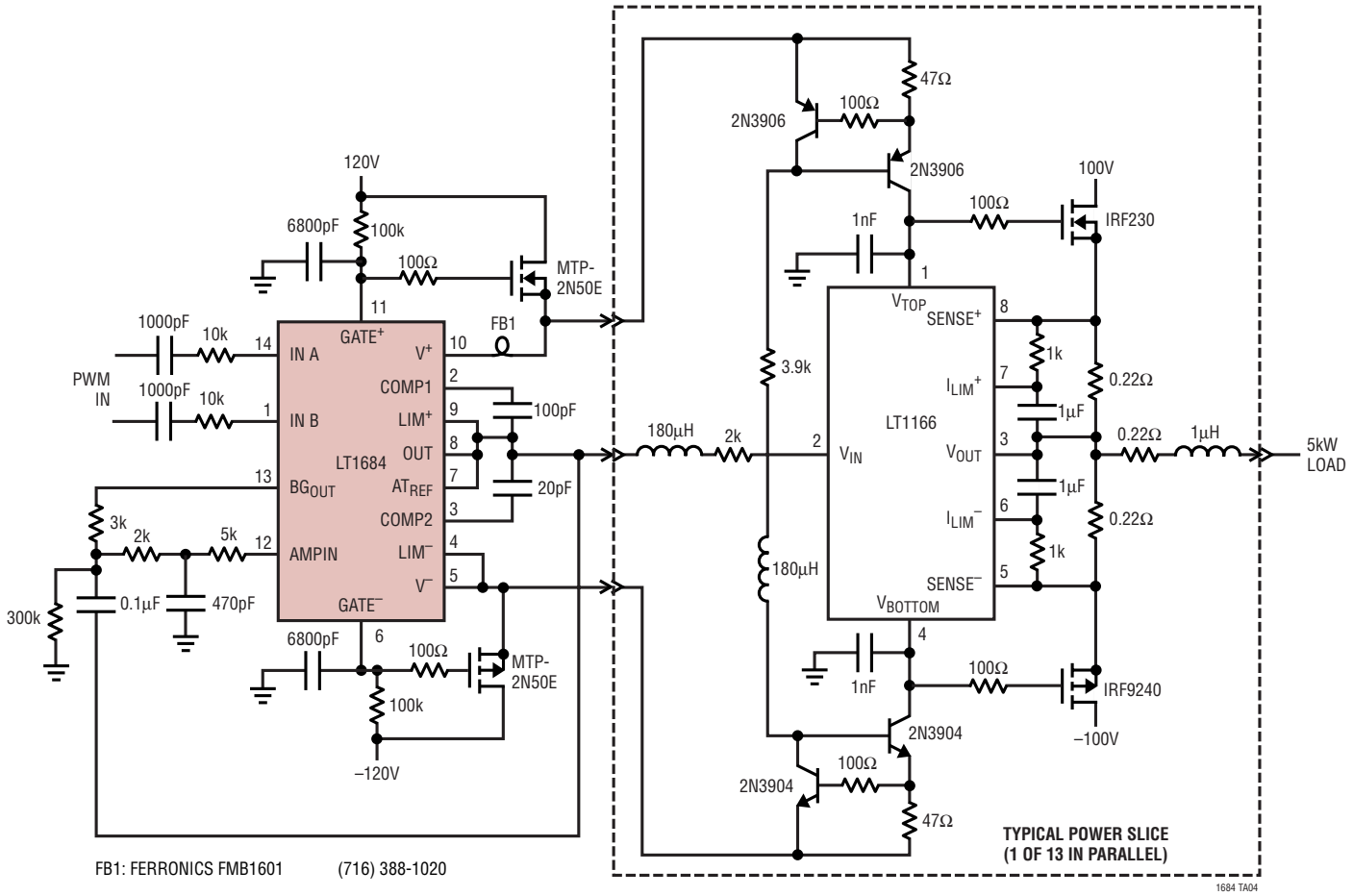
TYPICAL APPLICATIONS

5V-15V to Ring Tone Fully Isolated Converter Using an Active Filter-Tuned Oscillator Circuit



TYPICAL APPLICATIONS

5kW PWM-to-Analog Converter

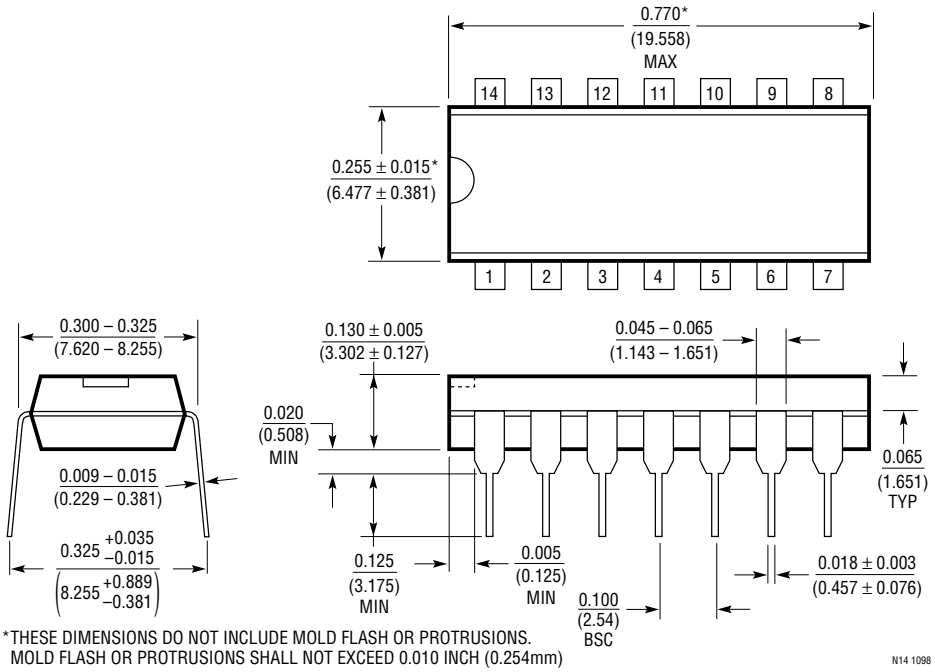


FB1: FERRONICS FMB1601 (716) 388-1020

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

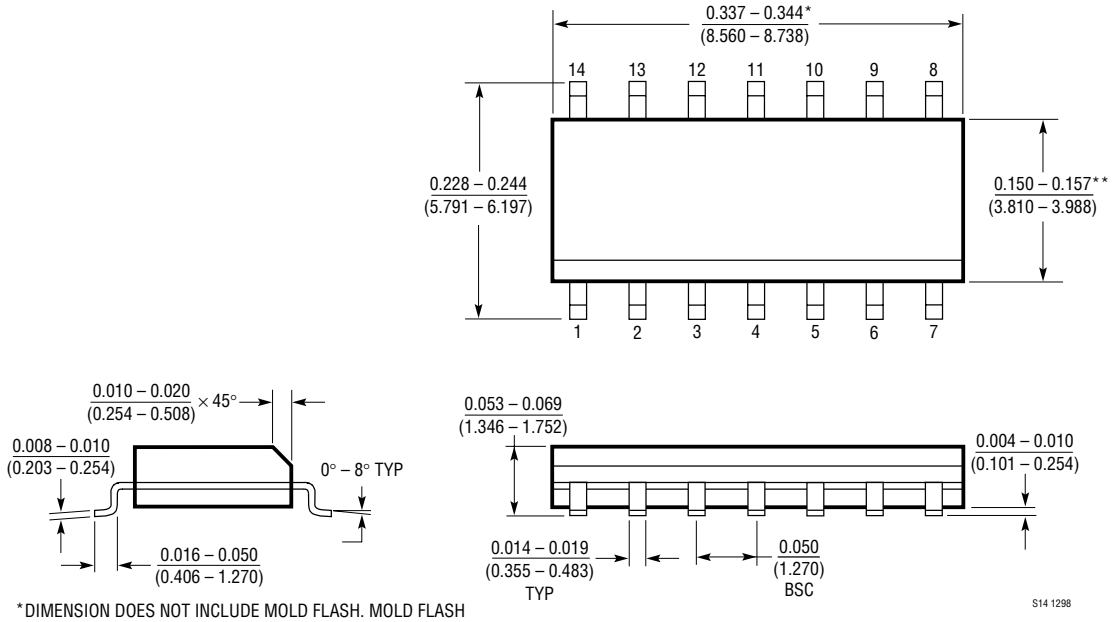
N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N14 1098

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



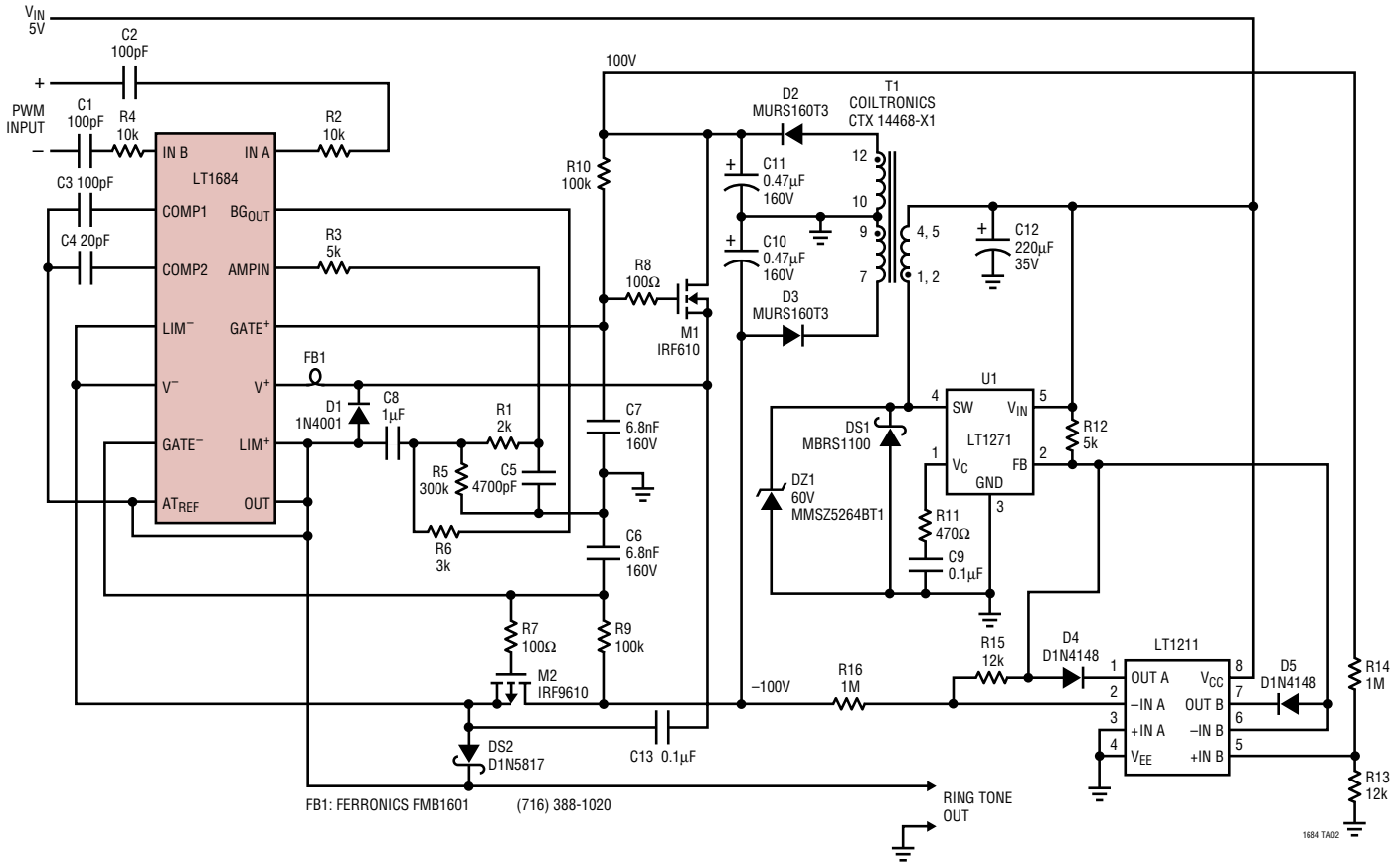
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S14 1298

TYPICAL APPLICATION

5V Input Nonisolated 5 REN Ring Generator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1082	1A High Voltage Switching Regulator	V_{IN} = 3V to 75V, SW Voltage = 100V
LT1166	Power Output Stage Automatic Bias System	Sets Class AB Bias Currents, Eliminates Adjustments and Thermal Runaway
LTC1177-5/LTC1177-12	Isolated MOSFET Drivers	2500V_{RMS} Isolation, UL Recognized
LT1270	8A Power Switching Regulator	V_{IN} = 3.5V to 30V, I_Q = 7mA
LT1271	4A Power Switching Regulator	V_{IN} = 3.5V to 30V, I_Q = 7mA
LT1339	High Power Synchronous DC/DC Controller	Operation Up to 60V, Output Current Up to 50A
LT1676	Wide Input Range, High Efficiency, Step-Down Switching Regulator	Operation Up to 60V, 100kHz, Up to 500mA Output

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