5 V, 3 A Logic Controlled High-Side Power Switch

Data Sheet **ADP197**

FEATURES

Low RDS_{ON} of 12 mΩ
Low input voltage range: 1.8 V to 5.5 V
Quick output discharge (QOD) circuit (ADP197-02)
3 A continuous operating current at 70°C
1.2 V logic-compatible enable input
Low 18 µA quiescent current, V_{IN} < 3 V
Low 31 µA quiescent current, V_{IN} = 4.2 V
Overtemperature protection
Ultralow shutdown current: <1 µA
Ultrasmall 1.0 mm × 1.5 mm, 0.5 mm pitch, 6-ball WLCSP
Tiny 2.0 mm × 2.0 mm × 0.55 mm, 0.65 mm pitch, 6-lead LFCSP

APPLICATIONS

Mobile phones
Digital cameras and audio devices
Portable and battery-powered equipment

TYPICAL APPLICATIONS CIRCUIT

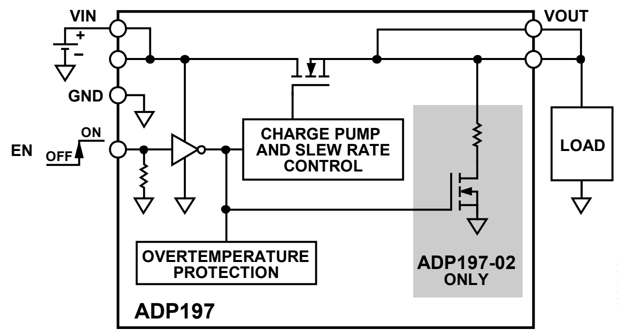

Figure 1.

GENERAL DESCRIPTION

The ADP197 is a high-side load switch designed for operation between 1.8 V and 5.5 V. This load switch provides power domain isolation, which helps extend battery operation. The device contains a low on-resistance, N-channel MOSFET that supports more than 3 A of continuous current and minimizes power loss. The low 18 µA quiescent current and ultralow shutdown current make the ADP197 ideal for battery-operated portable equipment. The built-in level shifter for enable logic makes the ADP197 compatible with many processors and GPIO controllers.

Overtemperature protection circuitry activates if the junction temperature exceeds 125°C, thereby protecting itself and downstream circuits from potential damage.

The ADP197-02 incorporates an internal quick output discharge (QOD) circuit to discharge the output capacitance when the ADP197-02 output is disabled

In addition to operating performance, the ADP197 WLCSP package occupies minimal printed circuit board (PCB) space with an area of less than 1.5 mm^2 and a height of 0.60 mm.

The ADP197 is available in an ultrasmall 1.0 mm × 1.5 mm, 0.5 mm pitch, 6-ball WLCSP and a 2.0 mm × 2.0 mm × 0.55 mm, 0.65 mm pitch, 6-lead LFCSP.

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5/12—Rev. A to Rev. B

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11/11—Rev. 0 to Rev. A

Changed EN to GND Rating, Table 2 ... 4

4/11—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, I_{OUT} = 1 A, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +85°C	1.8		5.5	V
EN INPUT						
EN Input	V_{IH}	V_{IN} = 1.8 V to 5.5 V	1.2			V
	V_{IL}	V_{IN} = 1.8 V to 5.5 V, T_J = −40°C to +85°C			0.4	V
		V_{IN} = 1.8 V to 5.5 V, T_J = −40°C to +110°C			0.35	V
EN Input Pull-Down Current	I_{EN}	V_{IN} = 1.8 V		500		nA
CURRENT						
Ground Current	I_{GND}	V_{IN} = 1.8 V		18		μA
		V_{IN} = 3.4 V		14		μA
		V_{IN} = 4.2 V, T_J = −40°C to +110°C		18	31	μA
		V_{IN} = 5.5 V		28		μA
Off State Current	I_{OFF}	V_{EN} = GND, V_{OUT} = 0 V, V_{IN} = 4.2 V		0.1		μA
		V_{EN} = GND, T_J = −40°C to +85°C, V_{OUT} =0 V, V_{IN} = 1.8 V to 5.5 V			20	μA
		V_{EN} = GND, T_J = −40°C to +110°C, V_{OUT} =0 V, V_{IN} = 1.8 V to 5.5 V			75	μA
Continuous Operating Current[1]	I_{OUT}	V_{IN} = 1.8 V to 5.5 V		3		A
VIN TO VOUT RESISTANCE	RDS_{ON}					
WLCSP		V_{IN} = 5.5 V		0.012		Ω
		V_{IN} = 4.2 V		0.012		Ω
		V_{IN} = 1.8 V		0.012		Ω
		V_{IN} = 1.8 V, T_J = −40°C to +85°C		0.012	0.017	Ω
LFCSP		V_{IN} = 5.5 V		0.027		Ω
		V_{IN} = 4.2 V		0.027		Ω
		V_{IN} = 1.8 V		0.027		Ω
		V_{IN} = 1.8 V, T_J = −40°C to +85°C		0.027	0.036	Ω
V_{OUT} TURN-ON DELAY TIME		See Figure 2				
Turn-On Delay Time	t_{ON_DLY}	V_{IN} = 1.8 V to 5.5 V, C_{LOAD} = 1 μF		1		ms
ACTIVE PULL-DOWN RESISTANCE (ADP197-02 OPTION ONLY)	$R_{PULLDOWN}$	V_{IN} = 3.2 V		380		Ω
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		125		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C

[1] At an ambient temperature of 85°C, the device can withstand a continuous current of 2.22 A. At a load current of 3 A, the operational lifetime derates to 2190 hours.

TIMING DIAGRAM

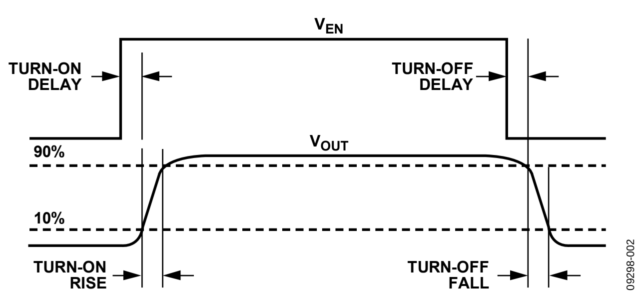

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
VOUT to GND	−0.3 V to V_{IN}
EN to GND	−0.3 V to +6.5 V
Continuous Drain Current	
T_A = 25°C	±4 A
T_A = 85°C	±2.22 A
Continuous Diode Current	−50 mA
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +105°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Typical θ_{JA} and Ψ_{JB} Values

Package Type	θ_{JA}	Ψ_{JB}	Unit
6-Ball, 0.5 mm Pitch WLCSP	260	58	°C/W
6-Lead, 0.65 mm Pitch LFCSP	68.9	44.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

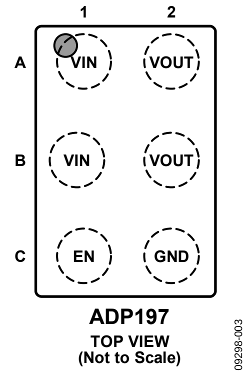

Figure 3. 6-Ball WLCSP Pin Configuration

Table 4. 6-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, B1	VIN	Input Voltage.
A2, B2	VOUT	Output Voltage.
C1	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
C2	GND	Ground.

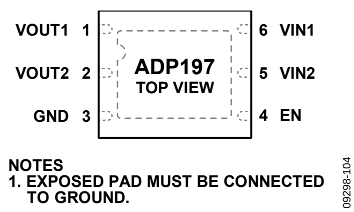

Figure 4. 6-Lead LFCSP Pin Configuration

Table 5. 6-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT1	Output Voltage. Connect VOUT1 and VOUT2 together.
2	VOUT2	Output Voltage. Connect VOUT1 and VOUT2 together.
3	GND	Ground.
4	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
5	VIN2	Input Voltage. Connect VIN1 and VIN2 together.
6	VIN1	Input Voltage. Connect VIN1 and VIN2 together.
	EP	Exposed Pad. The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

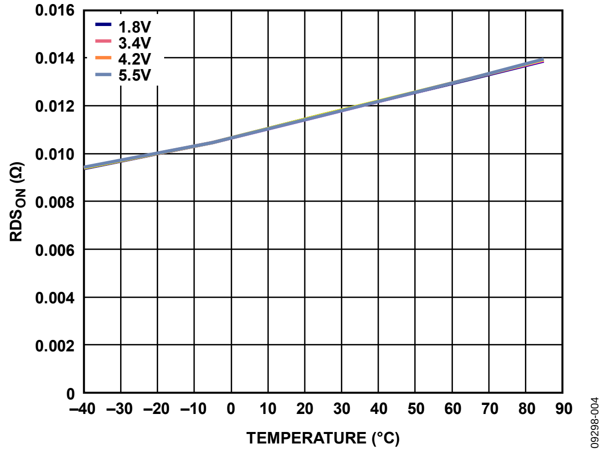

Figure 5. RDS_{ON} vs. Temperature, 500 mA

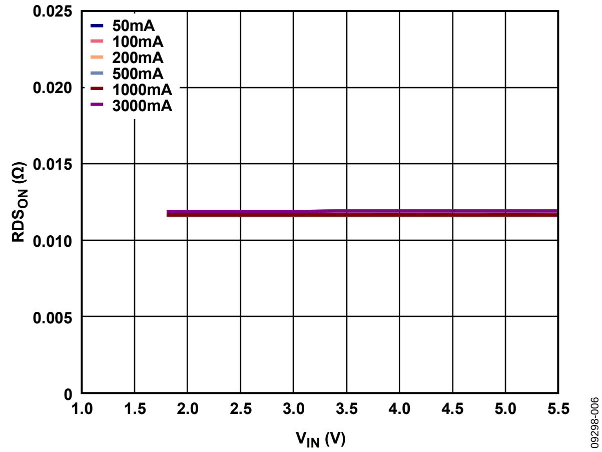

Figure 8. RDS_{ON} vs. Input Voltage (V_{IN}), Different Load Currents

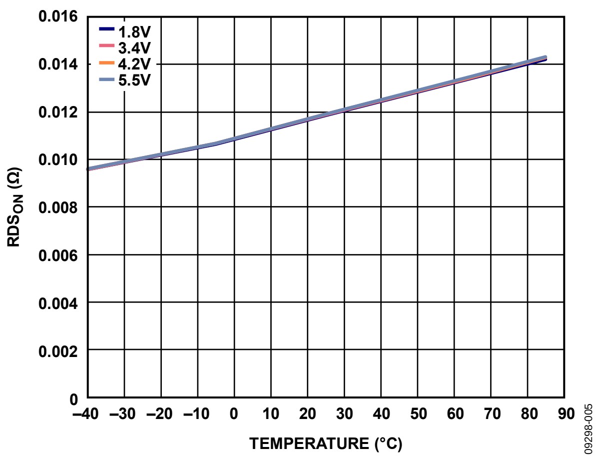

Figure 6. RDS_{ON} vs. Temperature, 3 A, Different Input Voltages (V_{IN})

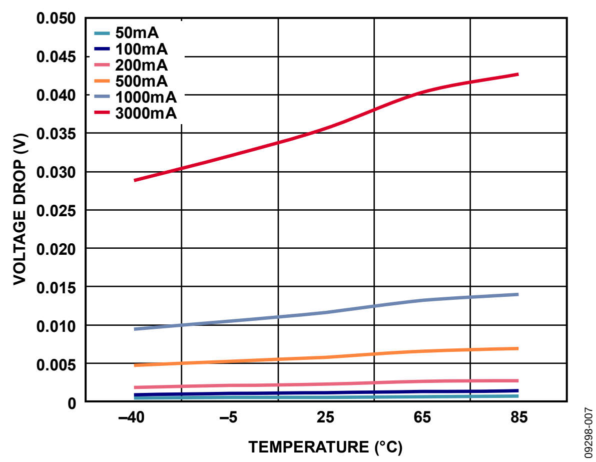

Figure 9. Voltage Drop vs. Temperature, Different Load Currents

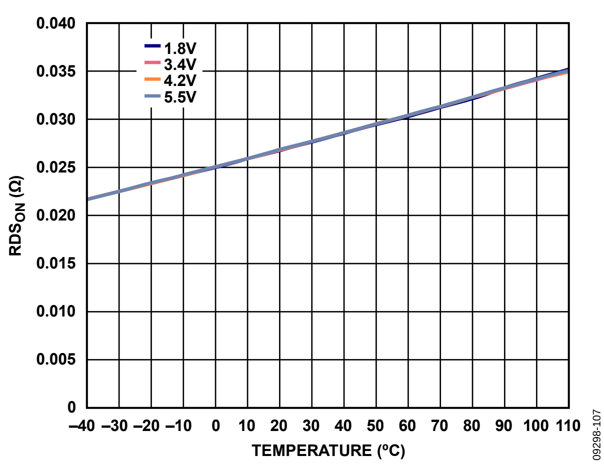

Figure 7. RDS_{ON} (LFCSP) vs. Temperature, 500 mA, Different Input Voltages (V_{IN})

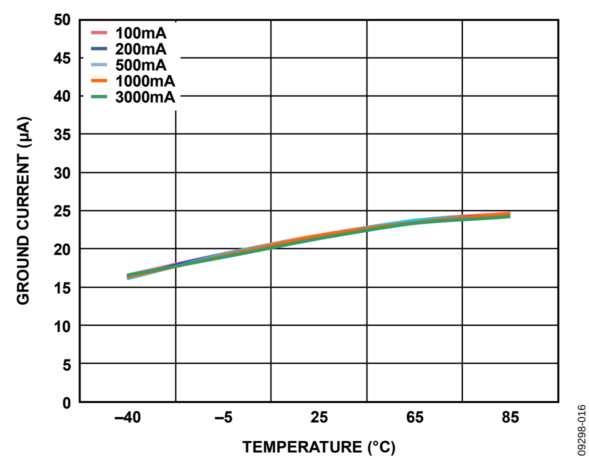

Figure 10. Ground Current vs. Temperature, Different Load Currents, V_{IN} = 1.8 V

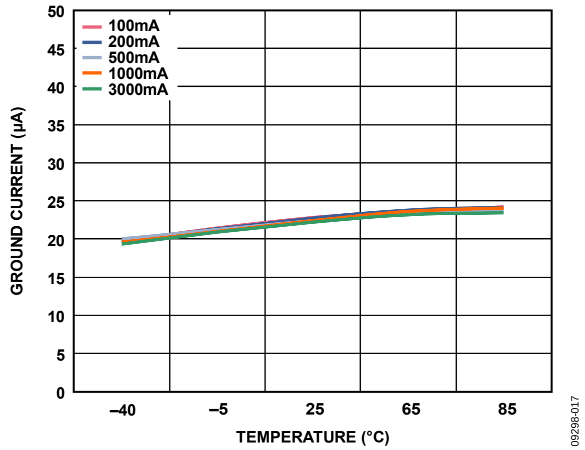

Figure 11. Ground Current vs. Temperature, Different Load Currents, V_{IN} = 4.2 V

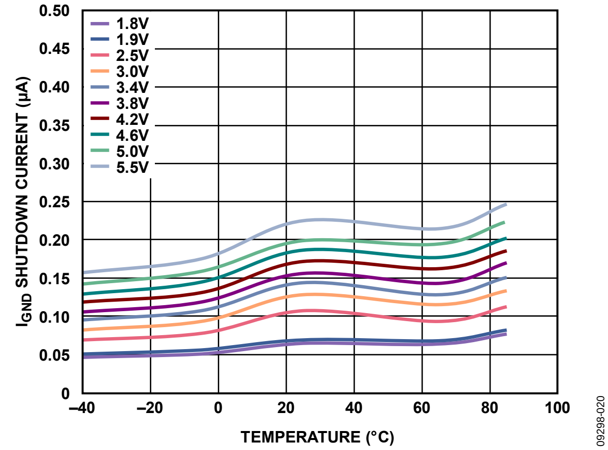

Figure 14. I_{GND} Shutdown Current vs. Temperature, Output Open, Different Input Voltages (V_{IN})

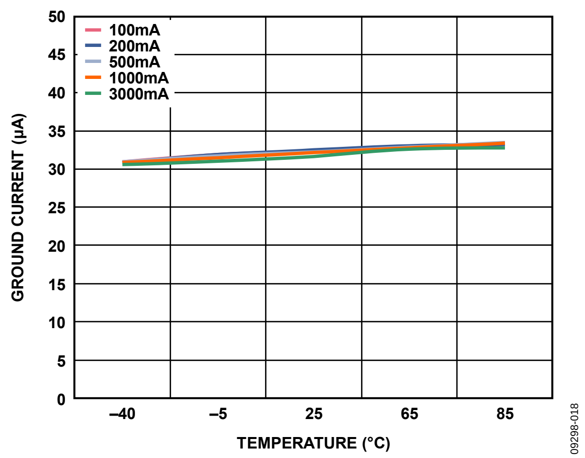

Figure 12. Ground Current vs. Temperature, Different Load Currents, V_{IN} = 5.5 V

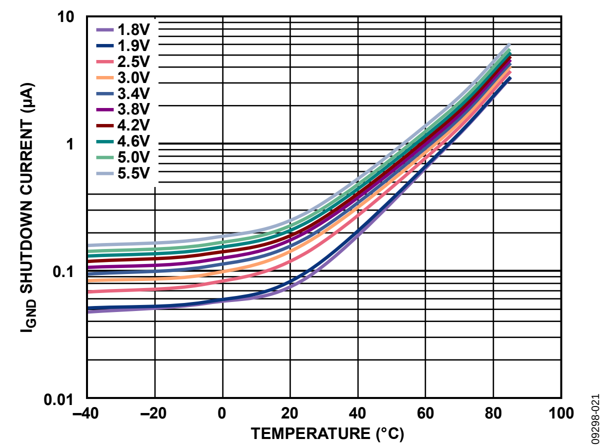

Figure 15. I_{GND} Shutdown Current vs. Temperature, V_{OUT} = 0 V, Different Input Voltages (V_{IN})

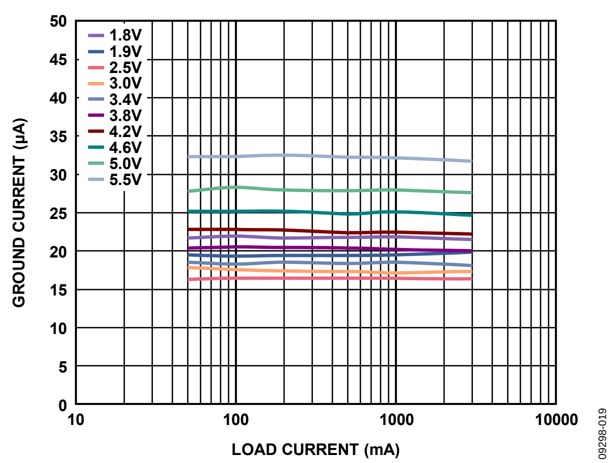

Figure 13. Ground Current vs. Load Current, Different Input Voltages (V_{IN})

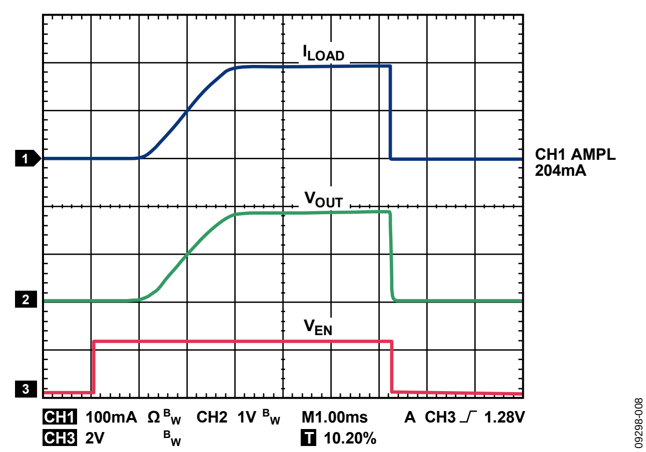

Figure 16. Typical Turn-On Time and Inrush Current, V_{IN} = 1.9 V, 200 mA Load

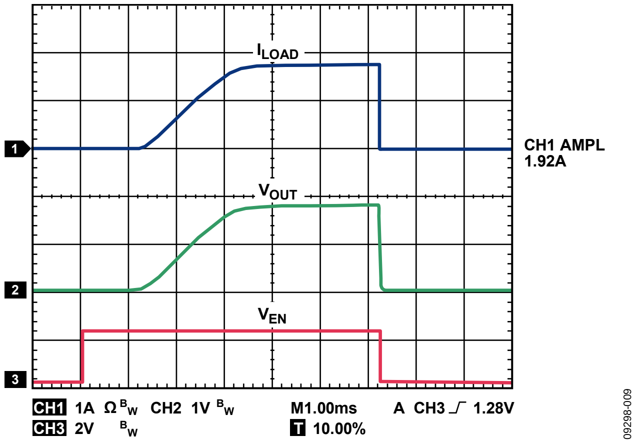

Figure 17. Typical Turn-On Time and Inrush Current, V_{IN} = 1.9 V, 2 A Load

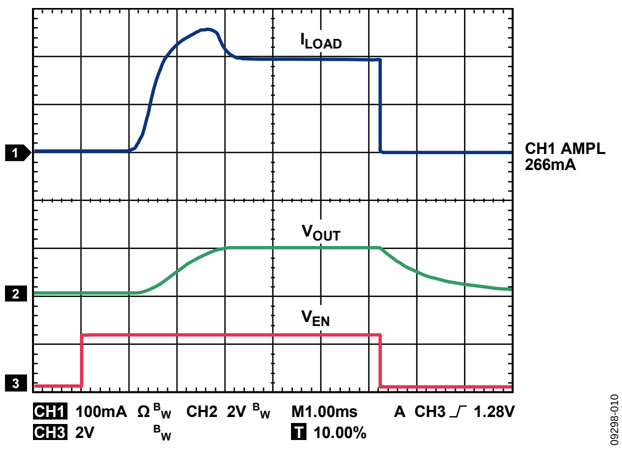

Figure 18. Typical Turn-On Time and Inrush Current, V_{IN} = 1.9 V, 200 mA Load, C_{OUT} = 100 µF

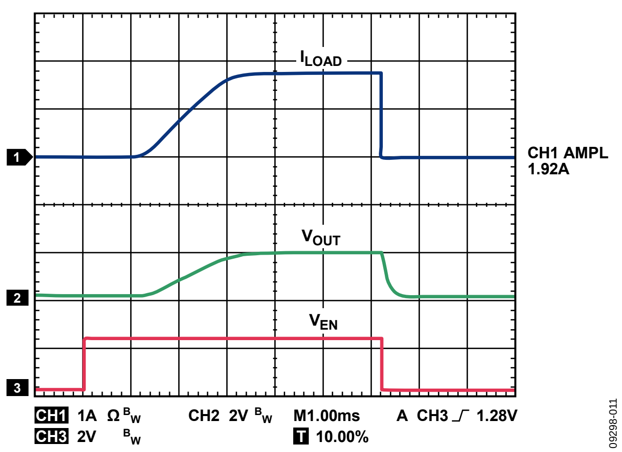

Figure 19. Typical Turn-On Time and Inrush Current, V_{IN} = 1.9 V, 2 A Load, C_{OUT} = 100 µF

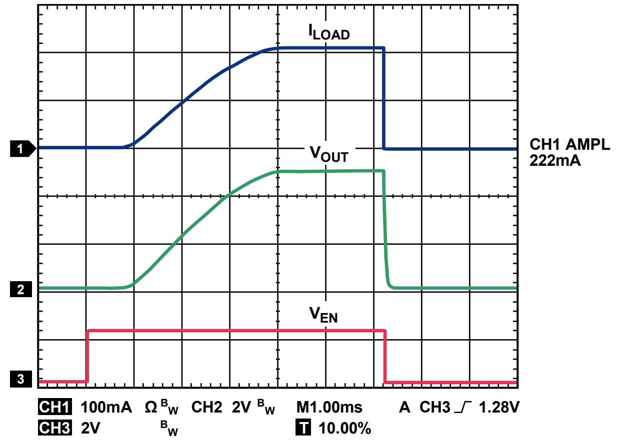

Figure 20. Typical Turn-On Time and Inrush Current, V_{IN} = 5.5 V, 200 mA Load

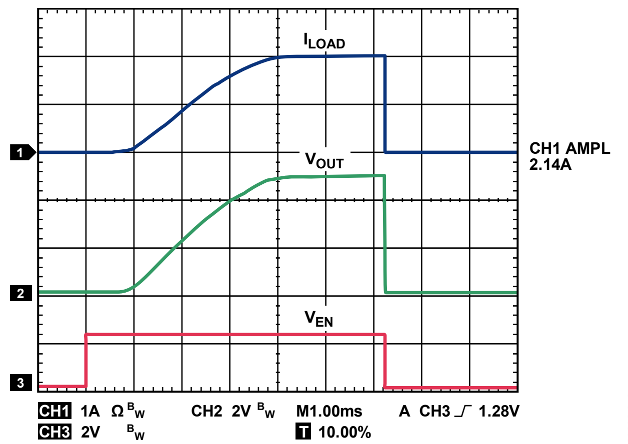

Figure 21. Typical Turn-On Time and Inrush Current, V_{IN} = 5.5 V, 2 A Load

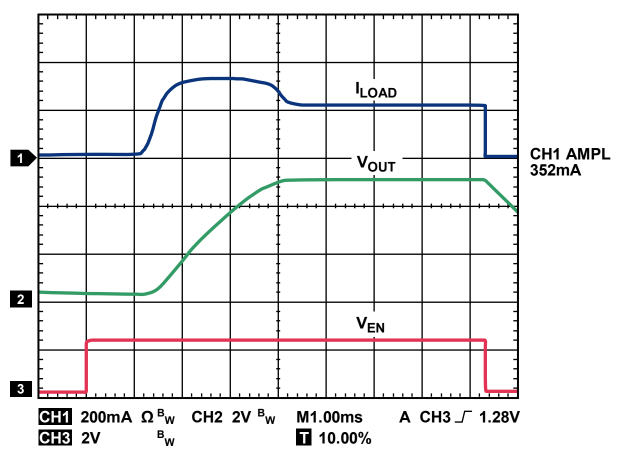

Figure 22. Typical Turn-On Time and Inrush Current, V_{IN} = 5.5 V, 200 mA Load, C_{OUT} = 100 µF

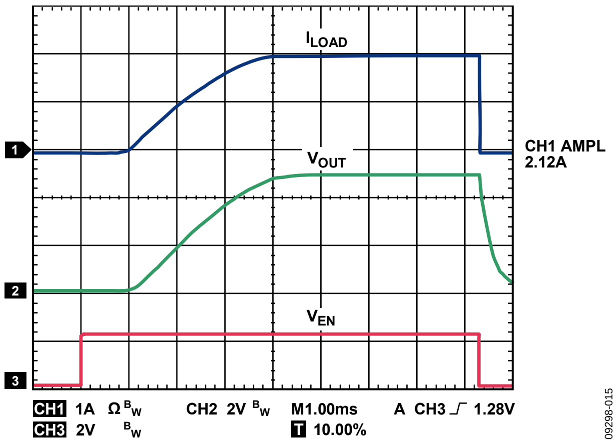

Figure 23. Typical Turn-On Time and Inrush Current, V_{IN} = 5.5 V, 2 A Load, C_{OUT} = 100 μF

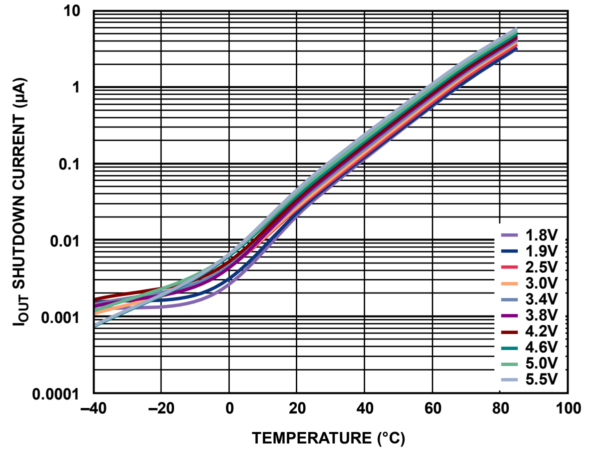

Figure 24. I_{OUT} Shutdown Current vs. Temperature, V_{OUT} = 0 V, Different Input Voltages (V_{IN})

THEORY OF OPERATION

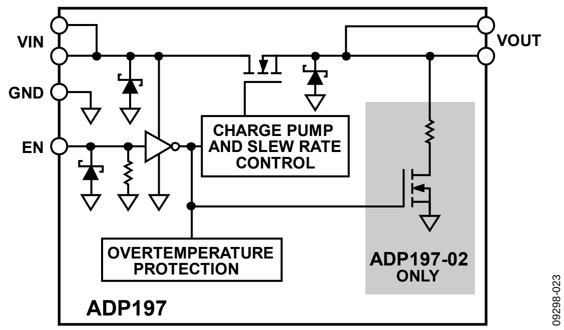

Figure 25. Functional Block Diagram

The ADP197 is a high-side NMOS load switch, controlled by an internal charge pump. The ADP197 is designed to operate with power supply voltages between 1.8 V and 5.5 V.

An internal charge pump biases the NMOS switch to achieve a relatively constant, ultralow on resistance of 12 mΩ across the entire input voltage range. The use of the internal charge pump also allows for controlled turn-on times. Turning the NMOS switch on and off is controlled by the enable input pin (EN), which is capable of interfacing directly with 1.8 V logic signals.

The ADP197 is capable of 3 A of continuous operating current as long as T_J is less than 70°C. At 85°C, the rated current drops to 2.22 A.

The overtemperature protection circuit activates if the load current causes the junction temperature to exceed 125°C. When this occurs, the overtemperature protection circuitry disables the output until the junction temperature falls below approximately 110°C, at which point the output is reenabled. If the fault condition persists, the output cycles off and on until the fault is removed.

The ADP197-02 incorporates a QOD circuit to discharge the output capacitance when the ADP197-02 output is disabled.

ESD protection structures are shown in the block diagram as Zener diodes.

The ADP197 is a low quiescent current device with a nominal 4 MΩ pull-down resistor on its EN pin. The package is a space-saving 1.0 mm × 1.5 mm, 0.5 mm pitch, 6-ball WLCSP and a tiny 2.0 mm × 2.0 mm × 0.55 mm, 0.65 mm pitch, 6-lead LFCSP.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP197 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors when the effective series resistance (ESR) value is carefully considered. The ESR of the output capacitor affects the response to load transients. A typical 1 µF capacitor with an ESR of 0.1 Ω or less is recommended for good transient response. Using a larger value of output capacitance improves the transient response to large changes in load current.

Input Bypass Capacitor

Connecting at least 1 µF of capacitance from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when high source impedance or long input traces are encountered. When greater than 1 µF of output capacitance is required, increase the input capacitor to match it.

GROUND CURRENT

The major source for ground current in the ADP197 is the internal charge pump for the FET drive circuitry. Figure 26 shows the typical ground current when $V_{EN} = V_{IN}$, and varies from 1.8 V to 5.5 V.

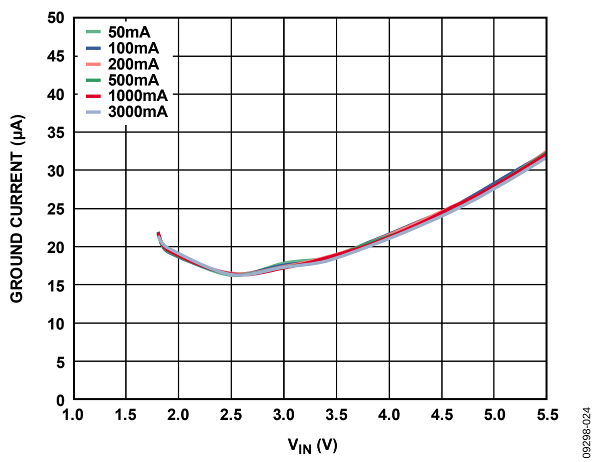

Figure 26. Ground Current vs. Input Voltage (V_{IN}), Different Load Currents

ENABLE FEATURE

The ADP197 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 27, when a rising voltage (V_{EN}) on the EN pin crosses the active threshold, VOUT turns on. When a falling voltage (V_{EN}) on the EN pin crosses the inactive threshold, VOUT turns off.

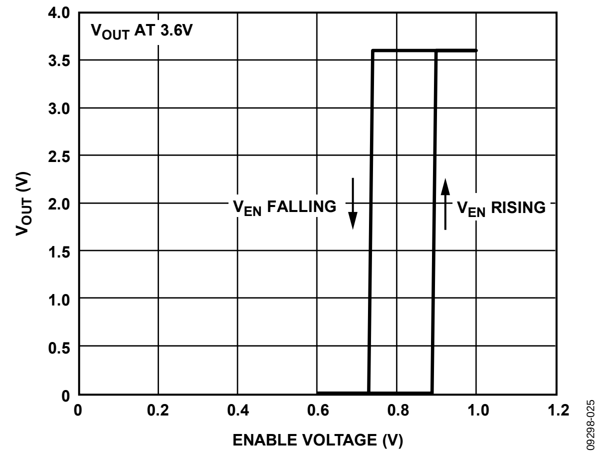

Figure 27. Typical EN Operation

As shown in Figure 27, the EN pin has hysteresis built into it. This built-in hysteresis prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active and inactive thresholds derive from the V_{IN} voltage; therefore, these thresholds vary with the changing input voltage. Figure 28 shows the typical EN active and inactive thresholds when the input voltage varies from 1.8 V to 5.5 V.

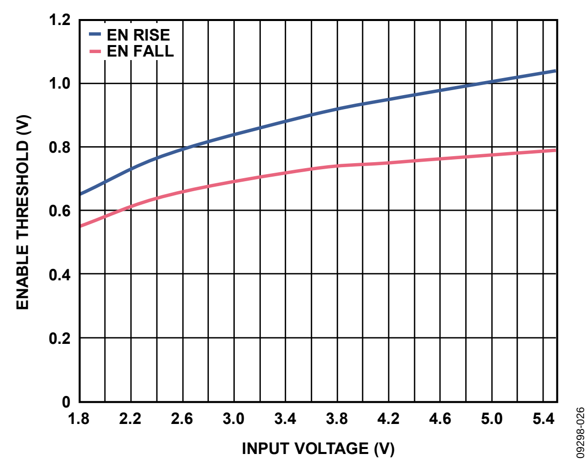

Figure 28. Typical EN Threshold vs. Input Voltage (V_{IN})

TIMING

Turn-on delay is defined as the interval between the time that V_{EN} exceeds the rising threshold voltage and when V_{OUT} rises to ~10% of its final value. The ADP197 includes circuitry that has a typical 1 ms turn-on delay and a controlled rise time to limit the V_{IN} inrush current. As shown in Figure 29 and Figure 30, the turn-on delay is nearly independent of the input voltage.

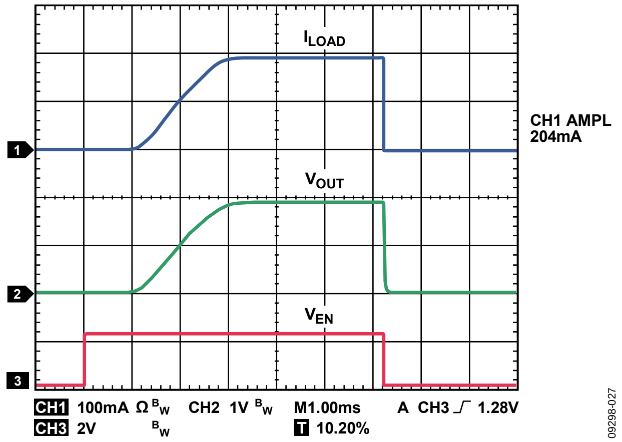

Figure 29. Typical Turn-On Delay Time with V_{IN} = 1.9 V, I_{LOAD} = 200 mA

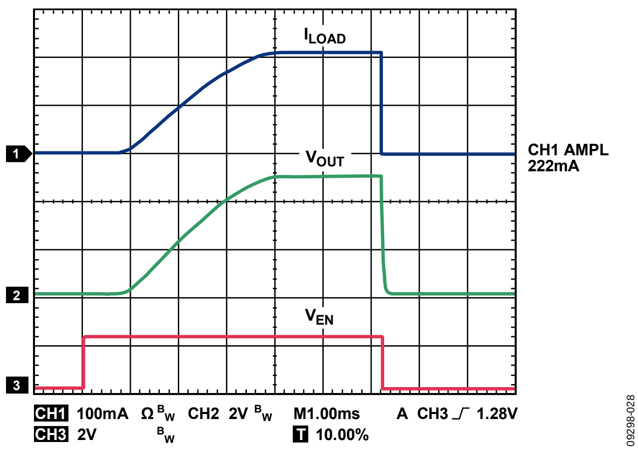

Figure 30. Typical Turn-On Delay Time with V_{IN} = 5.5 V, I_{LOAD} = 220 mA

The rise time is defined as the time it takes the output voltage to rise from 10% to 90% of V_{OUT} reaching its final value. It is dependent on the rise time of the internal charge pump.

For very large values of output capacitance, the RC time constant (where C is the load capacitance (C_{LOAD}) and R is the $RDS_{ON}||R_{LOAD}$) can become a factor in the rise time of the output voltage. Because RDS_{ON} is much smaller than R_{LOAD}, an adequate approximation for RC is $RDS_{ON} \times C_{LOAD}$. An input or load capacitor is not required for the ADP197 although capacitors can be used to suppress noise on the board. Figure 31 and Figure 32 show the inrush current when C_{LOAD} is 100 µF.

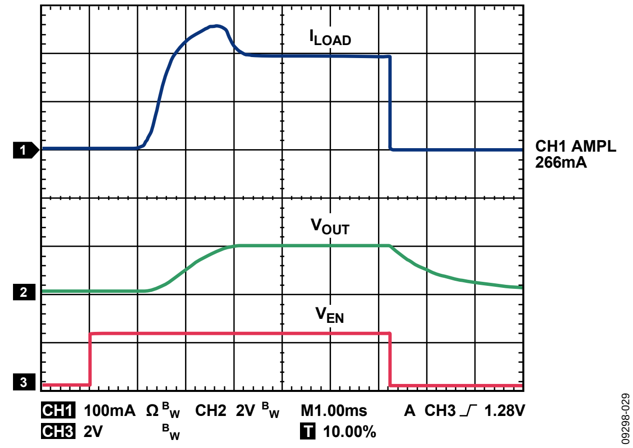

Figure 31. Typical Rise Time and Inrush Current, C_{LOAD} = 100 µF, V_{IN} = 1.9 V, I_{LOAD} = 270 mA

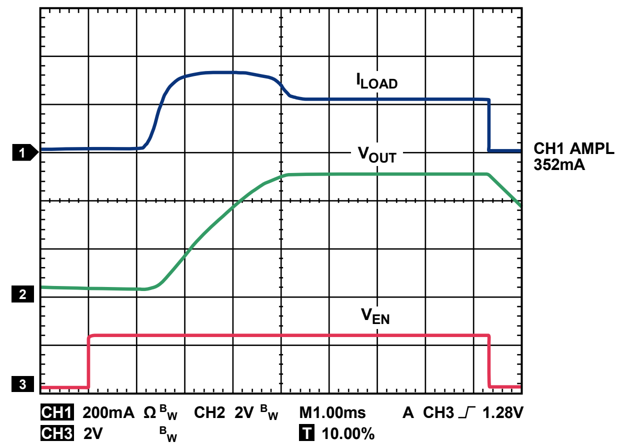

Figure 32. Typical Rise Time and Inrush Current, C_{LOAD} = 100 µF, V_{IN} = 5.5 V, I_{LOAD} = 350 mA

The turn-off time is defined as the time it takes for the output voltage to fall from 90% to 10% of V_{OUT} reaching its final value. It is also dependent on the RC time constant of the output capacitance and load resistance. Figure 33 shows the typical turn-off time with V_{IN} = 3.6 V, C_{OUT} = 1 µF, and R_{LOAD} = 18 Ω.

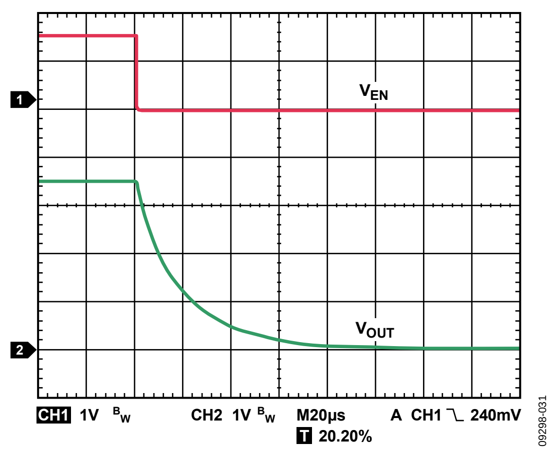

Figure 33. Typical Turn-Off Time

OUTLINE DIMENSIONS

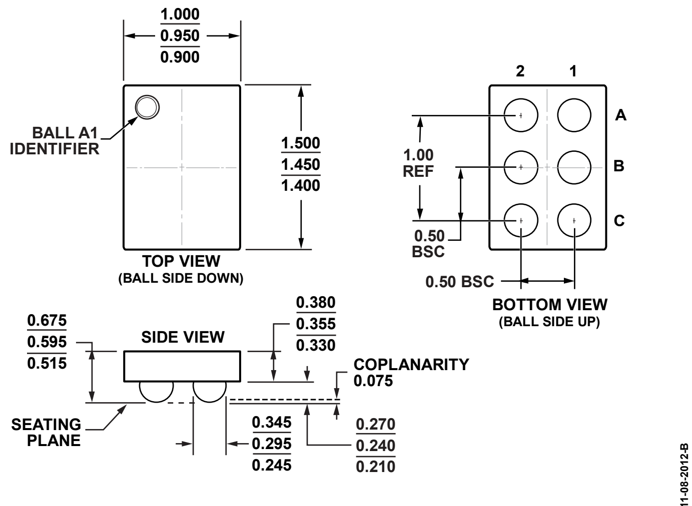

Figure 34. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-2)
Dimensions shown in millimeters

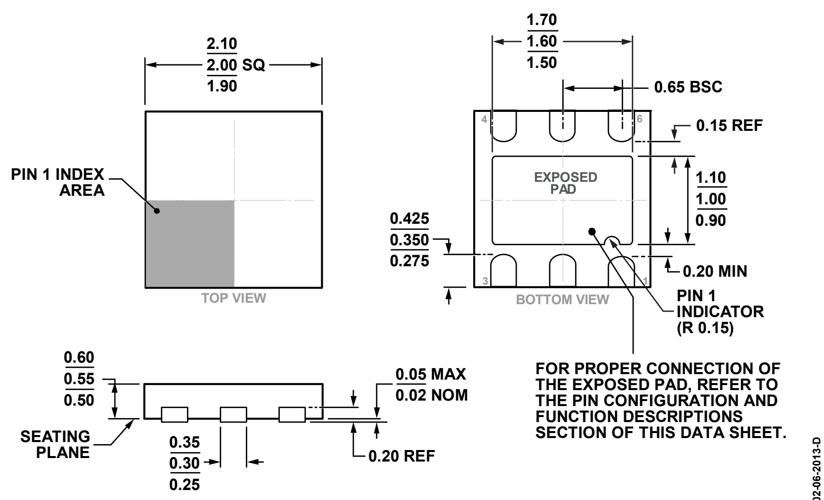

Figure 35. 6-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead
(CP-6-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	On/Off Time (µs)
ADP197ACBZ-R7	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	87	300
ADP197ACBZ-01-R7	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	AP	20
ADP197ACPZN-01-R7	−40°C to +85°C	6-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-6-3	AP	20
ADP197ACPZN-02-R7	−40°C to +85°C	6-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-6-3	D8	20
ADP197CB-EVALZ		Evaluation Board			
ADP197CP-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

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