LTC4228-1/LTC4228-2 Dual Ideal Diode and Hot Swap Controller

DESCRIPTION

Demonstration circuit 1899A controls two independent power rail circuits each with Hot Swap™ and ideal diode functionality provided by the LTC4228-1/LTC4228-2 dual ideal diode and Hot Swap controller.

DC1899A facilitates evaluation of LTC4228 performance in different operation modes such as supply ramp-up, power supply switchover, steady state, and overcurrent faults. Power supply switchover mode can be realized as either an ideal diode or as a prioritizer.

Each DC1899A circuit is assembled to operate with a 12V supply and 9A maximum current load. The main components of the board are the LTC4228 controller, two MOSFETs operating as ideal diodes, two MOSFETs operating as Hot Swap devices, two current sense resistors, two jumpers for independently enabling each rail, six LEDs to indicate status, power good and fault conditions separately for each channel, and input voltage snubbers. There are pads for optional RC circuits for each Hot Swap MOSFET gate in order to adjust output voltage slew rate. In addition to this there are jumpers allowing monitoring of supply undervoltage conditions at either IN or SENSE+ pins.

The standard configuration (as DC1899A populated by default) places the ideal diode MOSFET ahead of the Hot Swap MOSFET. The board also has pads for an alternative configuration with the Hot Swap MOSFET located ahead of the ideal diode MOSFET.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Range		2.9		18	V
$V_{INTVCC(UVL)}$	Internal V_{CC} Undervoltage Lockout	$INTV_{CC}$ Rising	2.1	2.2	2.3	V
$V_{INTVCC(HYST)}$	Internal V_{CC} Undervoltage Lockout Hysteresis		30	60	90	mV
Ideal Diode Control						
$\Delta V_{FWD(REG)}$	Forward Regulation Voltage ($V_{IN} - V_{OUT}$)		10	25	40	mV
ΔV_{DGATE}	External N-Channel Gate Drive ($V_{DGATE} - V_{IN}$)	ΔV_{FWD} = 0.1V IN < 7V IN = 7V to 18V	 5 10	 7 12	 14 14	 V V
$I_{CPO(UP)}$	CPO Pull-Up Current	CPO = IN = 2.9V CPO = IN = 18V	–60 –50	–95 –85	–120 –110	µA µA
$I_{DGATE(FPU)}$	DGATE Fast Pull-Up Current	ΔV_{FWD} = 0.2V, ΔV_{DGATE} = 0V, CPO = 17V		–1.5		A
$I_{DGATE(FPD)}$	DGATEn Fast Pull-Down Current	ΔV_{FWD} = –0.2V, ΔV_{DGATE} = 5V		1.5		A
Hot Swap Control						
$\Delta V_{SENSE(CB)}$	Circuit Breaker Trip Sense Voltage ($V_{SENSEEn}^+ - V_{SENSEEn}^-$)		47.5	50	52.5	mV
$\Delta V_{SENSE(ACL)}$	Active Current Limit Sense Voltage ($V_{SENSEEn}^+ - V_{SENSEEn}^-$)		55	65	75	mV
$I_{HGATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On, HGATE = 0V	–7	–10	–13	µA
$I_{HGATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off, OUT = 12V, HGATE = OUT + 5V	150	300	500	µA
$I_{HGATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn-Off, OUT = 12V, HGATE = OUT + 5V	100	200	300	mA

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input/Output Pin						
$V_{ON(TH)}$	ONn On Pin Threshold Voltage	ON Rising	1.21	1.235	1.26	V
$V_{ON(RESET)}$	ONn Pin Fault Reset Threshold Voltage	ON Falling	0.55	0.6	0.63	V
$V_{EN(TH)}$	$\overline{EN}$ Pin Threshold Voltage	$\overline{EN}$ Rising	1.185	1.235	1.284	V
$V_{TMR(TH)}$	TMRn Pin Threshold Voltage	TMR Rising TMR Falling	1.198 0.15	1.235 0.2	1.272 0.25	V V
$I_{TMR(UP)}$	TMRn Pin Pull-Up Current	TMR = 1V, In Fault Mode	–75	–100	–125	µA
$I_{TMR(DN)}$	TMRn Pin Pull-Down Current	TMR = 2V, No Faults	1.4	2	2.6	µA
$I_{TMR(RATIO)}$	TMRn Current Ratio $I_{TMR(DN)}/I_{TMR(UP)}$		1.4	2	2.7	%

OPERATING PRINCIPLES

The LTC4228 functions as an ideal diode with inrush current limiting and overcurrent protection by controlling two external back-to-back N-channel MOSFETs in a power path. The LTC4228 has two ideal diode and two Hot Swap controllers. Each ideal diode MOSFET is intended to operate with a defined Hot Swap MOSFET, because they are tied by common on/off control, and ideal diode controller sense voltage includes both MOSFETs and sense resistor voltage drop. Therefore, LTC4228 provides independent control for the two input supplies.

The LTC4228 gate drive amplifiers monitor the voltage between the INn and OUTn pins and drive the DGATEn pins. The amplifier quickly pulls up the DGATE pin, turning on the MOSFET (Q1 or Q3), for ideal diode control when it senses a large forward voltage drop. Pulling the ON pin high and $\overline{EN}$ pins low initiates a 100ms debounce timing cycle. After this timing cycle, a 10µA current source from the charge pump ramps up the HGATEn pin. When the Hot Swap MOSFET (Q2 or Q4) turns on, the inrush current is limited to a set level set by an external sense resistor placed between IN and SENSE pins.

An active current limit amplifier servos the gate of the Hot Swap MOSFET to 65mV across the current sense resistor. Inrush current can be further reduced, if desired, by adding a capacitor from HGATE to GND. When the MOSFET's gate overdrive (HGATE to OUT voltage) exceeds 4.2V, the PWRGD pin pulls low. When both MOSFETs (Q1 and Q2 or Q3 and Q4) are turned on, the gate drive amplifier controls DGATE to servo the forward voltage drop ($V_{IN} – V_{OUT}$) across the sense resistor and the back-to-back MOSFETs to 25mV. If the load current causes more than 25mV of voltage drop, the gate voltage rises to enhance the MOSFET used for ideal diode control. For large output currents the MOSFET's gate is driven fully on and the voltage drop is equal to the sum of the $I_{LOAD} • R_{DS(ON)}$ of the two MOSFETs in series.

In the case of an input supply short-circuit when the MOSFETs are conducting, a large reverse current starts flowing from the load towards the input. The gate drive amplifier detects this failure condition as soon as it appears and turns off the ideal diode MOSFET by pulling down the DGATE pin.

QUICK START PROCEDURE

Demonstration circuit 1899A can be easily set up to evaluate the performance of the LTC4228-1/LTC4228-2. Refer to the Figure 1 for proper measurement equipment setup and follow the procedure below. The DC1899A test includes independent tests of the LTC4228 Hot Swap functionality, ideal diode functionality and two power rails prioritizer functionality with the channel 1 highest priority.

HOT SWAP FUNCTIONALITY TEST

This test is identical for each 12V rail and is performed in the three steps by the measuring of the transient's parameters in the different operation modes.

Install the jumpers in the following positions:

JP4, RON1_SEL and JP5, RON2_SEL in position OFF;

JP1, EN1_SEL and JP2, EN2_SEL in position LOW.

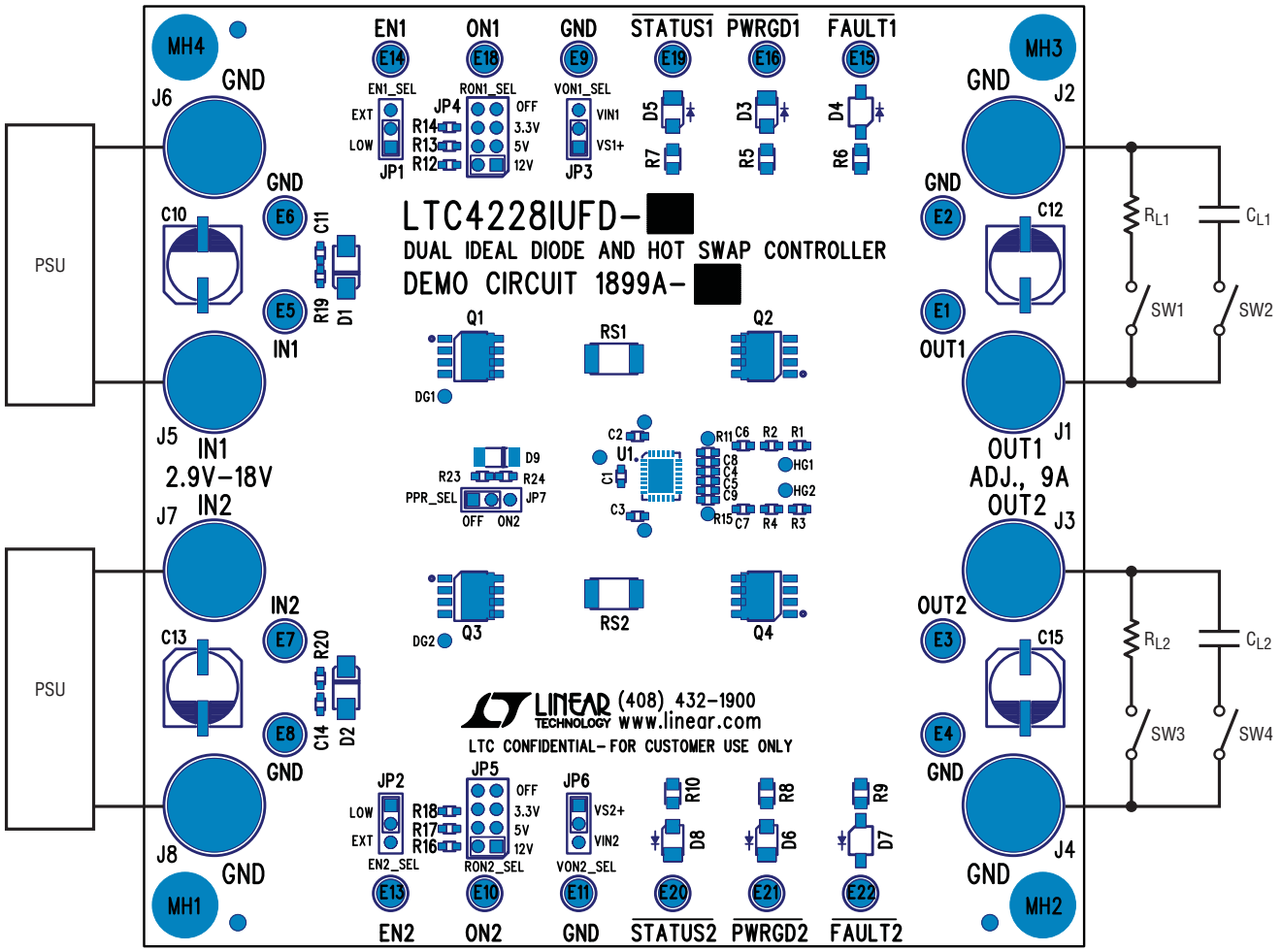


Figure 1. Measurement Equipment Setup for Hot Swap Functionality Test

QUICK START PROCEDURE

No-Load Rampup

Connect a 12V power supply to the board input turrets IN1 (IN2) and GND. Do not load the output. Place current probe on the 12V supply and voltage probes on the OUT1 (OUT2) turret. Provide ON1 (ON2) signal at the ON1 (ON2) pin by moving the RON1_SEL (RON2_SEL) jumper from OFF position to the 12V position. Observe the transient. The output voltage rise time should be in the range of 12ms to 29ms. PWRGD1 (PWRGD2) green LED should be lit. Turn off the rail using the RON1_SEL (RON2_SEL) jumper.

Current Limit

Initially adjust an electronic resistive load to 10Ω to 12Ω and connect it to the OUT1 (OUT2) turret and GND. Turn on the rail and slowly increase load current up to the circuit breaker threshold level. The current limit range should be between 9A and 12.3A. Turn off the rail using the RON1_SEL (RON2_SEL) jumper.

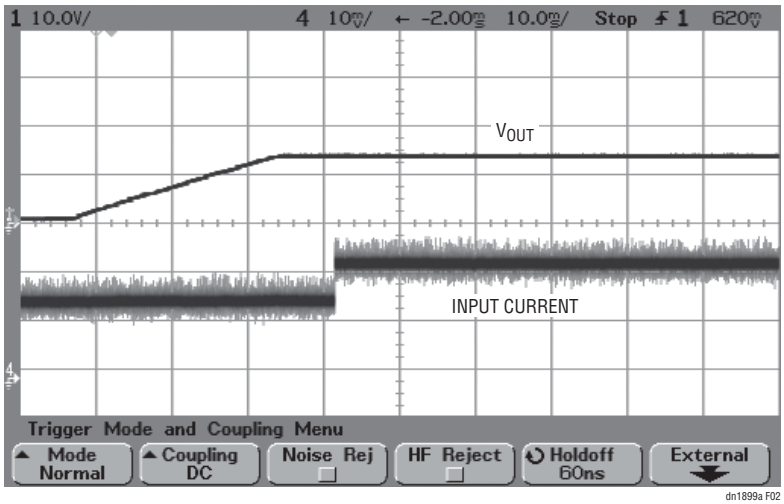


Figure 2. Turn-On Output Transient Test

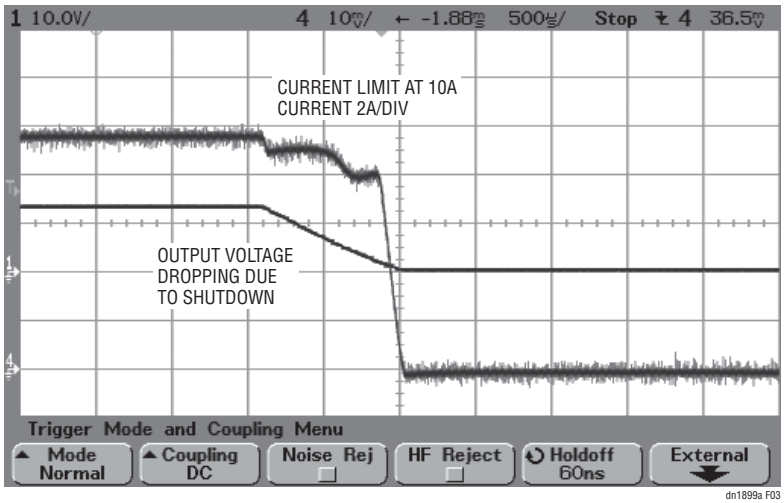


Figure 3. Current Limiting Test

QUICK START PROCEDURE

Power-Up into Output Short

Short the output to ground with a wire. Place the current probe on this wire. Turn on the rail and record the current shape. The maximum current should be in the 11.6A to 16.9A range. The LTC4228-1 latches off after overcurrent condition, but the LTC4228-2 automatically retries after 200ms to 450ms.

IDEAL DIODE FUNCTIONALITY TEST

Use an individual 12V power supply for each rail; connect the two outputs together at a common load. Adjust each input voltage to 12V with maximum possible accuracy. In this test, both rails are active and small variations in the input voltage will force one channel off and the other channel on. Place a voltmeter between IN1 and IN2 turrets to measure the difference between two input voltages. Activate both rails and keep a load around 1A to 3A. Adjust the input voltage level of one supply such that IN1 is 40mV more positive than IN2. Verify that only channel 1 is drawing current. Repeat this test with IN1 at –40mV with respect to IN2. In this case channel only channel 2 is drawing current.

PRIORITIZER FUNCTIONALITY TEST

The DC1899A is assembled with components to implement a power prioritizer with channel 1 having the higher priority. Place JP7 PPR_SEL (power priority select) jumper in position ON2 and JP5 RON2_SEL (ON2 select) in position OFF.

Apply independent supply voltages (12V) to both inputs. Channel 1 will be connected to load. Reduce channel 1 input voltage until it reaches an undervoltage condition and D6 (PWRGD2) lights. At the same time channel 2 power supply will deliver power to the load.

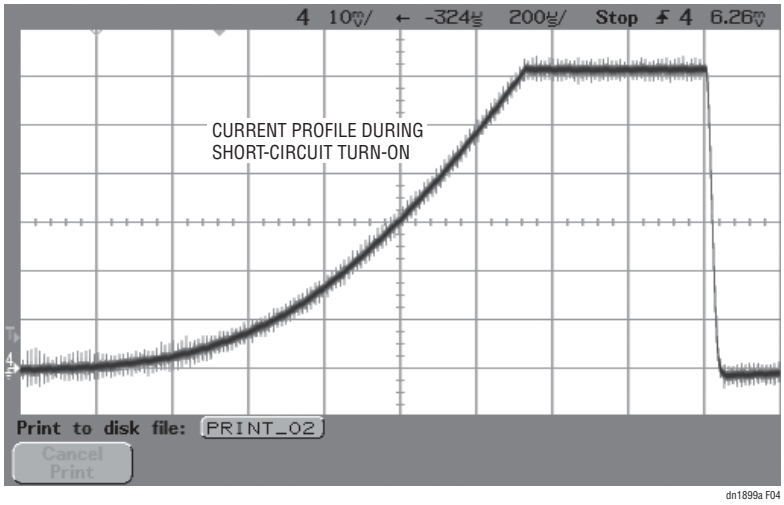
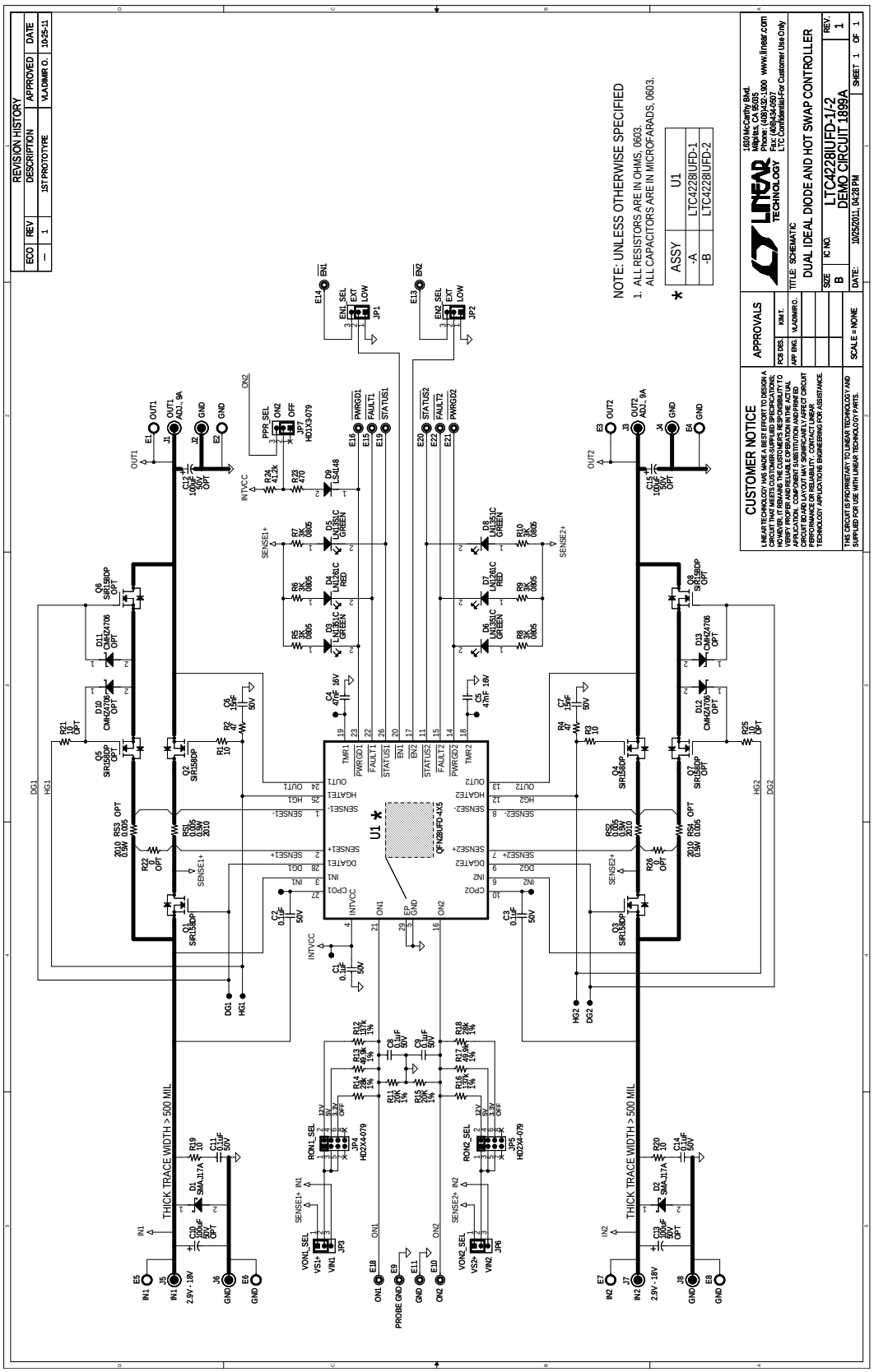


Figure 4. Short-Circuit Test (2A/Div)

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	7	C1, C2, C3, C8, C9, C11, C14	CAP., X7R, 0.1µF, 50V, 0603	AVX, 06035C104KAT
2	2	C4, C5	CAP., X7R, 47nF, 50V, 0603	AVX, 06035C473KAT
3	2	C6, C7	CAP., X7R, 15nF, 50V, 0603	AVX, 06035C153KAT
4	0	C10, C12, C13, C15	CAP., ALUMINUM, 100µF 50V, OPT	SANYO, 50CE100BS
5	2	D1, D2	DIODE, VOLTAGE SUPP. 19V 5%, SMA-DIODE	VISHAY, SMAJ17A-E3
6	4	D3, D5, D6, D8	LED, SMT GREEN, J TYPE, LED-LN1351C-GREEN	PANASONIC, LN1351C-TR
7	2	D4, D7	LED, SMT RED, GW TYPE, LED-LN1261C-RED	PANASONIC, LN1261C-TR
8	1	D9	DIODE, SWITCHING, SOD80	VISHAY, LS4148-GS18
9	0	D10, D11, D12, D13	DIODE, CMHZ4706, SOD123	OPT
10	8	E1, E2, E3, E4, E5, E6, E7, E8	TP, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
11	12	E9, E10, E11, E13-E16, E18-E22	TP, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
12	5	JP1, JP2, JP3, JP6, JP7	JMP, HD1X3, 0.079CC	SAMTEC, TMM-103-02-L-S
13	2	JP4, JP5	JMP, HD2X4, 0.079CC	SAMTEC, TMM-104-02-L-D
14	8	J1, J2, J3, J4, J5, J6, J7, J8	JACK, BANANA	KEYSTONE, 575-4
15	4	Q1, Q2, Q3, Q4	MOSFET, N-CH, 30-V, SO8-POWERPAK	VISHAY, SiR158DP
16	0	Q5, Q6, Q7, Q8	MOSFET, N-CH, 30-V, SiR158DP, SO8-POWERPAK	OPT
17	2	RS1, RS2	RES., CHIP, 0.005, 1/2W, 1%, 2010	VISHAY, WSL20105L000FEA
18	0	RS3, RS4	RES., CHIP, 0.005, 1/2W, 1%, 2010, OPT	VISHAY, WSL20105L000FEA
19	4	R1, R3, R19, R20	RES., CHIP, 10Ω, 1%, 0603	VISHAY, CRCW060310R0FKEA
20	2	R2, R4	RES., CHIP, 47Ω, 1%, 0603	VISHAY, CRCW060347R0FKEA
21	6	R5, R6, R7, R8, R9, R10	RES., CHIP, 3k, 1%, 0805	VISHAY, CRCW08053K00FKEA
22	2	R11, R15	RES., CHIP, 20k, 1%, 0603	VISHAY, CRCW0060320K0FKEA
23	2	R12, R16	RES., CHIP, 137k, 1%, 0603	VISHAY, CRCW0603137KFKEA
24	2	R13, R17	RES., CHIP, 49.9k, 1%, 0603	VISHAY, CRCW060349K9FKEA
25	2	R14, R18	RES., CHIP, 28k, 1%, 0603	VISHAY, CRCW0060328K0FKEA
26	0	R21, R25	RES., CHIP, 10Ω, 0603	OPT
27	0	R22, R26	RES., CHIP, 0Ω, 0603	OPT
28	1	R23	RES., CHIP, 470Ω, 1%, 0603	VISHAY, CRCW0603470RFKEA
29	1	R24	RES., CHIP, 41.2k, 1%, 0603	VISHAY, CRCW0060341K2FKEA
DC1899A-A Assembly				
2	1	U1	I.C. LTC4228IUFD-1, QFN28UFD	LINEAR TECH., LTC4228IUFD-1
DC1899A-A Assembly				
2	1	U1	I.C. LTC4228IUFD-2, QFN28UFD	LINEAR TECH., LTC4228IUFD-2

SCHEMATIC DIAGRAM



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Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035