Bidirectional, Synchronous PWM Controller for Battery Test and Formation

Data Sheet

ADP1974

FEATURES

- Input voltage range: 6 V to 60 V
- On-board 5 V linear regulator
- Buck/charge or boost/discharge mode
- High PWM linearity with internal 4 V p-p PWM ramp voltage
- FAULT and COMP input compatible with AD8450/AD8451
- Programmable dead time control
- Adjustable frequency from 50 kHz to 300 kHz
- Synchronization output or input with adjustable phase shift
- Programmable maximum duty cycle
- Programmable soft start
- Peak hiccup current-limit protection
- Pin-compatible with ADP1972 (asynchronous version)
- TSD protection
- 16-lead TSSOP

APPLICATIONS

- Single and multicell battery formation and testing
- High efficiency battery test systems with recycle capability
- Battery conditioning (charging and discharging) systems
- Compatible with AD8450/AD8451 constant voltage (CV) and constant current (CC) analog front end error amplifier

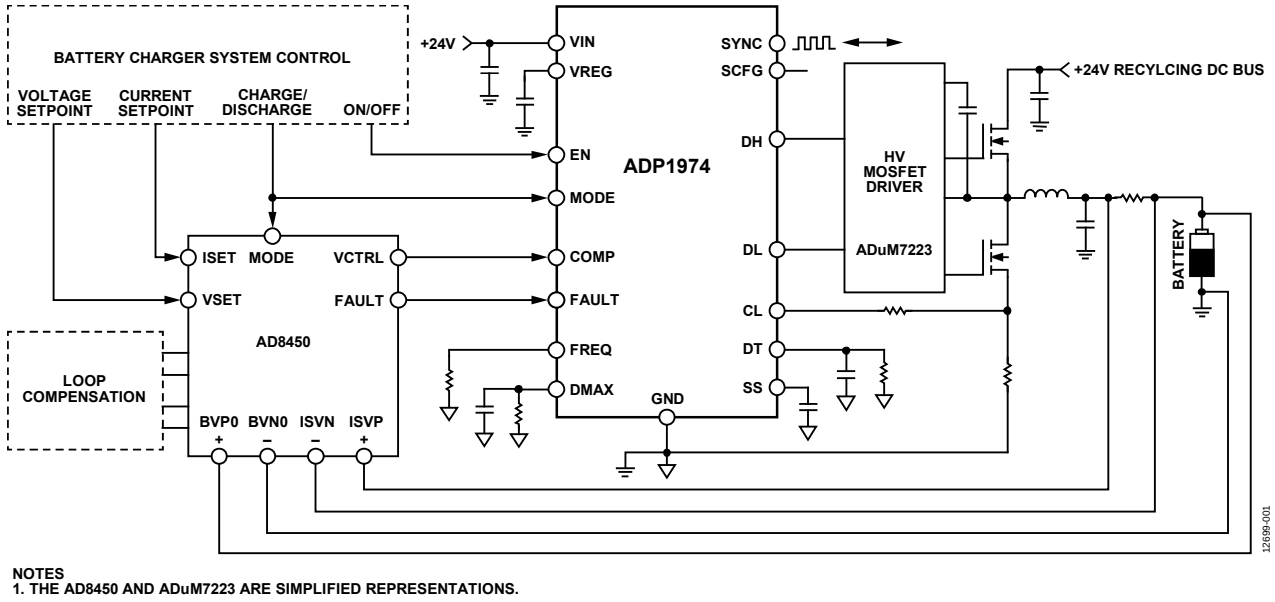
GENERAL DESCRIPTION

The ADP1974 is a constant frequency, voltage mode, synchronous, pulse-width modulation (PWM) controller for bidirectional dc-to-dc applications. The ADP1974 is designed for use in battery testing, formation, and conditioning applications with an external, high voltage field effect transistor (FET) half bridge driver, and an external control device such as the AD8450/AD8451. The device operates as a buck converter in battery charge mode and as a boost converter in discharge mode to recycle energy to the input bus.

The ADP1974 high voltage VIN supply pin can withstand a maximum operating voltage of 60 V and reduces the need for additional system supply voltages. The ADP1974 has integrated features such as precision enable, internal and external synchronization control with programmable phase shift, programmable maximum duty cycle, dead time control, and peak hiccup current-limit protection. Additional protection features include soft start to limit input inrush current during startup, precision enable, and thermal shutdown (TSD). The ADP1974 also has a COMP pin to provide external control of the PWM duty cycle and a FAULT pin that can disable the DH and DL outputs. These functions are compatible with the AD8450/AD8451 analog front-end (AFE) error amplifiers.

The ADP1974 is available in a 16-lead TSSOP package and is pin-compatible with the ADP1972.

TYPICAL APPLICATION CIRCUIT



NOTES
1. THE AD8450 AND ADuM7223 ARE SIMPLIFIED REPRESENTATIONS.

Figure 1.

Rev. 0

Document Feedback

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REVISION HISTORY

9/15—Revision 0: Initial Version

SPECIFICATIONS

VIN = 24 V and specifications valid for T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_A = 25°C. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE (VIN)						
Voltage Range	V_{IN}		6		60	V
VIN Supply Current	I_{VIN}	R_{FREQ} = 100 kΩ, V_{SS} = 0 V, SYNC floating, FAULT = low, EN = high		1.5	2.5	mA
VIN Shutdown Current	I_{SHDN}	V_{EN} = 0 V		15	70	µA
UVLO Threshold Rising		V_{IN} rising		5.71	6	V
UVLO Threshold Falling		V_{IN} falling	5.1	5.34		V
SOFT START (SS)						
SS Pin Current	I_{SS}	V_{SS} = 0 V	4	5	6	µA
SS Threshold Rising		Switching enable threshold		0.52	0.65	V
SS Threshold Falling		Switching disable threshold	0.4	0.5		V
End of Soft Start		Asynchronous to synchronous threshold	4.4	4.5	4.6	V
PWM CONTROL						
FREQ						
Frequency Range	f_{SET}	R_{FREQ} = 33.2 kΩ to 200 kΩ	50		300	kHz
Oscillator Frequency	f_{OSC}	R_{FREQ} = 100 kΩ	90	100	110	kHz
FREQ Pin Voltage	V_{FREQ}	R_{FREQ} = 100 kΩ	1.2	1.252	1.3	V
SYNC Output (Internal Frequency Control)		V_{SCFG} ≥ 4.53 V or SCFG pin floating				
Internal SYNC Range	f_{SET}	For SYNC output	50		300	kHz
SYNC Output Clock Duty Cycle		V_{SCFG} = V_{VREG}, R_{FREQ} = 100 kΩ	40	50	60	%
SYNC Sink Resistance	R_{SYNC}	V_{SCFG} = 5 V, I_{SYNC} = 10 mA		10	20	Ω
SYNC Input (External Frequency Control)		V_{SCFG} < 4.25 V				
External SYNC Range	f_{SYNC}	For SYNC input clock	50		300	kHz
SYNC Pull-Down Resistor			0.5	1	1.5	MΩ
Maximum SYNC Pin Voltage	V_{SYNC}				5.5	V
SYNC Threshold Rising				1.2	1.5	V
SYNC Threshold Falling			0.7	1.05		V
Minimum Pulse Width				100		ns
SCFG	V_{SCFG}					
SCFG High Threshold Rising		SYNC set to input		4.53	4.7	V
SCFG High Threshold Falling		SYNC set to output	4.25	4.51		V
SCFG Low Threshold Rising		Programmable phase shift above threshold		0.52	0.65	V
SCFG Low Threshold Falling		No phase shift	0.4	0.5		V
SCFG Pin Current	I_{ISCFG}	R_{FREQ} = 100 kΩ, V_{SCFG} = GND	9.5	11	12.5	µA
DMAX						
Maximum Internal Duty Cycle		V_{COMP}, V_{DMAX}, V_{SS}, and V_{SCFG} = 5 V		97		%
DMAX Setting Current	I_{DMAX}	V_{DMAX} = 0 V, R_{FREQ} = 100 kΩ	9.5	11	12.5	µA
DMAX and SCFG Current Matching[1]					10	%
COMP						
COMP Pin Input Voltage Range	V_{COMP}		0		5.0	V
Internal Peak-to-Peak Ramp Voltage	V p-p			4		V p-p
Maximum Internal Ramp Voltage				4.5		V
Minimum Internal Ramp Voltage			0.45	0.5	0.55	V
DT						
DT Pin Current	I_{DT}	R_{FREQ} = 100 kΩ, V_{DT} = GND		20	22	µA
Maximum DT Programming Voltage	V_{DT}				3.5	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PRECISION ENABLE LOGIC (EN)						
Maximum EN Pin Voltage					60	V
EN Threshold Rising				1.25	1.4	V
EN Threshold Falling			1.1	1.22		V
EN Pin Current		V_{EN} = 5 V, internal pull down		0.32	2	µA
MODE LOGIC						
Maximum MODE Pin Voltage					5.5	V
MODE Threshold Rising				1.20	1.5	V
MODE Threshold Falling			0.7	1.05		V
CURRENT LIMIT (CL)						
Set Current	I_{CL}	V_{CL} = 0 V	18	20	21	µA
Buck CL Threshold	$V_{CL\ (BUCK)}$		250	300	350	mV
Buck Negative Current Threshold	$V_{NC\ (BUCK)}$		400	450	500	mV
Boost CL Threshold	$V_{CL\ (BOOST)}$		450	500	550	mV
Hiccup Detect Time		R_{FREQ} = 100 kΩ, 500 consecutive clock pulses		5.2		ms
Hiccup Off Time		R_{FREQ} = 100 kΩ, 500 consecutive clock pulses		5.2		ms
VREG		EN = high				
LDO Regulator Output Voltage	V_{VREG}	V_{IN} = 6 V to 60 V, no external load	4.9	5	5.1	V
Guaranteed Output Current	$I_{OUT\ (MAX)}$	V_{IN} = 6 V, external load			5	mA
Load Regulation		V_{IN} = 6 V, I_{OUT} = 0 mA to 5 mA	4.9	5	5.1	V
FAULT						
Maximum FAULT Pin Voltage	V_{FAULT}				60	V
FAULT Threshold Rising				1.2	1.5	V
FAULT Threshold Falling			0.7	1.05		V
FAULT Pin Current		V_{FAULT} = 5 V, internal 8.5 MΩ pull-down resistor		0.49	2	µA
PWM DRIVE LOGIC SIGNALS (DH/DL)						
DL Drive Voltage	V_{DL}	No load		VREG		V
DH Drive Voltage	V_{DH}	No load		VREG		V
DL and DH Sink Resistance		I_{DL} = 10 mA		1.2	2.4	Ω
DL and DH Source Resistance		I_{DL} = 10 mA		1.4	2.6	Ω
DL and DH Pull-Down Resistor			0.5	1	1.5	MΩ
THERMAL SHUTDOWN (TSD)						
TSD Threshold Rising				150		°C
TSD Threshold Falling				135		°C

[1] The DMAX and SCFG current matching specification is calculated by taking the absolute value of the difference between the measured I_{SCFG} and I_{DMAX} currents, dividing them by the 11 µA typical value, and multiplying this answer by 100.

$$DMAX\ and\ SCFG\ Current\ Matching\ (\%) = \left[\frac{I_{SCFG} - I_{DMAX}}{11\,\mu A}\right] \times 100$$

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN, FAULT to GND	−0.3 V to +61 V
SYNC, COMP, MODE, VREG to GND	−0.3 V to +5.5 V
DH, DL, SS, DMAX, SCFG, CL, DT, FREQ to GND	−0.3 V to VREG + 0.3 V
Operating Ambient Temperature Range	−40°C to +85°C
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination.

THERMAL OPERATING RANGES

The ADP1974 can be damaged when the junction temperature limits are exceeded. The maximum operating junction temperature ($T_{J\ MAX}$) takes precedence over the maximum operating ambient temperature ($T_{A\ MAX}$). Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits.

In applications with high power dissipation and poor printed circuit board (PCB) thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit when the junction temperature is within specification limits.

The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction to ambient thermal resistance of the package (θ_{JA}). Use the following equation to calculate the maximum junction temperature (T_J) from the ambient temperature (T_A) and power dissipation (P_D):

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

For additional information on thermal resistance, refer to Application Note AN-000, *Thermal Characteristics of IC Assembly*.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

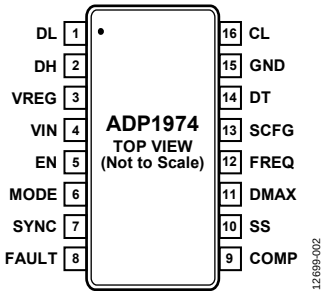

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DL	Logic Drive Output for the External Low-Side MOSFET Driver.
2	DH	Logic Drive Output for the External High-Side MOSFET Driver.
3	VREG	Internal Voltage Regulator Output and Internal Bias Supply. A bypass capacitance of 1 µF or greater from this pin to ground is required.
4	VIN	High Input Voltage Supply Pin (6 V to 60 V). Bypass this pin with a 4.7 µF capacitor to ground.
5	EN	Logic Enable Input. Drive EN logic low to shut down the device. Drive EN logic high to turn on the device.
6	MODE	Mode Select. Drive MODE logic low to place the device in boost (recycle) mode. Drive MODE logic high to place the device in buck (charge) mode of operation. The MODE status is sampled at EN rising or FAULT falling (see the Operating Modes section).
7	SYNC	Synchronization Pin. This pin is configured as an input (slave mode) with SCFG < 4.51 V to synchronize the ADP1974 to an external clock. This pin is an open-collector driver output with SCFG > 4.53 V (or SCFG connected to VREG). When configured as an output, SYNC is used to synchronize with other channels; a 10 kΩ resistor to VREG can be used as a pull-up.
8	FAULT	Fault Input Pin. Drive FAULT low to disable the DL and DH drivers in the event of a fault. Drive FAULT high to enable the DL and DH drivers. FAULT can also reset the mode of operation as described in the Operating Modes section. This pin was designed to interface with the overcurrent protection (OCP) or overvoltage protection (OVP) fault condition on the AD8450/AD8451.
9	COMP	PWM Modulator Input. This pin interfaces with an error amplifier output signal from the AD8450/AD8451. The signal on this pin is compared internally to the linear ramp to produce the PWM signal. Do not leave this pin floating; see the External COMP Control section for additional details.
10	SS	Soft Start Control Pin. A capacitor connected from SS to ground sets the soft start ramp time. Soft start controls the DL and DL duty cycle during power-up to reduce the inrush current. Drive SS below 0.5 V to disable switching of DL and DH. During soft start, the ADP1974 operates in pseudosynchronous mode (see the Soft Start section).
11	DMAX	Maximum Duty Cycle Input. Connect an external resistor to ground to set the maximum duty cycle. If the 97% internal maximum duty cycle is sufficient for the application, tie this pin to VREG. If DMAX is left floating, this pin is internally pulled up to VREG.
12	FREQ	Frequency Set Pin. Connect an external resistor between this pin and ground to set the frequency between 50 kHz and 300 kHz. When the ADP1974 is synchronized to an external clock (slave mode), set the slave frequency to 90% of the master frequency by multiplying the master R_{FREQ} value times 1.11.
13	SCFG	Synchronization Configuration Input. Drive $V_{SCFG} \geq 4.53$ V (typical) to configure SYNC as an output clock signal. Drive $V_{SCFG} < 4.51$ V (typical) to configure SYNC as an input. Connect a resistor to ground with $0.52 \text{ V} < V_{SCFG} < 4.53$ V (typical) to introduce a phase shift to the synchronized clock. Drive $V_{SCFG} \leq 0.5$ V (typical) to configure SYNC as an input with no phase shift. If SCFG is left floating, the SYNC pin is internally tied to VREG, and SYNC is configured as an output.
14	DT	Dead Time Programming Pin. Connect an external resistor between this pin and ground to set the dead time. Do not leave this pin floating.
15	GND	Power and Analog Ground Pin.
16	CL	Current-Limit Programming Pin. Connect a current sense resistor in series with the low-side FET source to measure the peak current in the inductor. The current-limit thresholds can operate with a 20 kΩ resistor as described in the Peak Current-Limit Hiccup Implementation section.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = V_{EN} = V_{FAULT} = 24$ V, $V_{MODE} = V_{CL} = V_{SS} = V_{COMP} = 0$ V, $T_A = 25°C$, unless otherwise noted.

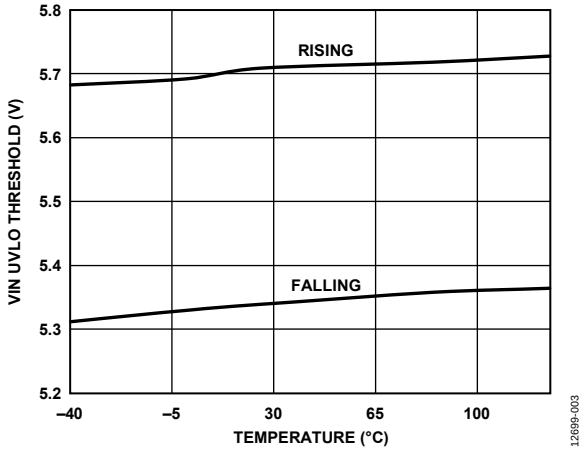

Figure 3. Input Voltage (V_{IN}) UVLO Threshold vs. Temperature, $V_{FAULT} = 0$ V

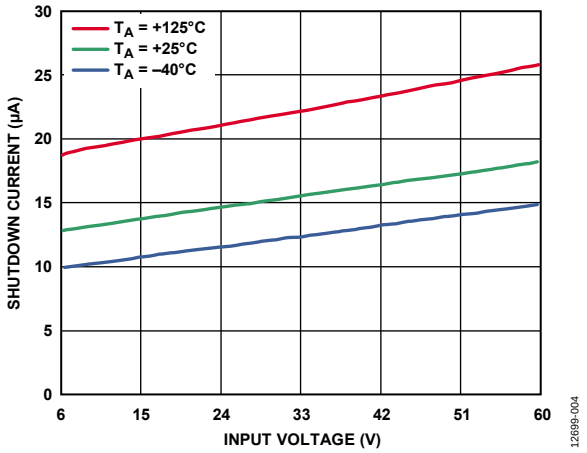

Figure 4. Shutdown Current vs. Input Voltage, $V_{EN} = 0$ V and $V_{FAULT} = 0$ V

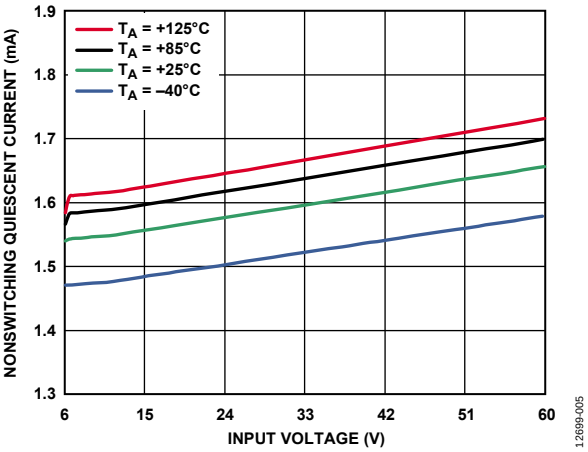

Figure 5. Nonswitching Quiescent Current vs. Input Voltage (SYNC = Floating)

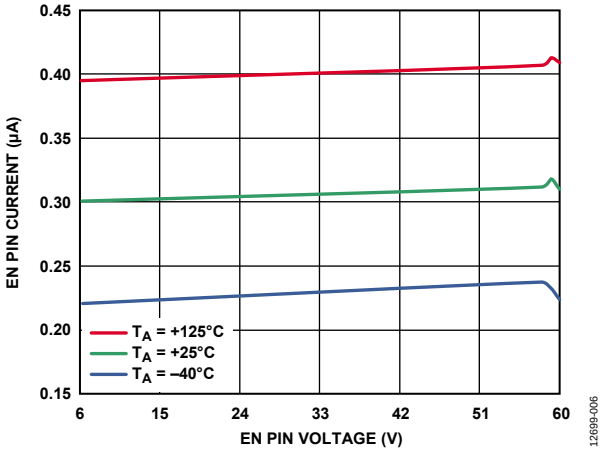

Figure 6. EN Pin Current vs. EN Pin Voltage, $V_{EN} = 5$ V and $V_{FAULT} = 0$ V

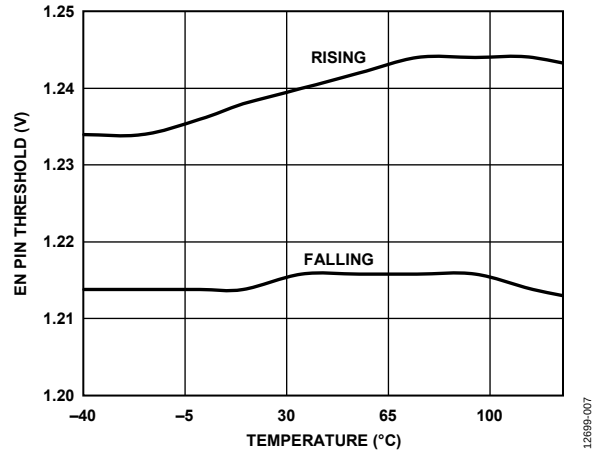

Figure 7. EN Pin Threshold vs. Temperature, $V_{FAULT} = 0$ V

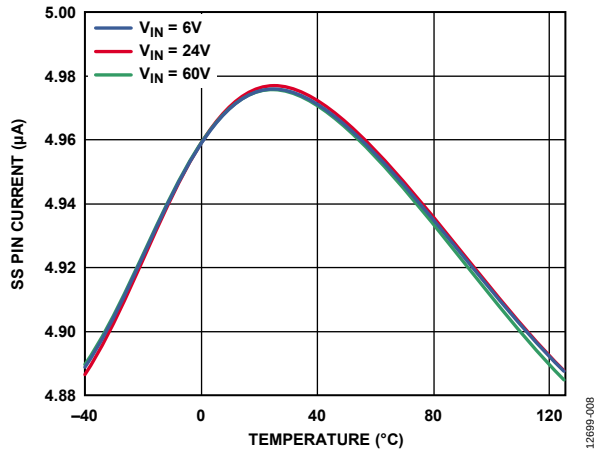

Figure 8. SS Pin Current vs. Temperature

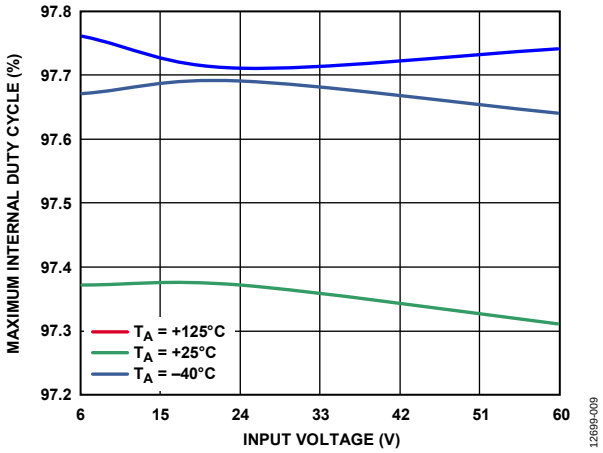

Figure 9. Maximum Internal Duty Cycle vs. Input Voltage, R_{FREQ} = 100 kΩ, V_{COMP} = 5 V, and No Load on DL, DH, or DMAX

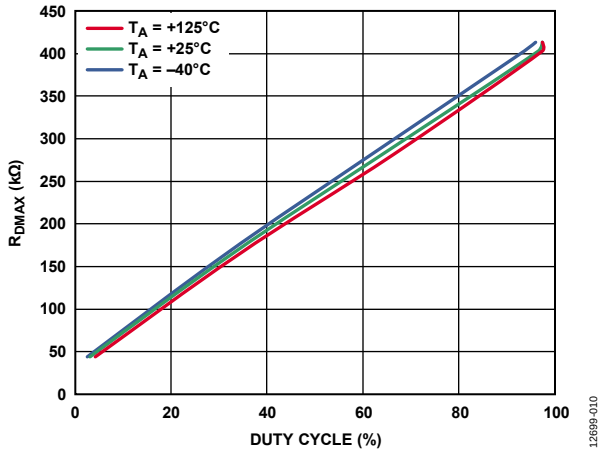

Figure 10. R_{DMAX} vs. Duty Cycle, R_{FREQ} = 100 kΩ, V_{COMP} = 5 V, and No Load on DL or DH

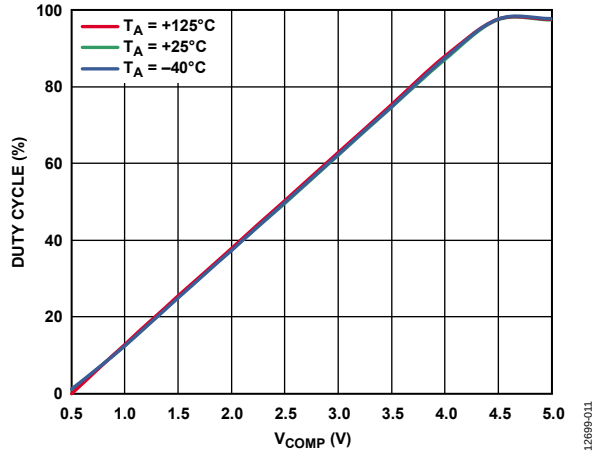

Figure 11. Duty Cycle vs. V_{COMP}, R_{FREQ} = 100 kΩ, and No Load on DL, DH, or DMAX

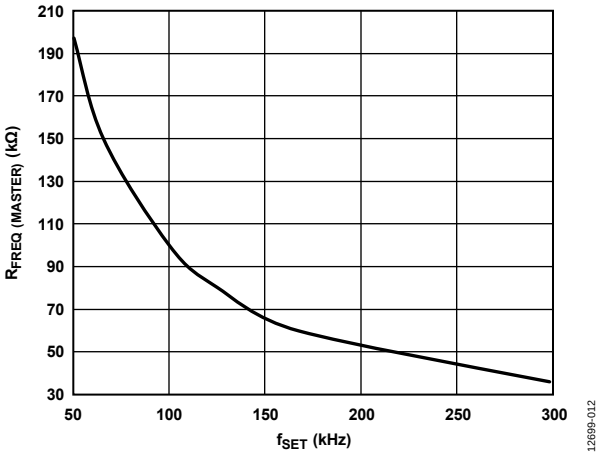

Figure 12. $R_{FREQ\ (MASTER)}$ vs. Switching Frequency (f_{SET})

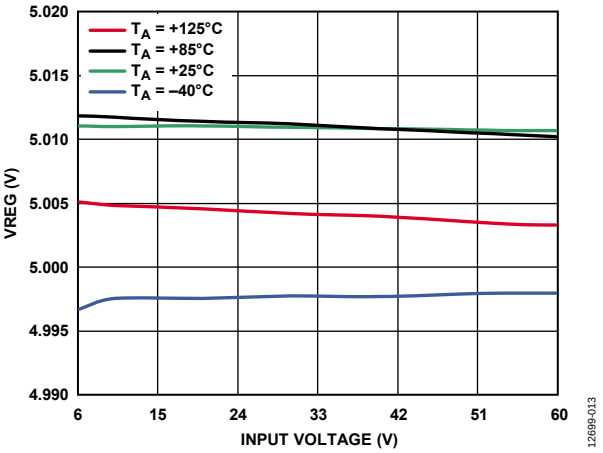

Figure 13. VREG vs. Input Voltage, No Load

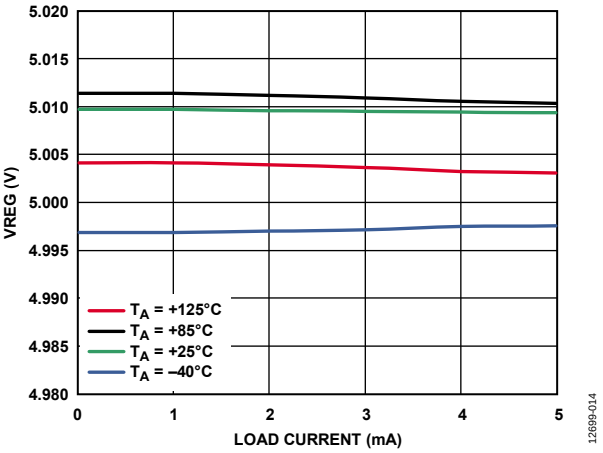

Figure 14. VREG vs. Load Current

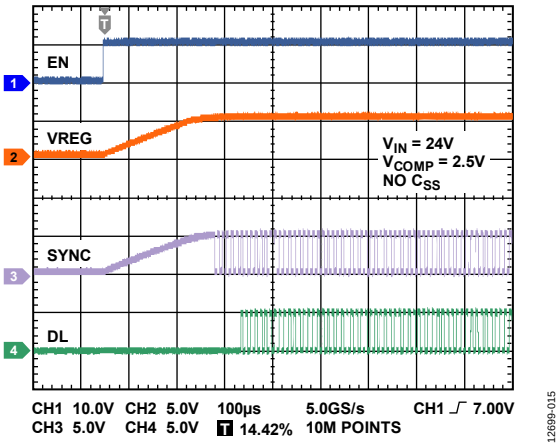

Figure 15. Startup

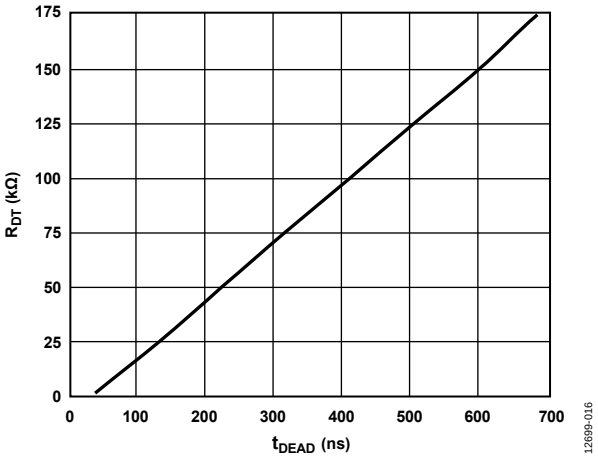

Figure 18. DT Pin Resistance (R_{DT}) vs. Dead Time (t_{DEAD})

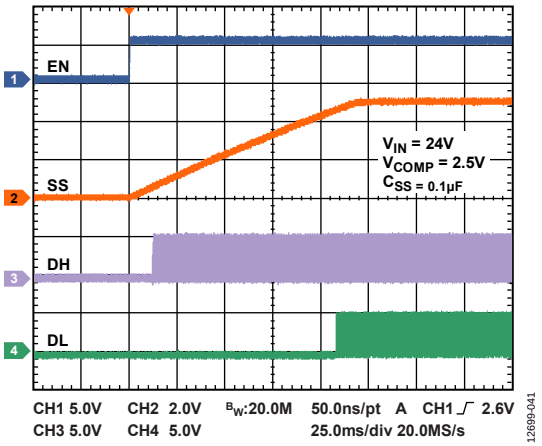

Figure 16. Buck Soft Start

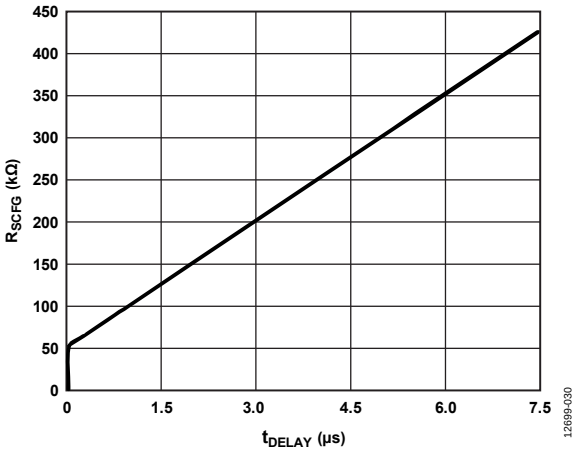

Figure 19. R_{SCFG} vs. Phase Time Delay (t_{DELAY})

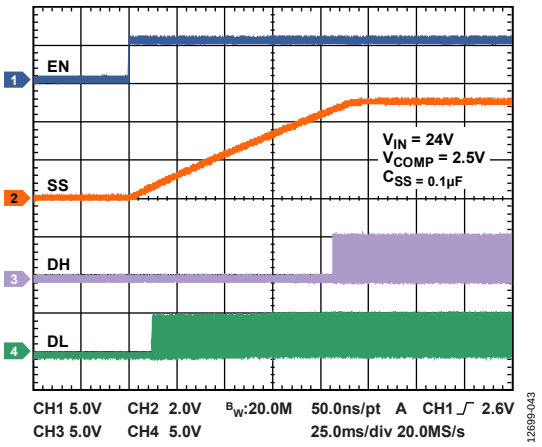

Figure 17. Boost Soft Start

THEORY OF OPERATION

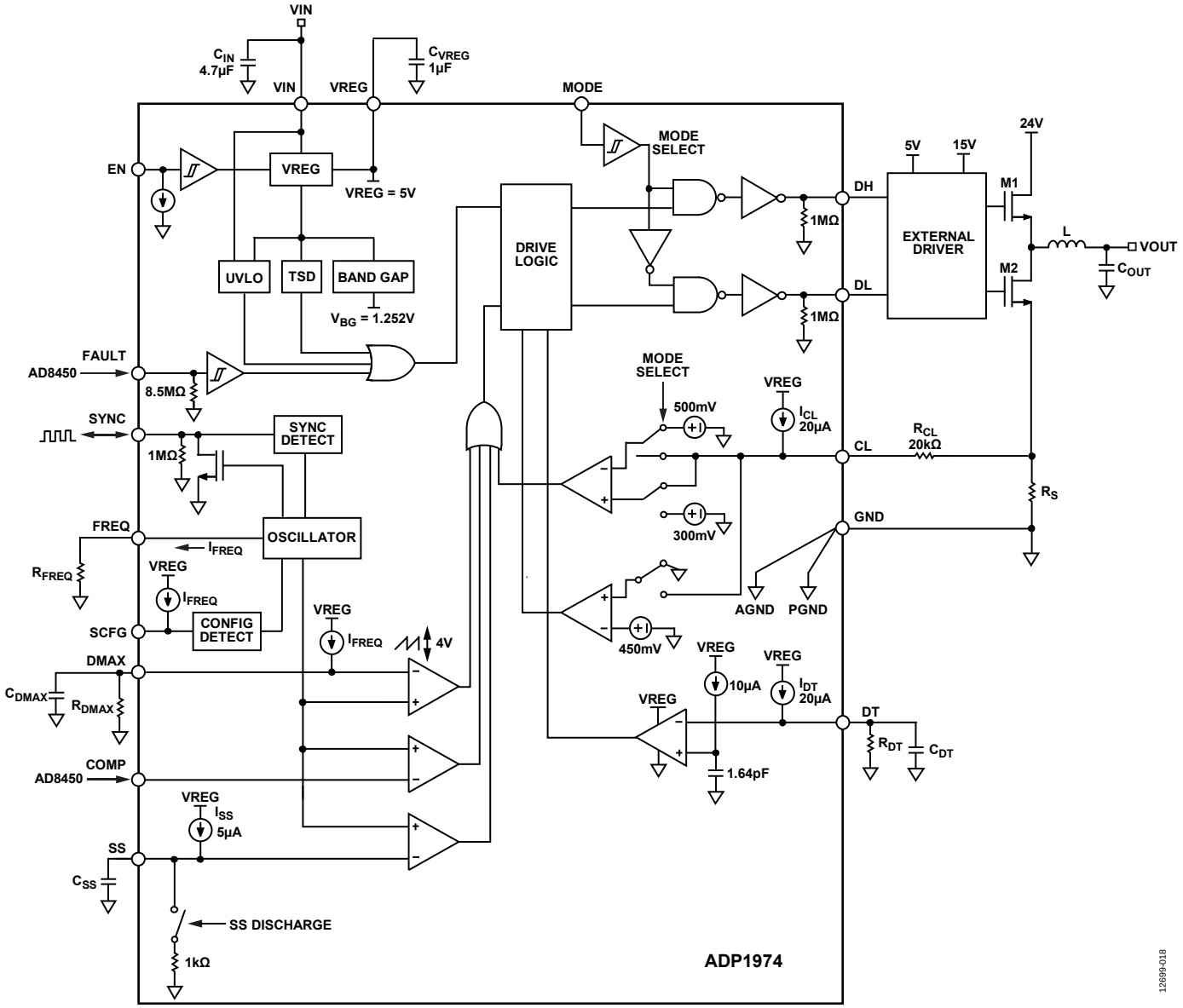

Figure 20. Internal Block Diagram

The ADP1974 is a constant frequency, voltage mode, synchronous, PWM controller for bidirectional dc-to-dc applications. The ADP1974 is designed to be used with an external, high voltage FET half bridge driver, such as the ADuM7223, and an external error amplifier AFE device, such as the AD8450/AD8451, to implement a battery testing, charging, and discharging system. The ADP1974 has a high input voltage range, multiple externally programmed control pins, and integrated safety features. In buck mode, the device charges a battery and delivers energy from the input power source to the output. In boost mode, the device discharges a battery and delivers energy from the battery to the input. In both modes, the ADP1974 operates as a synchronous controller for maximum efficiency.

SUPPLY PINS

The ADP1974 has two voltage supply pins, VIN and VREG. The VIN pin operates from an external supply that ranges from 6 V to 60 V and is the supply voltage for the internal linear regulator of the ADP1974. Bypass the VIN pin to ground with a 4.7 µF or greater ceramic capacitor.

The VREG pin is the output of the internal linear regulator. The internal regulator generates the 5 V (typical) rail that is used internally to bias the control circuitry and can be used externally as a pull-up voltage for the MODE, SYNC, DMAX, and FAULT pins. Bypass the VREG pin to ground with a 1 µF ceramic capacitor. VREG is disabled when EN is low and is active as long as VIN is above the internal UVLO (5.71 V typical) and EN is high.

When operating with an input voltage above 50 V, additional input filtering is recommended. Figure 21 shows the recommended filter configuration.

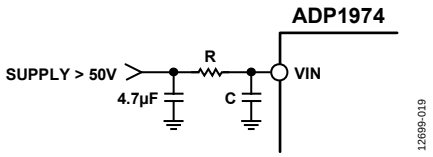

Figure 21. Recommended Filter Configuration for Input Voltages Greater than 50 V

EN/SHUTDOWN

The EN input turns the ADP1974 on or off and can operate from voltages up to 60 V. The EN pin is designed with precision enable control. When the EN voltage is less than 1.22 V (typical), the ADP1974 shuts down, VREG is disabled, and both DL and DH are driven low. When the ADP1974 shuts down, the VIN supply current is 15 µA (typical). When the EN voltage is greater than 1.25 V (typical), the ADP1974 is enabled, and VREG ramps to 5 V.

In addition to the EN pin, the device can be disabled via a fault condition indicated by an internal TSD event, a UVLO condition on VIN, or an external fault condition signaled via the FAULT pin. It is necessary to disable the device to change the operating mode from buck to boost.

UNDERVOLTAGE LOCKOUT (UVLO)

The UVLO function prevents the IC from turning on when the input voltage is below the specified operating range to avoid an undesired operating mode. When VIN rises, the UVLO does not allow the ADP1974 to turn on unless VIN is greater than 5.71 V (typical). The UVLO disables the device when VIN drops below 5.34 V (typical). The UVLO levels have ~370 mV of hysteresis to prevent the system from turning on and off repeatedly when there is a slow voltage ramp on the VIN pin.

SOFT START

The ADP1974 has a programmable soft start that prevents output voltage overshoot during startup. When the ADP1974 is enabled with the EN pin, the VREG voltage begins rising to 5 V. When VREG reaches 90% of its 5 V (typical) value, the 5 µA (typical) internal soft start current (I_{SS}) begins charging the soft start capacitor (C_{SS}), causing the voltage on the SS pin (V_{SS}) to rise.

While V_{SS} is less than 0.52 V (typical), the ADP1974 switching control remains disabled. When V_{SS} reaches 0.52 V (typical), switching is enabled. As C_{SS} continues to charge and V_{SS} rises, the PWM duty cycle gradually increases, allowing the output voltage to rise linearly. C_{SS} continues to charge, and V_{SS} rises to the internal VREG voltage (5 V typical). When the system duty cycle set by COMP is less than the soft start duty cycle, the external control loop takes control of the ADP1974. See Figure 22 for a soft start diagram.

When the device shuts down or a fault is detected, an active internal 1 kΩ pull-down resistor on the SS pin discharges C_{SS}.

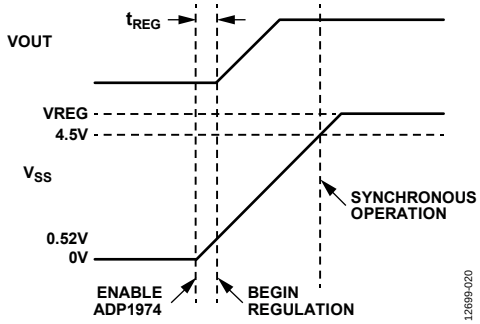

Figure 22. Soft Start Diagram

The MODE pin controls the ADP1974 duty cycle generator and affects the DL and DH signals during soft start. In buck mode, a DH pulse initiates the on time (or Phase 1). In boost mode, a DL pulse initiates the on time. For more information about buck vs. boost operation, see the Operating Modes section. During soft start, the ADP1974 operates in asynchronous mode, and the synchronous FET is not driven. During the off cycle, the diode in parallel to the low-side FET (buck mode) or the high-side FET (boost mode) conducts the current until it reaches zero or the next cycle begins. After the soft start period is completed (SS > 4.5 V), the ADP1974 switches to full synchronous mode.

OPERATING MODES

The ADP1974 operates as a synchronous buck or boost controller. When the MODE pin is driven high, above the 1.20 V (typical) threshold, the ADP1974 operates in a buck configuration for battery charging. If the MODE pin is driven low, below the 1.05 V (typical) threshold, the ADP1974 operates in a boost configuration. A boost configuration is ideal for discharging in battery formation applications. See Figure 23 and Figure 24 for the ADP1974 behavior in each mode. When the ADP1974 is enabled, the internal regulator connected to the VREG pin also powers up. On the rising edge of VREG, the state of the MODE pin is latched, preventing the mode of operation from being changed while the device is enabled. To change between boost and buck modes of operation, shut down or disable the ADP1974, adjust the MODE pin to change the operating mode, and restart the system.

The operating mode can be changed when the EN pin is driven low, the FAULT pin is driven low, or the ADP1974 is disabled via a TSD event or UVLO condition. On the rising edge of the FAULT control signal, the state of the MODE pin is latched, preventing the mode of operation from being changed while the device is enabled.

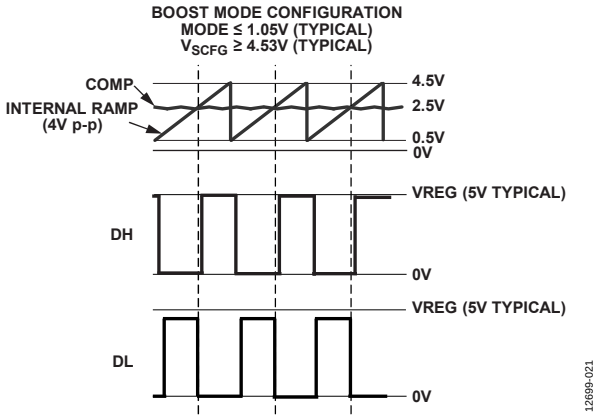

Figure 23. Drive Signal Diagram for Boost Configuration

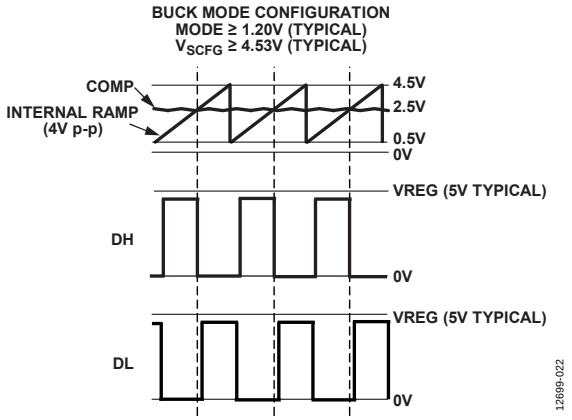

Figure 24. Drive Signal Diagram for Buck Configuration

PWM DRIVE SIGNALS

The ADP1974 has two 5 V logic level output drive signals, DH and DL that are compatible with drivers similar to the ADuM7223. The DH and DL drive signals synchronously turn on and off the high-side and low-side switches driven from the external driver. The ADP1974 provides resistor programmable dead time to prevent the DH and DL pins from transitioning at the same time, as shown in Figure 25. Connect a resistor to ground on the DT pin to program the dead time.

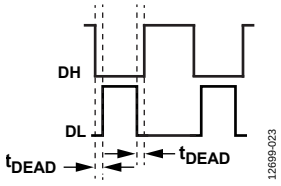

Figure 25. Dead Time (t_{DEAD}) Between DH and DL Transitions

When driving capacitive loads with the DH and DL pins, a 20 Ω resistor must be placed in series with the capacitive load to reduce ground noise and ensure signal integrity.

EXTERNAL COMP CONTROL

The ADP1974 COMP pin is the input to the PWM modulator comparator. The ADP1974 uses a voltage mode control that compares an error signal, applied to the COMP pin by an external error amplifier, such as the AD8450/AD8451, to an internal 4 V p-p triangle waveform. As the load changes, the error signal increases or decreases. The internal PWM comparator determines the appropriate duty cycle drive signal by monitoring the error signal at the COMP pin and the internal 4 V p-p ramp signal. The internal PWM comparator subsequently drives the external gate driver at the determined duty cycle through the DH and DL signals.

The functional voltage range of the COMP pin is from 0 V to 5.0 V. If V_{COMP} is between 0.5 V and 4.5 V, the ADP1974 regulates the DH and DL outputs accordingly. If V_{COMP} is greater than 4.5 V, the ADP1974 operates the DH and DL outputs at the maximum programmed duty cycle (or 97% whichever is the lowest). If V_{COMP} is less than 0.45 V, the ADP1974 operates the DH or DL output at a 0% duty cycle, according to the operating mode, while the complementary DL or DH output is driven at a 100% duty cycle. The input to the COMP pin must never exceed the 5.5 V absolute maximum rating.

The DL and DH signals swing from VREG (5 V typical) to ground. The external FET driver used must have input control pins compatible with a 5 V logic signal.

PEAK CURRENT-LIMIT HICCUP IMPLEMENTATION

The ADP1974 features a peak hiccup current-limit implementation measured on the low-side FET across a sense resistor. When the peak inductor current exceeds the programmed current limit for more than 500 consecutive clock cycles, 5.2 ms (typical) for a 100 kHz programmed frequency, the peak hiccup current-limit condition occurs. If the overcurrent exist for less than 500 consecutive cycles, the counter is reset to zero. When the overcurrent condition occurs, the SS pin is discharged through a 1 kΩ resistor, and the drive signals, DL and DH, are disabled for the next 500 clock cycles to allow the FETs to cool down (hiccup mode). When the 500 clock cycles expire, the ADP1974 restarts through a new soft start cycle.

Figure 26 shows the current-limit block diagram for peak current-limit protection.

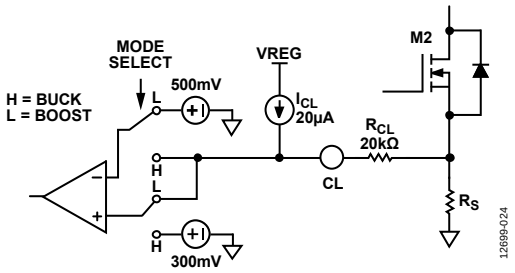

Figure 26. Current-Limit Block Diagram for Peak Current-Limit Protection

The current-limit threshold is set internally based on the mode selected. It is designed to trigger when the voltage on R_S reaches 100 mV in either buck or boost mode when using R_{CL} = 20 kΩ with 400 mV across it due to the 20 µA current source. More information on how to set the current limit is available in the Applications Information section.

NEGATIVE CURRENT-LIMIT DETECTION (BUCK MODE)

The ADP1974 detects negative current in the inductor in buck mode with a comparator on the CL pin set to 450 mV, as shown in Figure 27. When the current in the low-side FET drops below the limit (negative 50 mV on R_S), the DL driver immediately disables, which is used as a negative current limit in buck mode, detecting the equivalent of ½ the positive peak current.

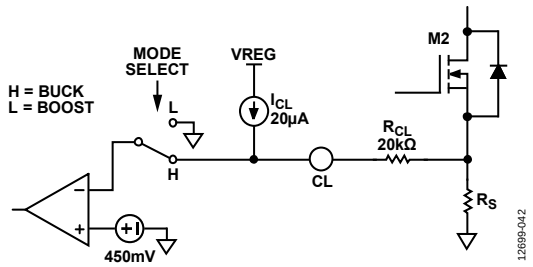

Figure 27. Block Diagram for Negative Current-Limit Protection

PWM FREQUENCY CONTROL

The FREQ, SYNC, and SCFG pins determine the source, frequency, and synchronization of the clock signal that operates the PWM control of the ADP1974.

Internal Frequency Control

The ADP1974 frequency can be programmed with an external resistor connected between FREQ and ground. The frequency range can be set from a minimum of 50 kHz to a maximum of 300 kHz. If the SCFG pin is tied to VREG, forcing $V_{SCFG} \geq 4.53$ V (typical), or if the SCFG pin is left floating, the SYNC pin is configured as an output, and the ADP1974 operates at the frequency set by R_{FREQ}, which outputs from the SYNC pin through the open-drain device. The output clock of the SYNC pin operates with a 50% (typical) duty cycle. In this configuration, the SYNC pin can synchronize other switching regulators in the system to the ADP1974. When the SYNC pin is configured as an output, an external pull-up resistor is needed from the SYNC pin to an external supply. The VREG pin of the ADP1974 can be used as the external supply rail for the pull-up resistor.

External Frequency Control

When $V_{SCFG} \leq 0.5$ V (typical), the SYNC pin is configured as an input, the ADP1974 synchronizes to the external clock applied to the SYNC pin, and the ADP1974 operates as a slave device. This synchronization allows the ADP1974 to operate at the same switching frequency with the same phase as other switching regulators or devices in the system. When operating the ADP1974 with an external clock, select R_{FREQ} to provide a frequency that approximates but is not equal to the external clock frequency, which is further explained in the Applications Information section.

Operating Frequency Phase Shift

When the voltage applied to the SCFG pin is 0.65 V < V_{SCFG} < 4.25 V, the SYNC pin is configured as an input, and the ADP1974 synchronizes to a phase shifted version of the external clock applied to the SYNC pin. To adjust the phase shift, place a resistor (R_{SCFG}) from SCFG to ground. The phase shift reduces the input supply ripple for systems containing multiple switching power supplies.

MAXIMUM DUTY CYCLE

The maximum duty cycle of the ADP1974 can be externally programmed to any value between 0% and 97% via an external resistor on the DMAX pin connected from DMAX to ground. The maximum duty cycle defaults to 97% if DMAX is left floating, if DMAX is tied to VREG, or if DMAX is programmed to a value greater than 97%.

EXTERNAL FAULT SIGNALING

The ADP1974 is equipped with a FAULT pin that signals the ADP1974 when an external fault condition occurs. The external fault signal stops PWM operation of the system to avoid damage to the application and components. When a voltage less than 1.05 V (typical) is applied to the FAULT pin, the ADP1974 is disabled. In this state, the DL and DH PWM drive signals are both driven low to prevent switching, and the soft start capacitor (C_{SS}) is discharged with a 1 kΩ resistance. When a voltage greater than 1.2 V (typical) is applied to the FAULT pin, the ADP1974 begins switching. A voltage ranging from 0 V to 60 V can be applied to the FAULT pin of the ADP1974.

THERMAL SHUTDOWN (TSD)

The ADP1974 has a TSD protection circuit. The thermal shutdown triggers and disables switching when the junction temperature of the ADP1974 reaches 150°C (typical). While in TSD, the DL and DH signals are driven low, the C_{SS} capacitor discharges to ground, and VREG remains high. When the junction temperature decreases to 135°C (typical), the ADP1974 restarts the application control loop.

APPLICATIONS INFORMATION

The ADP1974 has many programmable features that are optimized and controlled for a given application. The ADP1974 provides pins for selecting the operating mode, controlling the current limit, selecting an internal or external clock, setting the operating frequency, phase shifting the operating frequency, programming the dead time, programming the maximum duty cycle, and adjusting the soft start.

BUCK OR BOOST SELECTION

To operate the ADP1974 in boost (recycle) mode, apply a voltage less than 1.05 V (typical) to the MODE pin. To operate the ADP1974 in buck (discharge) mode, drive the MODE pin high, greater than 1.20 V (typical). The state of the MODE pin can change only when the ADP1974 is shut down via the EN pin, or is disabled via an external fault condition signaled on the FAULT pin, there is a TSD event, or there is a UVLO condition.

SELECTING R_S TO SET THE CURRENT LIMIT

See Figure 26 for the current-limit block diagram for peak current-limit control. To set the current limit, use the following equation:

$$I_{PK}\,(\text{mA}) = 100\ \text{mV}/R_S \quad (2)$$

where:
I_{PK} is the desired peak current limit in mA.
R_S is the sense resistor used to set the peak current limit in Ω.

When the ADP1974 is configured to operate in buck (charge) mode, the internal current-limit threshold is set to 300 mV (typical) and the negative valley current-limit threshold is set to 450 mV (typical). When the ADP1974 is configured to operate in boost (recycle) mode, the internal current-limit threshold is set to 500 mV (typical). The external resistor (R_{CL}) offsets the current properly to detect the peak in both buck and boost operation. Set the R_{CL} value to 20 kΩ. In operation, the equations for setting the peak currents follow.

For buck (charge) mode, use the following:

$$V_{CL\,(BUCK)} = (I_{CL}) \times (R_{CL}) - (I_{PK}) \times (R_S) \quad (3)$$
$$V_{NC\,(BUCK)} = (I_{CL}) \times (R_{CL}) + (I_{VL\,(NEG)}) \times (R_S) \quad (4)$$

For boost (recycle) mode, use the following:

$$V_{CL\,(BOOST)} = (I_{CL}) \times (R_{CL}) + (I_{PK}) \times (R_S) \quad (5)$$

where:
$V_{CL\,(BUCK)}$ = 300 mV typical.
I_{CL} = 20 µA typical.
R_{CL} = 20 kΩ.
I_{PK} is the peak inductor current.
$V_{NC\,(BUCK)}$ = 450 mV typical.
$I_{VL\,(NEG)}$ is the valley inductor current.
$V_{CL\,(BOOST)}$ = 500 mV typical.

The ADP1974 is designed so that the peak current limit is the same in both the buck mode and the boost mode of operation. A 1% or better tolerance for the R_{CL} and R_S resistors is recommended.

ADJUSTING THE OPERATING FREQUENCY

If the SCFG pin is tied to VREG, forcing $V_{SCFG} \geq 4.53$ V, or if SCFG is left floating and internally tied to VREG, the ADP1974 operates at the frequency set by R_{FREQ}, and the SYNC pin outputs a clock at the programmed frequency. When $V_{SCFG} \geq 4.53$ V, the output clock on the SYNC pin can be used as a master clock in applications that require synchronization.

If $V_{SCFG} \leq 0.5$ V, the SYNC pin is configured as an input, and the ADP1974 operates as a slave device. As a slave device, the ADP1974 synchronizes to the external clock applied to the SYNC pin. If the voltage applied to the SCFG pin is 0.65 V < V_{SCFG} < 4.25 V, and a resistor is connected between SCFG and ground, the SYNC pin is configured as an input, and the ADP1974 synchronizes to a phase shifted version of the external clock applied to the SYNC pin.

Whether operating the ADP1974 as a master or as a slave device, carefully select R_{FREQ} using the equations in the following sections.

Selecting R_{FREQ} for a Master Device

When V_{SCFG} is ≥ 4.53 V, the ADP1974 operates as a master device. When functioning as a master device, the ADP1974 operates at the frequency set by the external R_{FREQ} resistor connected between FREQ and ground, and the ADP1974 outputs a clock at the programmed frequency on the SYNC pin.

Figure 28 shows the relationship between the $R_{FREQ\,(MASTER)}$ value and the programmed switching frequency.

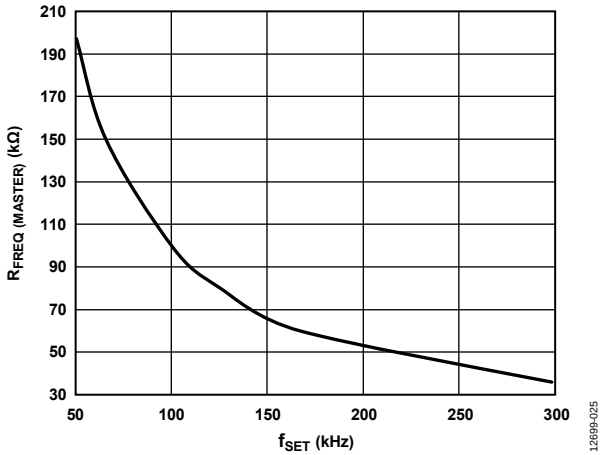

Figure 28. $R_{FREQ\,(MASTER)}$ vs. Switching Frequency (f_{SET})

To calculate the $R_{FREQ\,(MASTER)}$ value for a desired master clock synchronization frequency, use the following equation:

$$R_{FREQ\,(MASTER)}(\text{k}\Omega) = \frac{10^4}{f_{SET}(\text{kHz})} \quad (5)$$

where:
$R_{FREQ\,(MASTER)}$ is the resistor in kΩ to set the frequency for master devices.
f_{SET} is the switching frequency in kHz.

Selecting R_{FREQ} for a Slave Device

To configure the ADP1974 as a slave device, drive $V_{SCFG} < 4.53$ V. When functioning as a slave device, the ADP1974 operates at the frequency of the external clock applied to the SYNC pin. To ensure proper synchronization, select R_{FREQ} to set the frequency to a value slightly slower than that of the master clock by using the following equation:

$$R_{FREQ\ (SLAVE)} = 1.11 \times R_{FREQ\ (MASTER)} \quad (6)$$

where:
$R_{FREQ\ (SLAVE)}$ is the resistor value that appropriately scales the frequency for the slave device, and 1.11 is the R_{FREQ} slave to master ratio for synchronization.
$R_{FREQ\ (MASTER)}$ is the resistor value that corresponds to the frequency of the master clock applied to the SYNC pin.

The frequency of the slave device is set to a frequency slightly lower than that of the master device to allow the digital synchronization loop of the ADP1974 to synchronize to the master clock period. The slave device can synchronize to a master clock frequency running between 2% to 20% higher than the slave clock frequency. Setting $R_{FREQ\ (SLAVE)}$ to 1.11× larger than $R_{FREQ\ (MASTER)}$ runs the synchronization loop in approximately the center of the adjustment range.

Programming the External Clock Phase Shift

If a phase shift is not required for slave devices, connect the SCFG pin of each slave device to ground. For devices that require a phase shifted version of the synchronization clock that is applied to the SYNC pin of the slave devices, connect a resistor (R_{SCFG}) from SCFG to ground to program the desired phase shift. To determine the R_{SCFG} for a desired phase shift (φ_{SHIFT}), start by calculating the frequency of the slave clock (f_{SLAVE}).

$$f_{SLAVE}(\text{kHz}) = \frac{10^4}{R_{FREQ\ (SLAVE)}} \quad (7)$$

Next, calculate the period of the slave clock.

$$t_{SLAVE}(\mu\text{s}) = \frac{1}{f_{SLAVE}(\text{kHz})} \times 10^3 \quad (8)$$

where:
t_{SLAVE} is the period of the slave clock in µs.
f_{SLAVE} is the frequency of the slave clock in kHz.

Next, determine the phase time delay (t_{DELAY}) for the desired phase shift (φ_{SHIFT}) using the following equation:

$$t_{DELAY}(\mu\text{s}) = \frac{\varphi_{SHIFT} \times t_{SLAVE}\ (\mu\text{s})}{360} \quad (9)$$

where:
t_{DELAY} is the phase time delay in µs.
φ_{SHIFT} is the desired phase shift.

Lastly, use the following equation to calculate t_{DELAY}:

$$R_{SCFG}\ (\text{k}\Omega) = 0.45 \times R_{FREQ\ (SLAVE)}\ (\text{k}\Omega) + 50 \times t_{DELAY}\ (\mu\text{s}) \quad (10)$$

where:
R_{SCFG} is the corresponding resistor for the desired phase shift in kHz. See Figure 19 for the R_{SCFG} vs. t_{DELAY} graph.

When using the phase shift feature, connect a capacitor of 47 pF or greater in parallel with R_{SCFG}.

Alternatively, the SCFG pin can be controlled with a voltage source. When using an independent voltage source, ensure $V_{SCFG} \leq$ VREG under all conditions. When the ADP1974 is disabled via the EN pin or UVLO, VREG = 0 V, and the voltage source must be adjusted accordingly to ensure $V_{SCFG} \leq$ VREG.

Figure 29 shows the internal voltage ramp of the ADP1974. The voltage ramp is a well controlled 4 V p-p.

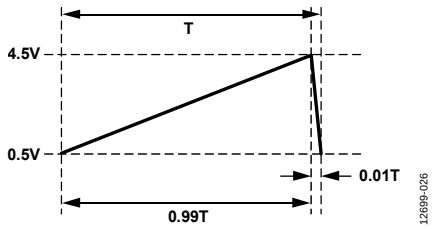

Figure 29. Internal Voltage Ramp

Programming the Dead Time

To adjust the dead time on the synchronous DH and DL outputs, connect a resistor (R_{DT}) from DT to GND and bypass with a 47 pF capacitor. Select R_{DT} for a given dead time using Figure 30 or calculate R_{DT} using the following equations. To reach a single equation for R_{DT}, combine the equations for V_{DT} and R_{DT}.

$$V_{DT}(\text{V}) = \frac{I_{DT} \times \left(t_{DEAD}(\text{ns}) - 28.51\right)}{3.76} \quad (11)$$

$$R_{DT} = \frac{V_{DT}}{I_{DT}} \quad (12)$$

where:
V_{DT} is the DT pin programming voltage.
I_{DT} is the 20 µA (typical) internal current source.
t_{DEAD} is the desired dead time in ns.
R_{DT} is the resistor value in kΩ for the desired dead time.

To calculate R_{DT} for a given t_{DEAD}, the resulting equation used is

$$R_{DT}(\text{k}\Omega) = \frac{t_{DEAD}(\text{ns}) - 28.51}{3.76} \quad (13)$$

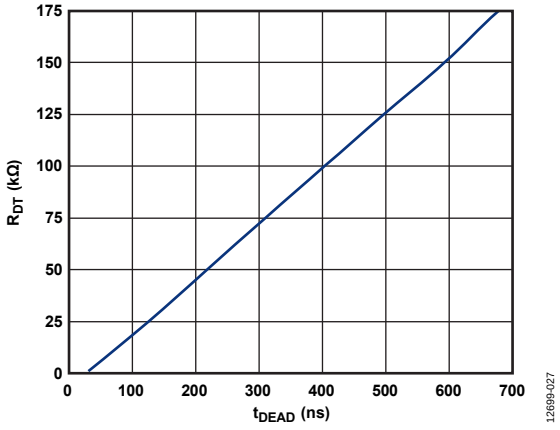

Figure 30. DT Pin Resistance (R_{DT}) vs. Dead Time (t_{DEAD})

PROGRAMMING THE MAXIMUM DUTY CYCLE

The ADP1974 is designed with a 97% (typical) maximum internal duty cycle. By connecting a resistor from DMAX to ground, the maximum duty cycle can be programmed at any value from 0% to 97%, by using the following equation:

$$D_{MAX}(\%) = \frac{21.5 \times V_{FREQ} \times R_{DMAX}}{R_{FREQ}} - 10.5 \quad (14)$$

where:
D_{MAX} is the programmed maximum duty cycle.
V_{FREQ} = 1.252 V (typical).
R_{DMAX} is the value of the resistance used to program the maximum duty cycle.
R_{FREQ} is the frequency set resistor used in the application.

The DMAX current source is equivalent to the programmed current of the FREQ pin:

$$I_{DMAX} = I_{FREQ} = \frac{V_{FREQ}}{R_{FREQ}} \quad (15)$$

where $I_{DMAX} = I_{FREQ}$ is the current programmed on the FREQ pin.

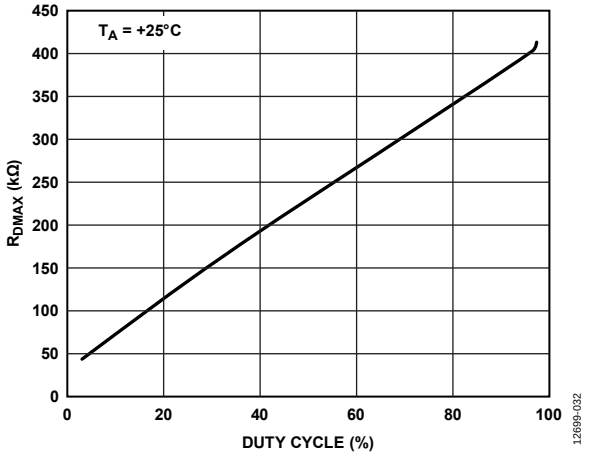

Figure 31. R_{DMAX} vs. Duty Cycle, R_{FREQ} = 100 kΩ, V_{COMP} = 5 V

The maximum duty cycle of the ADP1974 is 97% (typical). If the resistor on DMAX sets a maximum duty cycle larger than 97%, the ADP1974 defaults to its internal maximum. If the 97% internal maximum duty cycle is sufficient for the application, tie the DMAX pin to VREG or leave it floating.

The C_{DMAX} capacitor connected from the DMAX pin to the ground plane must be 47 pF or greater.

ADJUSTING THE SOFT START PERIOD

The ADP1974 has a programmable soft start feature that prevents output voltage overshoot during startup. Refer to Figure 22 for a soft start diagram. To calculate the delay time before switching is enabled (t_{REG}), use the following equation:

$$t_{REG} = \frac{0.52}{I_{SS}} \times C_{SS} \quad (16)$$

where:
I_{SS} = 5 µA, typical.
C_{SS} is the soft start capacitor value.

The output voltage rising ramp is then proportional to the ramp on SS and the input voltage of the ADP1974.

$$t_{RAMP} = \frac{4}{I_{SS}} \times C_{SS}$$

$$RAMP\_RATE = \frac{V_{OUT}}{Time(\text{s})} = \frac{V_{IN}}{t_{RAMP}} (\text{V/s})$$

As an example, a design with a 20 V input and a 10 nF capacitor creates a delay of 1 ms and a 2.5 V/ms ramp rate.

A C_{SS} capacitor is not required for the ADP1974. When the C_{SS} capacitor is not used, the internal 5 µA (typical) current source immediately pulls the SS pin voltage to VREG. When a C_{SS} capacitor is not used, there is no soft start control internal to the ADP1974, and the system can produce a large output overshoot, and a large peak inductor spike during startup. When a C_{SS} capacitor is not used, ensure that the output overshoot is not large enough to trip the hiccup current limit during startup.

PCB LAYOUT GUIDELINES

For high efficiency, good regulation, and stability, a well designed PCB layout is required.

Use the following guidelines when designing the PCB (see Figure 20 for the block diagram and Figure 2 for the pin configuration):

- Keep the low effective series resistance (ESR) input supply capacitor (C_{IN}) for VIN as close as possible to the VIN and GND pins to minimize noise injected into the device from board parasitic inductance.
- Keep the low ESR input supply capacitor (C_{VREG}) for VREG as close as possible to the VREG and GND pins to minimize the noise injected into the device from board parasitic inductance.
- Place the components for the SCFG, FREQ, DMAX, and SS pins close to the corresponding pins. Tie these components collectively to an analog ground plane that makes a Kelvin connection to the GND pin.
- Keep the trace from the COMP pin to the accompanying device (for example, the AD8450) as short as possible. Avoid routing this trace near switching signals, and shield the trace, if possible.
- Place any trace or components for the SYNC pin away from sensitive analog nodes. When using an external pull-up resistor, it is best to use a local 0.1 µF bypass capacitor from the supply of the pull-up resistor to GND.
- Keep the traces from the DH and DL pins to the external components as short as possible to minimize parasitic inductance and capacitance, which affect the control signal. The DH and DL pins are switching nodes; do not route them near any sensitive analog circuitry.
- Keep high current traces as short and as wide as possible.
- Connect the ground connection of the ADP1974 directly to the ground connection of the current sense resistor (R_S).
- Connect CL through a 20 kΩ resistor directly to R_S.
- From the ground connection shown in Figure 32, connect the following:
  - The GND pin to the ground point for RS
  - The system power ground bus to the ground point of RS
- When building a system with a master and multiple slave devices, minimize the capacitance of the trace attached to the SYNC pin by considering the following items:
  - For small systems with only a few slave devices, a resistor connected in series between the master SYNC signal and the slave SYNC input pins limits the capacitance of the trace and reduces the fast ground currents that can inject noise into the master device.
  - For larger applications, the series resistance is not enough to isolate the master SYNC clock. In larger systems, use an external buffer to reduce the capacitance of the trace. The external buffer has the drive capability to support a large number of slave devices.

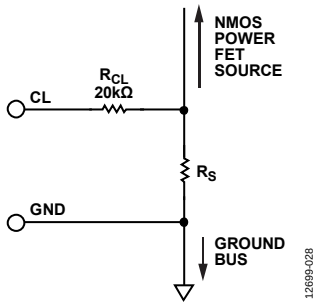

Figure 32. Recommended R_S Kelvin Ground Connection

OUTLINE DIMENSIONS

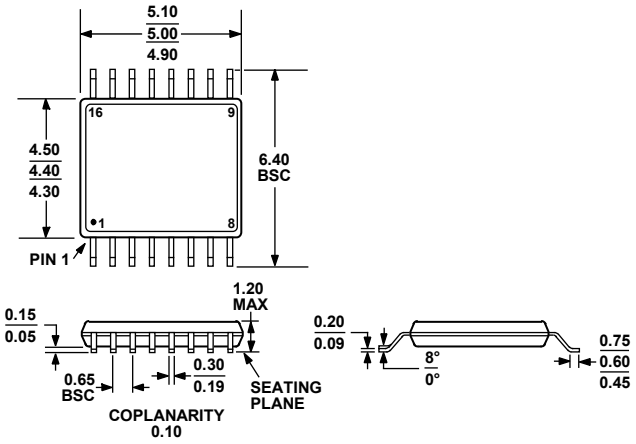

Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADP1974ARUZ-R7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP], 7″ Tape and Reel	RU-16	1000
ADP1974ARUZ-RL	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP], 13″ Tape and Reel	RU-16	2500
ADP1974-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.