10A Step-Down DC/DC µModule Regulator

FEATURES

- **10A DC Output Current**
- **Input Voltage Range: 4.5V to 16V**
- **Output Voltage Range: 0.6V Up to 3.3V**
- **No Heat Sink or Current Derating Up to 85°C Ambient Temperature**
- **±1.5% Total DC Voltage Output Error**
- **Multiphase Operation with Current Sharing**
- **Remote Sense Amplifier**
- Built-In General Purpose Temperature Monitor
- Selectable Pulse-Skipping Mode/Burst Mode® Operation for High Efficiency at Light Load
- Soft-Start/Voltage Tracking
- Protection: Output Overvoltage and Overcurrent Foldback
- 9mm × 15mm × 4.92mm BGA Package

APPLICATIONS

- Telecom, Networking and Industrial Equipment
- Point of Load Regulation

DESCRIPTION

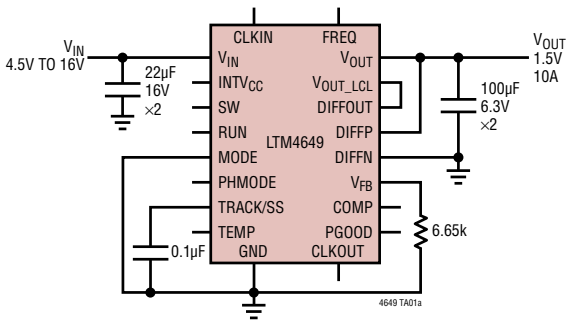
The LTM®4649 is a complete 10A high efficiency switching mode step-down DC/DC µModule® regulator in a 9mm × 15mm × 4.92 BGA package. Included in the package are the switching controller, power FETs, inductor, and all support components. Operating over an input voltage range of 4.5V to 16V, the LTM4649 supports an output voltage range of 0.6V to 3.3V, set by a single external resistor. This high efficiency design delivers 10A continuous current. Only bulk input and output capacitors are needed.

High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The device supports frequency synchronization, programmable multiphase operation, and output voltage tracking for supply rail sequencing.

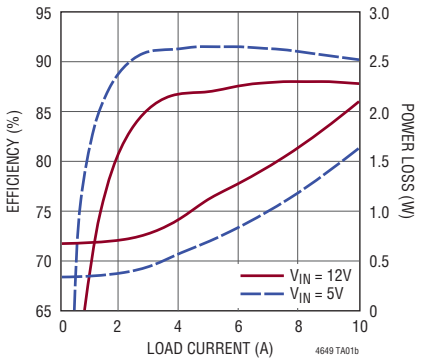
Fault protection features include output overvoltage and overcurrent protection. The LTM4649 is offered in a small 9mm × 15mm × 4.92mm BGA package available with SnPb or RoHS compliant terminal finish.

TYPICAL APPLICATION

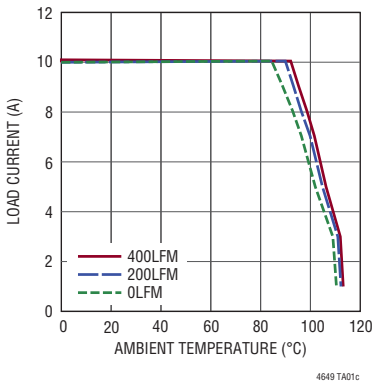
4.5V to 16V Input, 1.5V Output DC/DC µModule Regulator



Efficiency and Power Loss at 12V and 5V Input



Current Derating: 12V Input, 1.5V_{OUT}, No Heat Sink

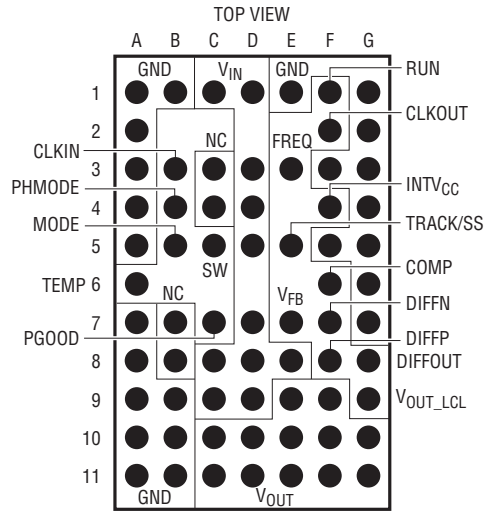


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 18V
V_{OUT} ..... –0.3V to 3.6V
$INTV_{CC}$, PGOOD, RUN ..... –0.3V to 6V
MODE, CLKIN, TRACK/SS, DIFFP, DIFFN,
DIFFOUT, PHMODE ..... –0.3V to $INTV_{CC}$
V_{FB} ..... –0.3V to 2.7V
COMP (Note 3) ..... –0.3V to 2.7V
$INTV_{CC}$ Peak Output Current 100mA
Internal Operating Temperature Range
(Note 2) ..... –55°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Package Body Temperature ... 245°C

PIN CONFIGURATION



BGA PACKAGE
68-LEAD (9mm × 15mm × 4.92mm)

T_{JMAX} = 125°C, θ_{JA} = 14°C/W, $\theta_{JCbottom}$ = 5°C/W, θ_{JCtop} = 20°C/W
$\theta_{JB} + \theta_{BA}$ = 14°C/W, WEIGHT = 1.7g

ORDER INFORMATION

http://www.linear.com/product/LTM4649#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4649EY#PBF	SAC305 (RoHS)	LTM4649Y	e1	BGA	3	–40°C to 125°C
LTM4649IY#PBF	SAC305 (RoHS)	LTM4649Y	e1	BGA	3	–40°C to 125°C
LTM4649IY	SnPb (63/37)	LTM4649Y	e0	BGA	3	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V per typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	4.5		16	V
$V_{OUT(RANGE)}$	Output Voltage Range		●	0.6		3.3	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF × 1,C_{OUT} = 100µF Ceramic, 100µF POSCAP, R_{FB} = 6.65k, MODE = GND, V_{IN} = 4.5V to 16V, I_{OUT} = 0A to 10A	●	1.477	1.50	1.523	V
Input Specifications							
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising		1.1	1.25	1.4	V
$V_{RUN(HYS)}$	RUN Pin On Hysteresis				150		mV
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, Burst Mode Operation V_{IN} = 12V, V_{OUT} = 1.5V, Pulse-Skipping Mode V_{IN} = 12V, V_{OUT} = 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			5 15 75 70		mA mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A			1.5		A
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)		0		10	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 4.5V to 16V I_{OUT} = 0A	●		0.010	0.04	%/V
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 10A, V_{IN} = 12V (Note 4)	●		0.15	0.5	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, 100µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V			15		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF Ceramic, 100µF POSCAP, V_{OUT} = 1.5V, I_{OUT} = 0A, V_{IN} = 12V			20		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic, 100µF POSCAP, No Load, TRACK/SS = 0.01µF, V_{IN} = 12V			5		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic, 100µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V			60		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic, 100µF POSCAP, V_{IN} = 12V, V_{OUT}=1.5V			20		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)		12			A
Control Specifications							
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.593	0.60	0.607	V
I_{FB}	Current at V_{FB} Pin	(Note 3)			–12	–25	nA
V_{OVL}	Feedback Overvoltage Lockout		●	0.64	0.66	0.68	V
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V		1.0	1.2	1.4	µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 3)			90		ns
R_{FBHI}	Resistor Between V_{OUT_LCL} and V_{FB} Pins			9.90	10	10.10	kΩ
DIFFP, DIFFN CM RANGE	Common Mode Input Range	V_{IN} = 12V, Run > 1.4V		0		3.6	V
$V_{DIFFOUT(MAX)}$	Maximum DIFFOUT Voltage	$I_{DIFFOUT}$ = 300µA		$INTV_{CC}$-1.4			V
V_{OS}	Input Offset Voltage	V_{DIFFP} = $V_{DIFFOUT}$ = 1.5V, $I_{DIFFOUT}$ = 100µA				4	mV
A_V	Differential Gain	(Note 3)			1		V/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V per typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	(Note 5)			2		V/µs
GBP	Gain Bandwidth Product	(Note 5)			3		MHz
CMRR	Common Mode Rejection	(Note 3)			60		dB
$I_{DIFFOUT}$	DIFFOUT Current	Sourcing		2			mA
R_{IN}	Input Resistance	DIFFP, DIFFN to GND			80		kΩ
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive			 –10 10		 % %
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage			4.8	5	5.2	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.9		%
Oscillator and Phase-Locked Loop							
f_{SYNC}	Frequency Sync Capture Range			250		800	kHz
f_S	Nominal Switching Frequency			400	450	500	kHz
R_{MODE}	MODE Input Resistance				250		kΩ
V_{IH_CLKIN}	Clock Input Level High			2.0			V
V_{IL_CLKIN}	Clock Input Level Low					0.8	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Notes are automatically numbered when you apply the note style.

Note 2: The LTM4649 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4649E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4649I is guaranteed to meet specifications over the –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

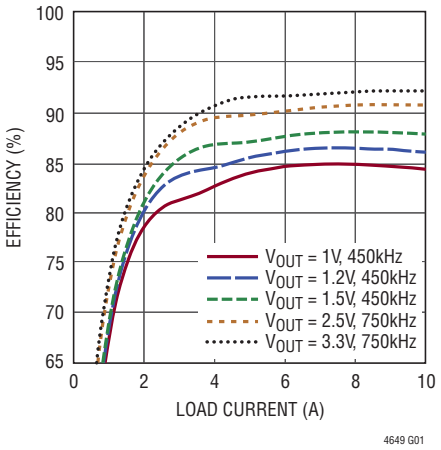
Note 3: 100% tested at wafer level.

Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

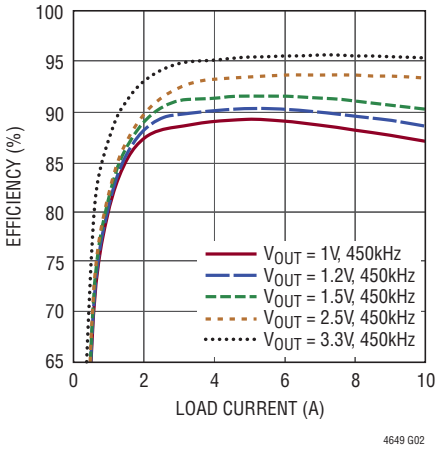
Note 5: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

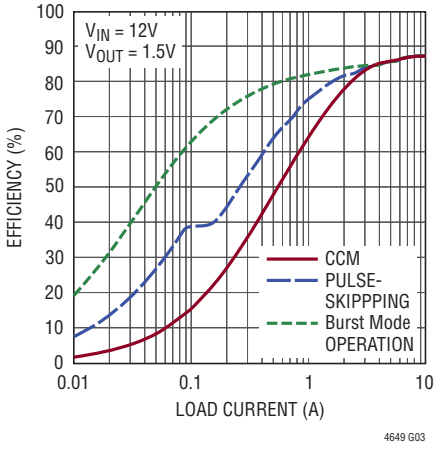
$12V_{IN}$ Efficiency



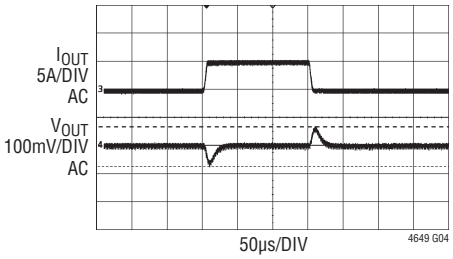
$5V_{IN}$ Efficiency



CCM, Burst Mode and Pulse-Skipping Mode Efficiency

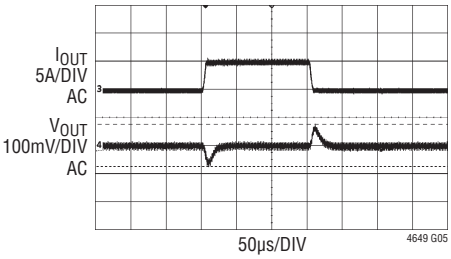


$5V_{IN}$, $1V_{OUT}$ Load Transient



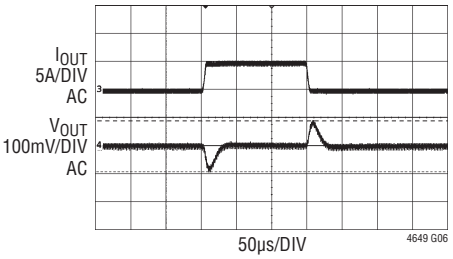
$5V_{IN}$, $1V_{OUT}$, 5A TO 10A LOAD STEP
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR
NO C_{FF} CAPACITOR

$12V_{IN}$, $1V_{OUT}$ Load Transient



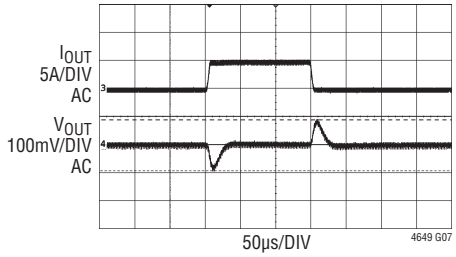
$12V_{IN}$, $1V_{OUT}$, 5A TO 10A LOAD STEP
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR
NO C_{FF} CAPACITOR

$5V_{IN}$, $1.5V_{OUT}$ Load Transient



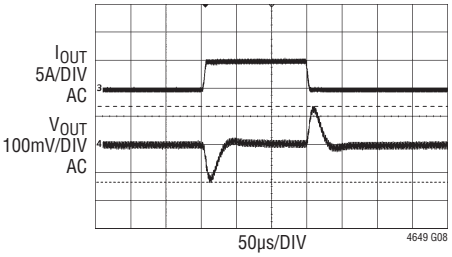
$5V_{IN}$, $1.5V_{OUT}$, 5A TO 10A LOAD STEP
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR
NO C_{FF} CAPACITOR

$12V_{IN}$, $1.5V_{OUT}$ Load Transient



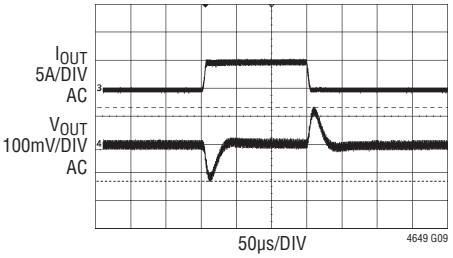
$12V_{IN}$, $1.5V_{OUT}$, 5A TO 10A LOAD STEP
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR
NO C_{FF} CAPACITOR

$5V_{IN}$, $2.5V_{OUT}$ Load Transient



$5V_{IN}$, $2.5V_{OUT}$, 5A TO 10A LOAD STEP
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR
NO C_{FF} CAPACITOR

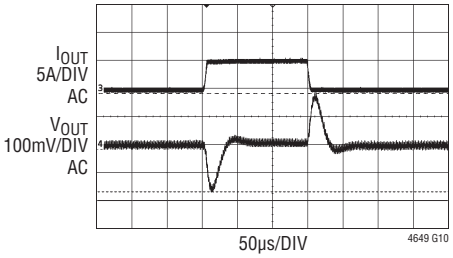
$12V_{IN}$, $2.5V_{OUT}$ Load Transient



$12V_{IN}$, $2.5V_{OUT}$, 5A TO 10A LOAD STEP, 750kHz
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR
NO C_{FF} CAPACITOR

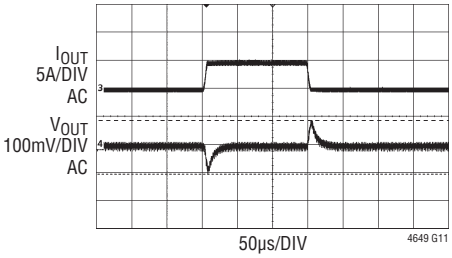
TYPICAL PERFORMANCE CHARACTERISTICS

$5V_{IN}$, $3.3V_{OUT}$ Load Transient



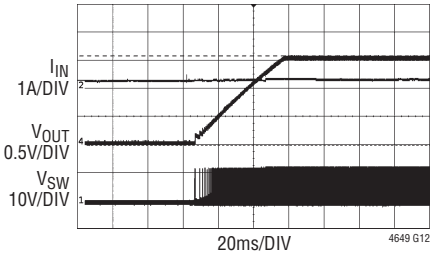
$5V_{IN}$, $3.3V_{OUT}$, 5A TO 10A LOAD STEP
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR
NO C_{FF} CAPACITOR

$12V_{IN}$, $3.3V_{OUT}$ Load Transient



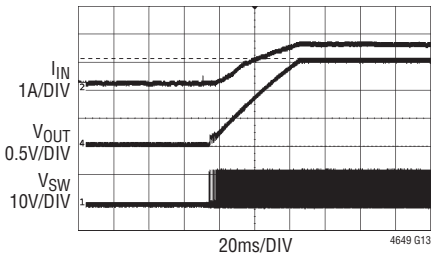
$12V_{IN}$, $3.3V_{OUT}$, 5A TO 10A LOAD STEP, 750kHz
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR
NO C_{FF} CAPACITOR

Soft-Start with No Load



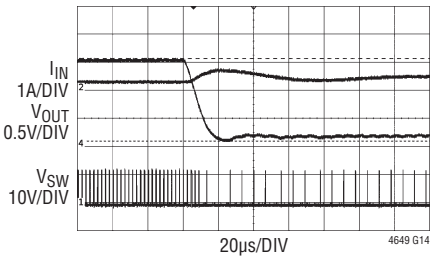
$12V_{IN}$, $1.5V_{OUT}$
I_O = 0A START-UP
C_{SS} = 0.1µF

Soft-Start with Full Load



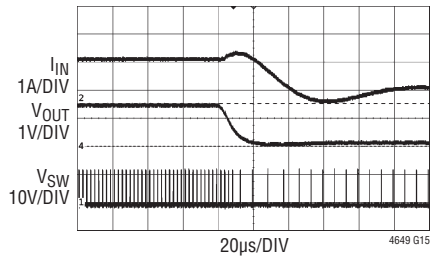
$12V_{IN}$, $1.5V_{OUT}$
I_O = 10A START-UP
C_{SS} = 0.1µF

Short-Circuit Protection with No Load



$12V_{IN}$, $1.5V_{OUT}$
SHORT CIRCUIT WITH NO LOAD
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR

Short-Circuit Protection with Full Load



$12V_{IN}$, $1.5V_{OUT}$
SHORT CIRCUIT WITH FULL LOAD
C_{OUT} = 2 • 220µF 4V CERAMIC CAPACITOR

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (A1-A5, A7-A11, B1, B9-B11, E1, F3, F5, G1-G7): Ground Pins for Both Input and Output Returns. All ground pins need to connect with large copper areas underneath the unit.

TEMP (A6): Onboard Temperature Diode for Monitoring the V_{BE} Junction Voltage Change with Temperature. See the Applications Information section.

CLKIN (B3): External Synchronization Input to Phase Detector Pin. A clock on this pin will enable synchronization with forced continuous operation. See the Applications Information section.

PHMODE (B4): This pin can be tied to GND, tied to $INTV_{CC}$ or left floating. This pin determines the relative phases between the internal controllers and the phasing of the CLKOUT signal. See Table 2 in the Operation section.

MODE (B5): Mode Select Input. Connect this pin to $INTV_{CC}$ to enable Burst Mode operation. Connect to ground to enable forced continuous mode of operation. Floating this pin will enable pulse-skipping mode.

NC (B7-B8, C3-C4): No Connection Pins. Either float these pins or connect them to GND for thermal purpose.

V_{IN} (C1, C8, C9, D1, D3-D5, D7-D9 and E8): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT} (C10-C11, D10-D11, E9-E11, F9-F11, G10-G11): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

SW (C5): Switching Node of the Circuit. This pin is used to check the switching frequency. Leave pin floating. A resistor-capacitor snubber can be placed from SW to GND to eliminate high frequency switch node ringing. See the Applications Information section.

PGOOD (C7): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point.

V_{OUT_LCL} (G9): This pin is connected to the top of the internal top feedback resistor for the output. When the remote sense amplifier is used, connect the remote sense amplifier output DIFFOUT to V_{OUT_LCL} to drive the 10k top feedback resistor. When the remote sense amplifier is not used, connect V_{OUT_LCL} to V_{OUT} directly.

FREQ (E3): Frequency Set Pin. A 10µA current is sourced from this pin. A resistor from this pin to ground sets a voltage, that in turn, programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the Applications Information section. The LTM4649 has an internal resistor to program the frequency to 450kHz.

TRACK/SS (E5): Output Voltage Tracking Pin and Soft-Start Inputs. The pin has a 1.2µA pull-up current source. A capacitor from this pin to ground will set a soft-start ramp rate. In tracking, the regulator output can be tracked to a different voltage. The different voltage is applied to a voltage divider then the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. See the Applications Information section.

V_{FB} (E7): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT_LCL} with a 10k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and ground pins. In PolyPhase operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section for details.

RUN (F1): Run Control Pin. A voltage above 1.25V will turn on the module. The RUN pin has a 1µA pull-up current, and then once the RUN pin reaches 1.2V an additional 4.5µA pull-up current is added to this pin.

PIN FUNCTIONS

CLKOUT (F2): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT is determined by the state of the PHMODE pin.

$INTV_{CC}$ (F4): Internal 5V LDO for Driving the Control Circuitry and the Power MOSFET Drivers. The 5V LDO has an absolute maximum 100mA peak current limit.

COMP (F6): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Tie all COMP pins together in parallel operation.

DIFFN (F7): Input to the Remote Sense Amplifier. This pin connects to the ground remote sense point. Connect to ground when not used.

DIFFP (F8): Input to the Remote Sense Amplifier. This pin connects to the output remote sense point. Connect to ground when not used.

DIFFOUT (G8): Output of the Remote Sense Amplifier. This pin connects to the V_{OUT_LCL} pin for remote sense applications. Otherwise float when not used.

BLOCK DIAGRAM

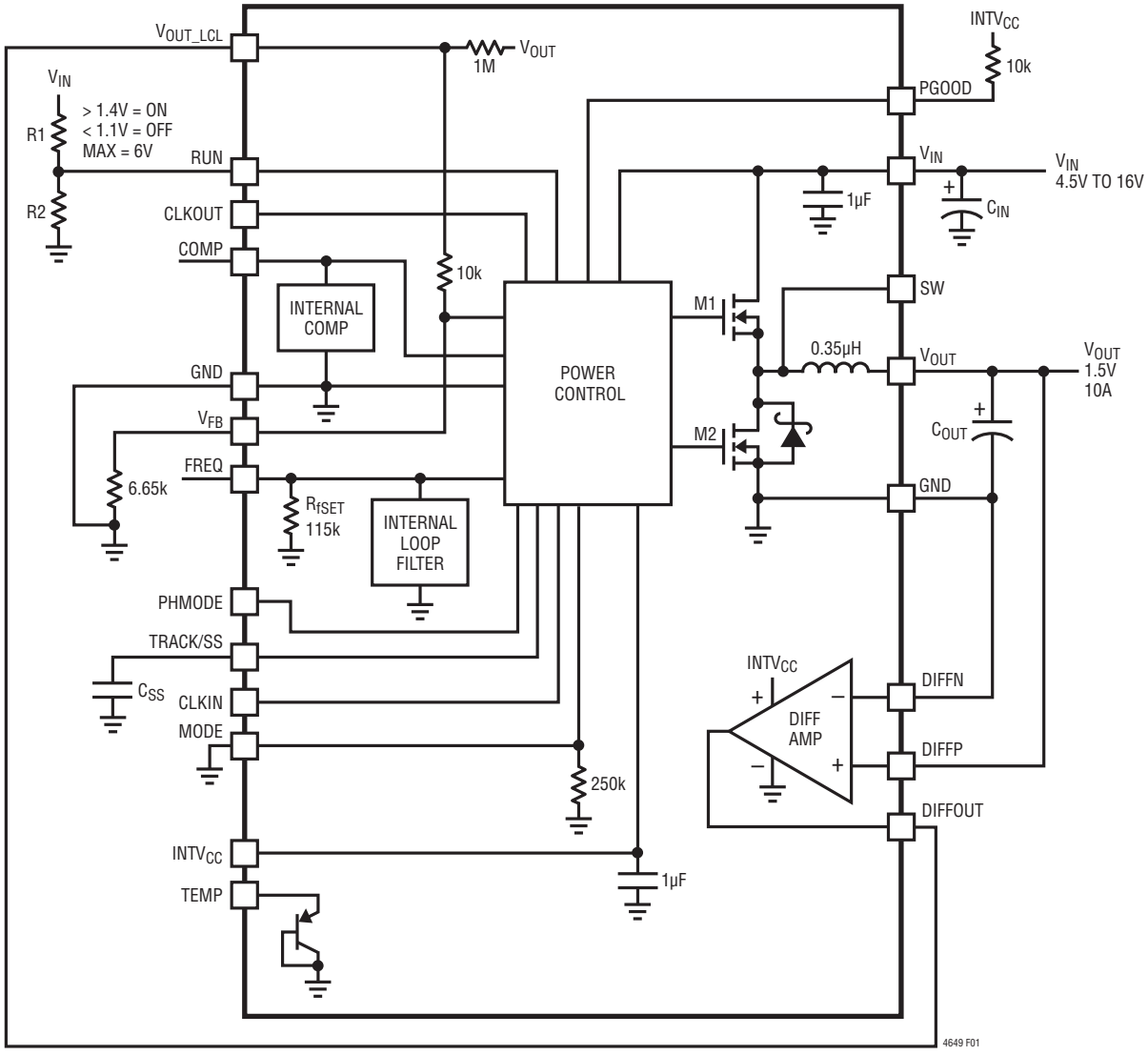


Figure 1. Simplified LTM4649 Block Diagram

OPERATION

Power Module Description

The LTM4649 is a high performance single output standalone nonisolated switching mode DC/DC power supply. It can provide up to 10A output current with few external input and output capacitors. This module provides precisely regulated output voltage programmable via an external resistor from 0.6VDC to 3.3VDC over a 4.5V to 16V input range. The typical application schematic is shown in Figure 17.

The LTM4649 has an integrated constant-frequency current mode regulator, power MOSFETs, inductor, and other supporting discrete components. The typical switching frequency is 450kHz. For switching noise-sensitive applications, it can be externally synchronized from 400kHz to 800kHz. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4649 module has sufficient stability margins and good transient performance with a wide range of output capacitors, especially with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit in an overcurrent condition. An internal overvoltage monitor protects the output voltage in the event of an overvoltage >10%. The top MOSFET is turned off and the bottom MOSFET is turned on until the output is cleared.

Pulling the RUN pin below 1.1V forces the regulator into a shutdown state. The TRACK/SS pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Application Information section.

The LTM4649 is internally compensated to be stable over all operating conditions. Table 3 provides a guideline for input and output capacitances for several operating conditions. LTpowerCAD™ is available for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground.

A remote sense amplifier is provided in the LTM4649 for accurately sensing output voltages ≤3.3V at the load point.

Multiphase operation can be easily employed with the synchronization inputs using an external clock source. See application examples.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

A TEMP pin is provided to allow the internal device temperature to be monitored using an onboard diode connected PNP transistor. This diode connected PNP transistor is grounded in the module and can be used as a general temperature monitor using a device that is designed to monitor the single-ended connection.

The switching node pin is available for functional operation monitoring. A resistor-capacitor snubber circuit can be carefully placed from the switching node pin to ground to dampen any high frequency ringing on the transition edges. See the Applications Information section for details.

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The typical LTM4649 application circuit is shown in Figure 17. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 3 for specific external capacitor requirements for particular applications.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage. The V_{IN} to V_{OUT} minimum dropout is a function of load current and at very low input voltage and high duty cycle applications output power may be limited as the internal top power MOSFET is not rated for 10A operation at higher ambient temperatures. At very low duty cycles a minimum 110ns on-time should be maintained. See the Frequency Adjustment section and temperature derating curves.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 10k internal feedback resistor connects the V_{OUT_LCL} and V_{FB} pins together. When the remote sense amplifier is used, then DIFFOUT is connected to the V_{OUT_LCL} pin. If the remote sense amplifier is not used, then V_{OUT_LCL} connects to V_{OUT}. The output voltage will default to 0.6V with no feedback resistor. Adding a resistor R_{FB} from V_{FB} to ground programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{10k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}(V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3
R_{FB}(k)	OPEN	15	10	6.65	4.99	3.16	2.21

For parallel operation of N LTM4649, the following equation can be used to solve for R_{FB}:

$$R_{FB} = \frac{\frac{10k}{N}}{\frac{V_{OUT}}{0.6} - 1}$$

In parallel operation the V_{FB} pins have an I_{FB} current of 25nA maximum each channel. To reduce output voltage error due to this current, an additional V_{OUT_LCL} pin can be tied to V_{OUT}, and an additional R_{FB} resistor can be used to lower the total Thevenin equivalent resistance seen by this current.

Input Capacitors

The LTM4649 module should be connected to a low AC impedance DC source. Additional input capacitors are needed for the RMS input ripple current rating. The $I_{CIN(RMS)}$ equation which follows can be used to calculate the input capacitor requirement. Typically 22µF X7R ceramics are a good choice with RMS ripple current ratings of ~2A each. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the previous equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated aluminum electrolytic capacitor or a polymer capacitor.

Output Capacitors

The LTM4649 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, low ESR Polymer capacitor or ceramic capacitors. The typical output capacitance range is from 200µF to 470µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient

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spikes is required. Table 3 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 3 matrix, and LTpowerCAD is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. LTpowerCAD can calculate the output ripple reduction as the number of implemented phase's increases by N times.

Burst Mode Operation

The LTM4649 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply tie the MODE pin to $INTV_{CC}$. During Burst Mode operation, the peak current of the inductor is set to approximately 30% of the maximum peak current value in normal operation even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise, the internal sleep line goes low, and the LTM4649 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4649 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Floating the MODE pin enables pulse-skipping operation. With pulse-skipping mode at light load, the internal current comparator may remain tripped for several cycles, thus skipping operation cycles. This mode has lower ripple than Burst Mode operation and maintains a higher frequency operation than Burst Mode operation.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE pin to ground. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4649's output voltage is in regulation.

Frequency Selection

The LTM4649 device is internally programmed to 450kHz switching frequency to improve power conversion efficiency. It is recommended for all applications with low V_{IN} or low V_{OUT}. For applications with high V_{IN} ($V_{IN} \geq$ 12V) and high V_{OUT} ($V_{OUT} \geq$ 1.8V), 750kHz is the recommended operating frequency to limit inductor ripple current. Simply tie FREQ to $INTV_{CC}$. Table 3 lists different frequency and FREQ pin recommendations for different V_{IN}, V_{OUT} conditions.

If desired, a resistor can be connected from the FREQ pin to $INTV_{CC}$ to adjust the FREQ pin DC voltage to increase the switching frequency between the default 450kHz and the maximum 750kHz. Figure 2 shows a graph of frequency versus FREQ pin DC voltage. Figure 18 shows an example where the frequency is programmed to 650kHz. Please be aware the FREQ pin has an internal 10µA current sourced from this pin when calculating the resistor value.

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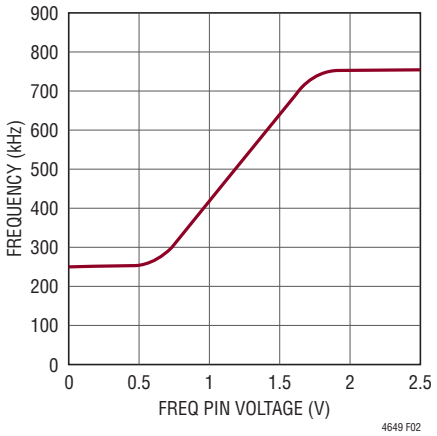

Figure 2. Operating Frequency vs FREQ Pin Voltage

PLL and Frequency Synchronization

The LTM4649 device operates over a range of frequencies to improve power conversion efficiency. The nominal switching frequency is 450kHz. It can also be synchronized from 400kHz to 800kHz with an input clock that has a high level above 2V and a low level below 0.8V at the CLKIN pin. Once the LTM4649 is synchronizing to an external clock frequency, it will always be running in Forced Continuous operation. Although synchronization to 250kHz is possible, 400kHz is the lowest recommended operating frequency to limit inductor ripple current.

Multiphase Operation

For outputs that demand more than 10A of load current, multiple LTM4649 devices can be paralleled to provide more output current and reduced input and output voltage ripple.

The CLKOUT signal together with CLKIN pin can be used to cascade additional power stages to achieve a multiphase power supply solution. Tying the PHMODE pin to $INTV_{CC}$, GND, or leaving it floating generates a phase difference (between CLKIN and CLKOUT) of 180°, 120°, or 90° respectively as shown in Table 2. A total of 4 phases can be cascaded to run simultaneously with respect to each other by programming the PHMODE pin of each LTM4649 channel to different levels. Figure 3 shows a 3-phase design and 4-phase design example for clock phasing with the PHMODE table.

Table 2. PHMODE and CLKOUT Signal Relationship

PHMODE	GND	FLOAT	$INTV_{CC}$
CLKOUT	120°	90°	180°

The LTM4649 device is an inherently current mode controlled device, so parallel modules will have good current sharing. This will balance the thermals in the design. Tie the COMP, V_{FB}, TRACK/SS and RUN pins of each LTM4649 together to share the current evenly. Figures 19 and 20 each show a schematic of a parallel design.

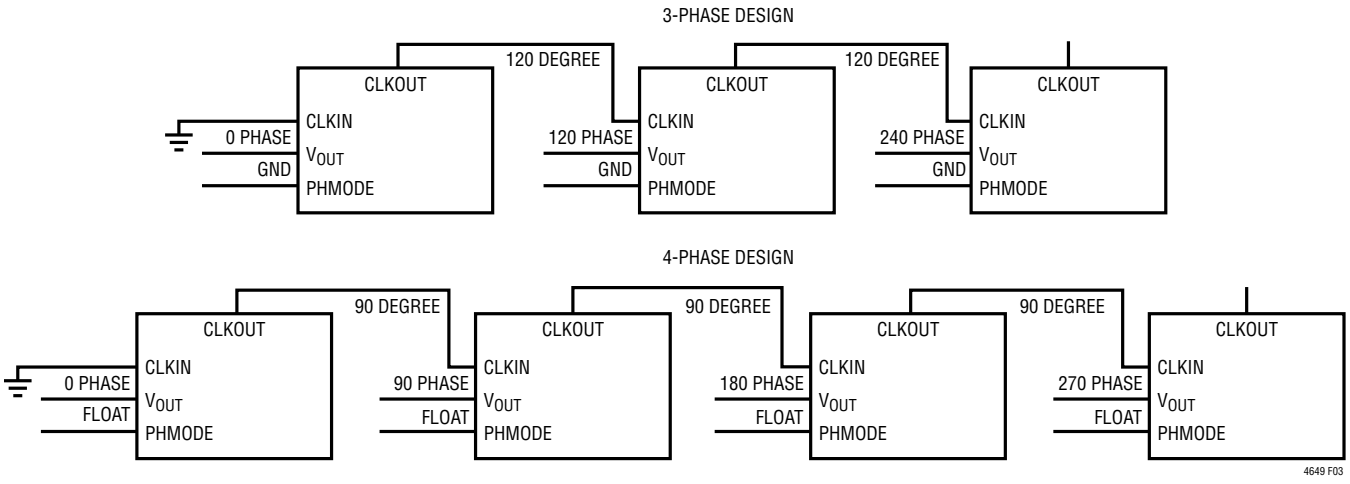

Figure 3. Examples of 3-Phase, 4-Phase Operation with PHMODE Table

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A multiphase power supply could significantly reduce the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases (see Figure 4).

Minimum On-Time

Minimum on-time t_{ON} is the smallest time duration that the LTM4649 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \bullet FREQ} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple and current will increase. The minimum on-time can be increased by lowering the switching frequency. A good rule of thumb is to assume a 110ns minimum on-time.

Soft-Start

The TRACK/SS pin of the master can be controlled by a capacitor placed from the master regulator TRACK/SS pin to ground. A 1.2µA current source will charge the TRACK/SS pin up to the reference voltage and then proceed up to

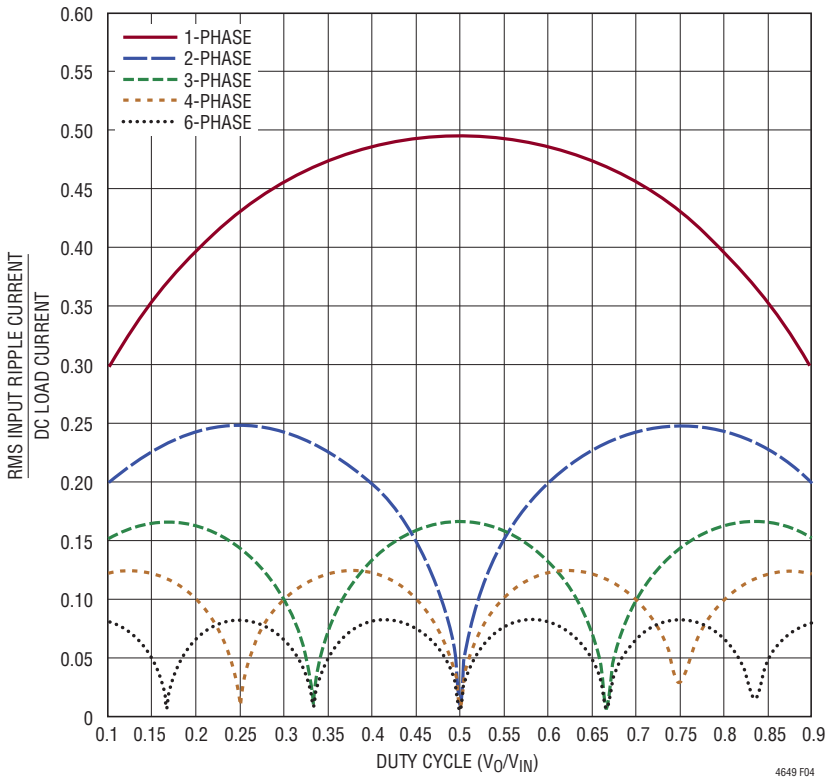

Figure 4. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

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$INTV_{CC}$. After ramping to 0.6V, the TRACK/SS pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. Foldback current limit is disabled during this sequence of turn-on during tracking or soft-starting. The TRACK/SS pin is pulled low when the RUN pin is below 1.2V. The total soft-start time can be calculated as:

$$t_{SS} = \left(\frac{C_{SS}}{1.2\mu A}\right) \bullet 0.6V$$

Regardless of the mode selected by the MODE pin, the regulator will always start in pulse-skipping mode up to TRACK/SS = 0.5V. Between TRACK/SS = 0.5V and 0.54V, it will operate in forced continuous mode and revert to the selected mode once TRACK/SS > 0.54V. In order to track with another regulator once in steady state operation, the LTM4649 is forced into continuous mode operation as soon as V_{FB} is below 0.54V regardless of the setting on the MODE pin.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4649 uses an accurate 10k resistor internally for the top feedback resistor. Figure 6 shows the coincident tracking characteristic.

$$V_{SLAVE} = \left(1 + \frac{10k}{R_{TA}}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.6V, or the internal reference voltage. When the master's output is divided

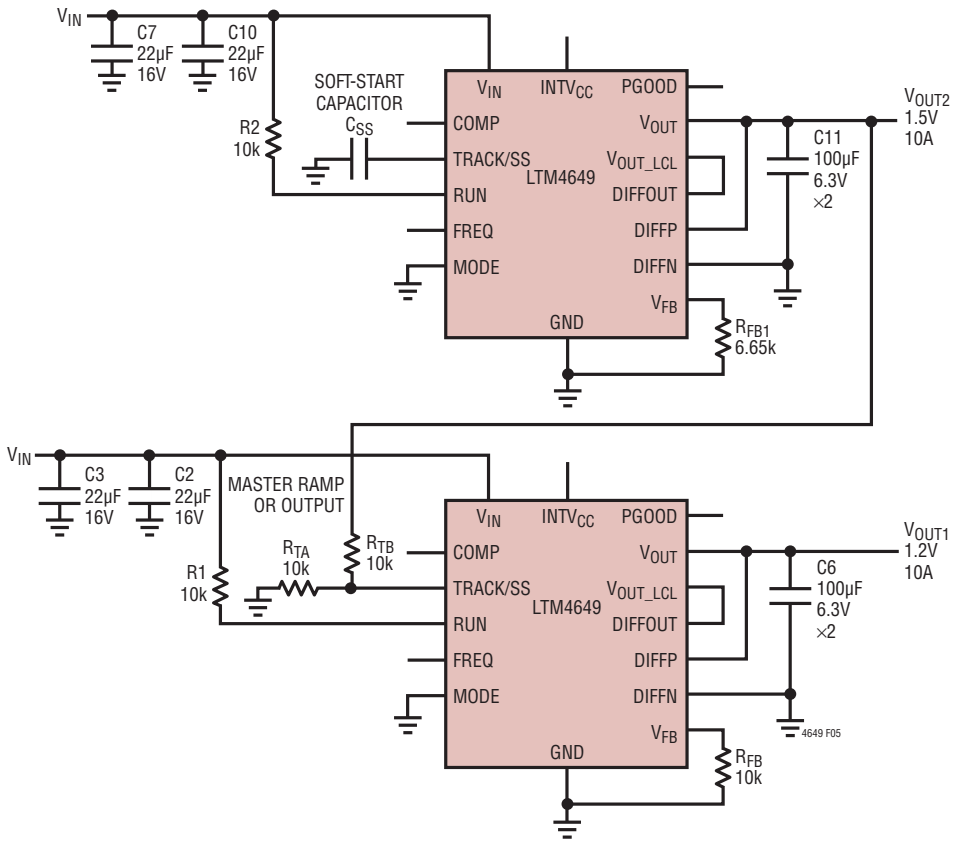

Figure 5. Dual Outputs (1.5V and 1.2V) with Tracking

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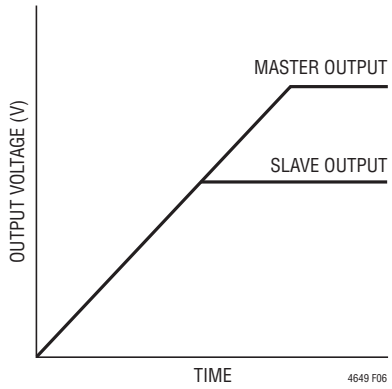

Figure 6. Output Coincident Tracking Characteristic

down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when V_{TRACK} is more than 0.6V. RTA in Figure 5 will be equal to R_{FB} for coincident tracking.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK/SS pin. As mentioned above, the TRACK/SS pin has a control range from 0V to 0.6V. The master's TRACK/SS pin slew rate is directly equal to the master's output slew rate in Volts/Time. The equation for R_{TB}:

$$\frac{MR}{SR} \bullet 10k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal to 10k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.6V}{\frac{V_{FB}}{10k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.6V. Since R_{TB} is equal to the 10k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB} with $V_{FB} = V_{TRACK}$. Therefore R_{TB} = 10k, and R_{TA} = 10k in Figure 5.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

Each of the TRACK/SS pins will have the 1.3µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK/SS pin input. Smaller value resistors with the same ratios as the resistor values calculated from the previous equations can be used. For example, where the 10k value is calculated then a 1.0k can be used to reduce the TRACK/SS pin offset to a negligible value.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point. A pull-up resistor can be connected from PGOOD to a supply voltage no greater than 6V.

Stability Compensation

The module has already been internally compensated for all output voltages. Table 3 is provided for most application requirements. LTpowerCAD is available for other control loop optimization.

Run Enable

The RUN pin has an enable threshold of 1.4V maximum, typically 1.25V with 150mV of hysteresis. It controls the turn-on of the µModule. The RUN pin can be pulled up to V_{IN} for 5V operation, or a 5V Zener diode can be placed on the pin and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the µModule. The RUN pin can also be used for output voltage sequencing.

In parallel operation the RUN pins can be tied together and controlled from a single control. See the Typical Application circuits in Figures 19 and 20. The RUN pin can also be left floating. The RUN pin has a 1µA pull-up current source that increases to 4.5µA during ramp-up.

Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is provided in the LTM4649 to sense low output voltages accurately at the remote load points. This is especially applicable for

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high current loads. It is very important that the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to V_{OUT_LCL}. Review the parallel schematics in Figures 19 and 20.

SW Pins

The SW pin is generally used for testing purposes. The SW pin can also be used to dampen out switch node ringing caused by LC parasitic in the switched current path. Usually a series R-C combination is used, referred to as a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor.

If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to determine. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored using a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z_L = 2\pi \bullet f \bullet L$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by:

$$Z_C = \frac{1}{2\pi \bullet f \bullet C}$$

These values are a good place to start. Modification to these components should be made to attenuate the ringing with the least amount of power loss.

Temperature Monitoring

A diode connected PNP transistor is used for the TEMP monitor function by monitoring its voltage over temperature. The temperature dependence of this diode voltage can be understood in the equation:

$$V_D = nV_T \ln\left(\frac{I_D}{I_S}\right)$$

where V_T is the thermal voltage (kT/q), and n, the ideality factor, is 1 for the diode connected PNP transistor being used in the LTM4649. I_S is expressed by the typical empirical equation:

$$I_S = I_0 \exp\left(\frac{-V_{G0}}{V_T}\right)$$

where I_0 is a process and geometry dependent current, (I_0 is typically around 20k orders of magnitude larger than I_S at room temperature) and V_{G0} is the band gap voltage of 1.2V extrapolated to absolute zero or –273°C.

If we take the I_S equation and substitute into the V_D equation, then we get:

$$V_D = V_{G0} - \left(\frac{k_T}{q}\right)\ln\left(\frac{I_0}{I_D}\right), V_T = \frac{kT}{q}$$

The expression shows that the diode voltage decreases (linearly if I_0 were constant) with increasing temperature and constant diode current. Figure 7 shows a plot of V_D vs Temperature over the operating temperature range of the LTM4649.

If we take this equation and differentiate it with respect to temperature T, then:

$$\frac{dV_D}{dT} = -\frac{V_{G0} - V_D}{T}$$

This dV_D/dT term is the temperature coefficient equal to about –2mV/K or –2mV/°C. The equation is simplified for the first order derivation.

Solving for T, $T = -(V_{G0} - V_D)/(dV_D/dT)$ provides the temperature.

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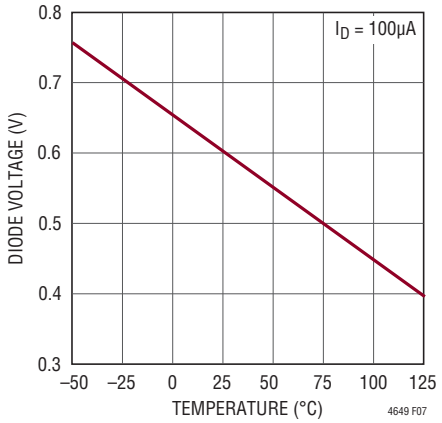

Figure 7. Diode Voltage V_D vs Temperature T(°C)

1st Example: Figure 7 for 27°C, or 300K the diode voltage is 0.598V, thus, 300K = –(1200mV – 598mV)/–2.0mV/K).

2nd Example: Figure 7 for 75°C, or 350K the diode voltage is 0.5V, thus, 350K = –(1200mV – 500mV)/–2.0mV/K).

Converting the Kelvin scale to Celsius is simply taking the Kelvin temperature and subtracting 273 from it.

Measure the forward voltage at 27°C to establish a reference point. Then using the above expression while measuring the forward voltage over temperature will provide a general temperature monitor. Connect a resistor between TEMP and V_{IN} to set the current to 100µA. See Figure 21 for an example.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}: the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}: the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB}: the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule package and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of

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the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 8; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4649, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4649 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4649 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves shown in this data sheet. After these laboratory tests have been performed and correlated to the LTM4649 model, then the θ_{JB} and θ_{BA} values are summed together to correlate quite well with the µModule model for θ_{JA} with

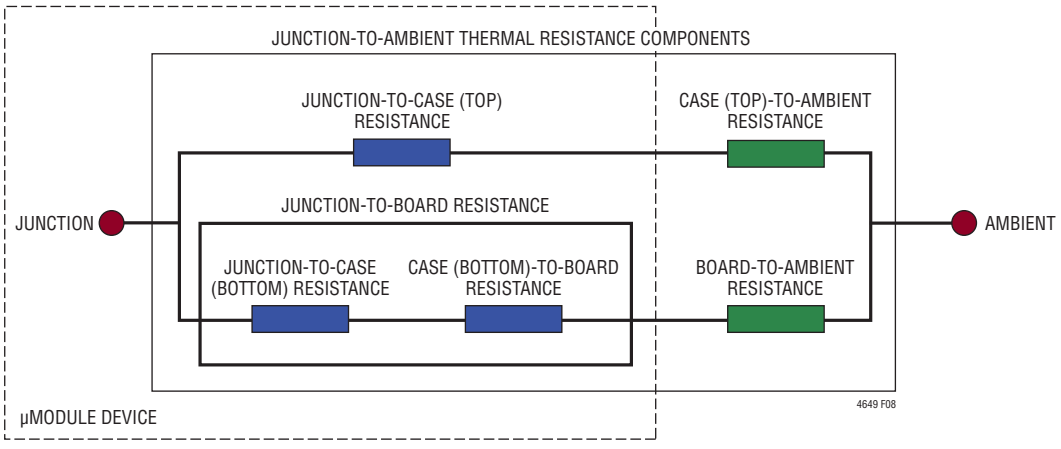

Figure 8. Graphical Representation of JESD51-12 Thermal Coefficients

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no airflow or heat sinking in a properly defined chamber. This θ_{JB} + θ_{BA} value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The $5V_{IN}$ and $12V_{IN}$ power loss curves in Figures 9 and 10 can be used in coordination with the load current derating curves in Figures 11 to 14 for calculating an approximate θ_{JA} thermal resistance for the LTM4649 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a multiplicative factor according to the ambient temperature. This approximate factor is: 1.4 for 120°C. The derating curves are plotted with the output current starting at 10A and the ambient temperature at 40°C. The output voltages are 1.5V and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored

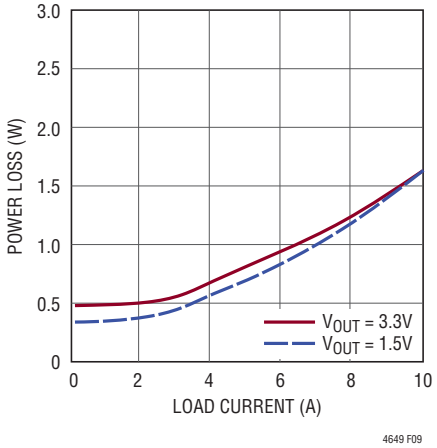


Figure 9. $5V_{IN}$, $3.3V_{OUT}$ and $1.5V_{OUT}$ Power Loss

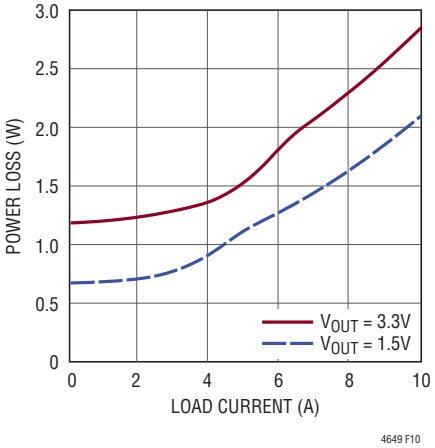


Figure 10. $12V_{IN}$, $3.3V_{OUT}$ and $1.5V_{OUT}$ Power Loss

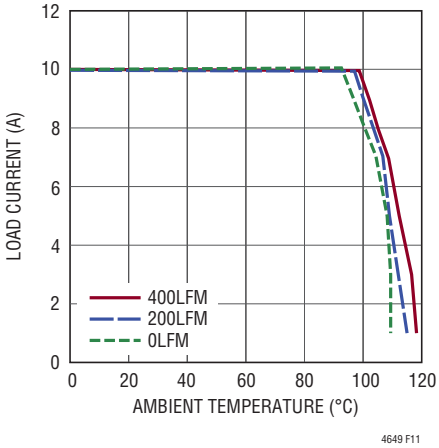


Figure 11. No Heat Sink with $5V_{IN}$ to $1.5V_{OUT}$

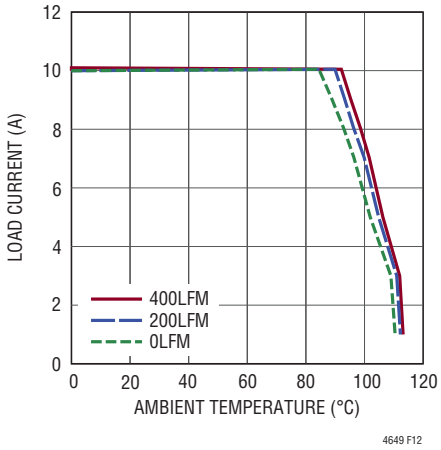


Figure 12. No Heat Sink with $12V_{IN}$ to $1.5V_{OUT}$

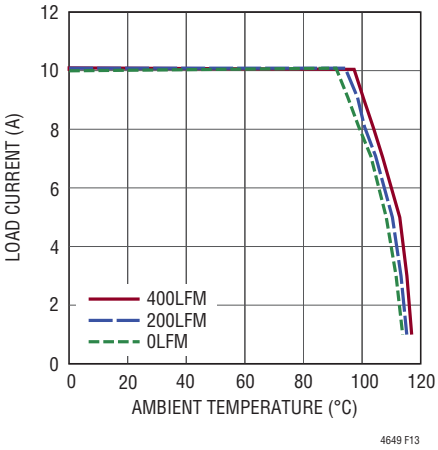


Figure 13. No Heat Sink with $5V_{IN}$ to $3.3V_{OUT}$

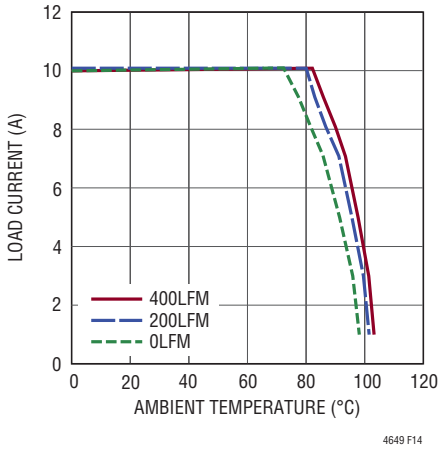


Figure 14. No Heat Sink with $12V_{IN}$ to $3.3V_{OUT}$

APPLICATIONS INFORMATION

while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 12 the load current is derated to ~8A at ~90°C with no air or heat sink and the power loss for the 12V to 1.5V at 8A output is about 2.24W. The 2.24W loss is calculated with the 1.6W room temperature loss from the 12V to 1.5V power loss curve at 8A, and the 1.40 multiplying factor at 120°C junction. If the 90°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 30°C divided by 2.24W equals a 13°C/W θ_{JA} thermal resistance. Table 4 specifies a 14°C/W value which is very close. Table 4 and Table 5 provide equivalent thermal resistances for 1.5V and 3.3V outputs with and without airflow. The derived thermal resistances in Tables 4 and 5 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

Safety Considerations

The LTM4649 module does not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

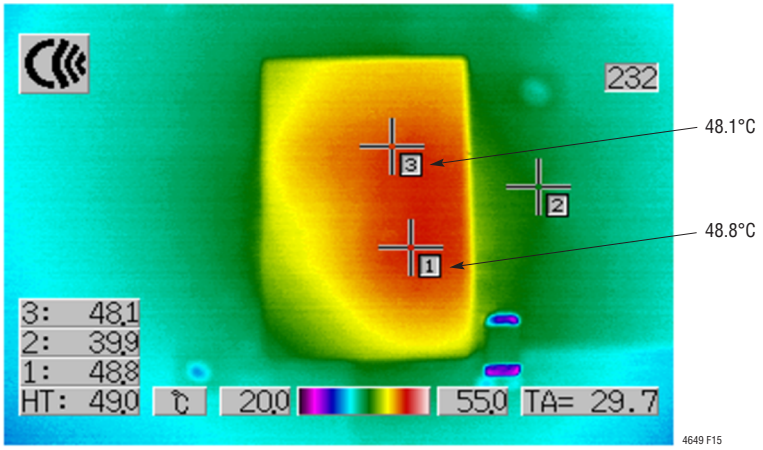


Figure 15. Thermal Image 12V to 1.5V at 10A
(No Heat Sink, No Air Flow. At Room Temperature Ambient)

APPLICATIONS INFORMATION

Layout Checklist/Example

The high integration of LTM4649 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pads, unless they are capped.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.

Figure 16 gives a good example of the recommended layout.

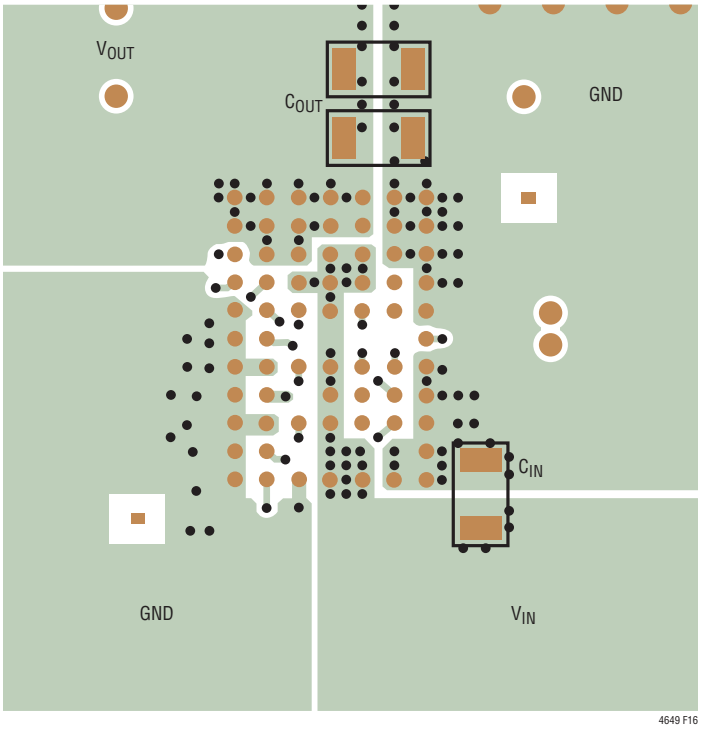


Figure 16. Recommended PCB Layout

APPLICATIONS INFORMATION

Table 3. Output Voltage Response vs Component Matrix (Refer to Figure 18) 0A to 5A Load Step Typical Measured Values

C_{IN} (BULK)*	VENDORS	PART NUMBER	C_{IN} (CERAMIC)	VENDORS	PART NUMBER	C_{OUT} (CERAMIC)	VENDORS	PART NUMBER
150µF, 16V	SANYO OSCON	25HVH150MT	22µF, 16V	MURATA	GRM32ER71C226KE18L	100µF, 6.3V	MURATA	GRM32ER60J107ME20L
						220µF, 4V	MURATA	GRM31CR60G227M

V_{OUT}	V_{IN}	C_{IN} (BULK)*	C_{IN} (CERAMIC)	C_{OUT} (CERAMIC)	C_{FF}	LOAD STEP	V_{DROOP}	V_{P-P}	RECOVERY TIME	LOAD STEP SPEED	R_{FB}	SW FREQ	FREQ PIN
1V	5V, 12V	120µF*	22µF × 2	100µF × 3	None	75% to 100%	45mV	90mV	40µs	1A/µs	15kΩ	450kHz	Float
1.2V	5V, 12V	120µF*	22µF × 2	100µF × 3	None	75% to 100%	50mV	100mV	50µs	1A/µs	10kΩ	450kHz	Float
1.5V	5V, 12V	120µF*	22µF × 2	100µF × 3	None	75% to 100%	57mV	114mV	60µs	1A/µs	6.65kΩ	450kHz	Float
2.5V	5V	120µF*	22µF × 2	100µF × 3	None	75% to 100%	75mV	150mV	70µs	1A/µs	3.16kΩ	450kHz	Float
2.5V	12V	120µF*	22µF × 2	100µF × 3	None	75% to 100%	75mV	150mV	70µs	1A/µs	3.16kΩ	750kHz	$INTV_{CC}$
3.3V	5V	120µF*	22µF × 2	100µF × 3	None	75% to 100%	95mV	190mV	70µs	1A/µs	2.21kΩ	450kHz	Float
3.3V	12V	120µF*	22µF × 2	100µF × 3	None	75% to 100%	95mV	190mV	70µs	1A/µs	2.21kΩ	750kHz	$INTV_{CC}$
1V	5V, 12V	120µF*	22µF × 2	220µF × 2	None	50% to 100%	70mV	140mV	30µs	1A/µs	15kΩ	450kHz	Float
1.2V	5V, 12V	120µF*	22µF × 2	220µF × 2	None	50% to 100%	75mV	150mV	40µs	1A/µs	10kΩ	450kHz	Float
1.5V	5V, 12V	120µF*	22µF × 2	220µF × 2	None	50% to 100%	90mV	180mV	40µs	1A/µs	6.65kΩ	450kHz	Float
2.5V	5V	120µF*	22µF × 2	220µF × 2	None	50% to 100%	135mV	270mV	50µs	1A/µs	3.16kΩ	450kHz	Float
2.5V	12V	120µF*	22µF × 2	220µF × 2	None	50% to 100%	135mV	270mV	50µs	1A/µs	3.16kΩ	750kHz	$INTV_{CC}$
3.3V	5V	120µF*	22µF × 2	220µF × 2	None	50% to 100%	175mV	350mV	60µs	1A/µs	2.21kΩ	450kHz	Float
3.3V	12V	120µF*	22µF × 2	220µF × 2	None	50% to 100%	175mV	350mV	60µs	1A/µs	2.21kΩ	750kHz	$INTV_{CC}$

*Bulk capacitor is optional if V_{IN} has very low input impedance.

Table 4. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figures 11, 12	5, 12	Figure 9	0	None	14
Figures 11, 12	5, 12	Figure 9	200	None	12
Figures 11, 12	5, 12	Figure 9	400	None	10

Table 5. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figures 13, 14	5, 12	Figure 10	0	None	14
Figures 13, 14	5, 12	Figure 10	200	None	12
Figures 13, 14	5, 12	Figure 10	400	None	10

TYPICAL APPLICATIONS

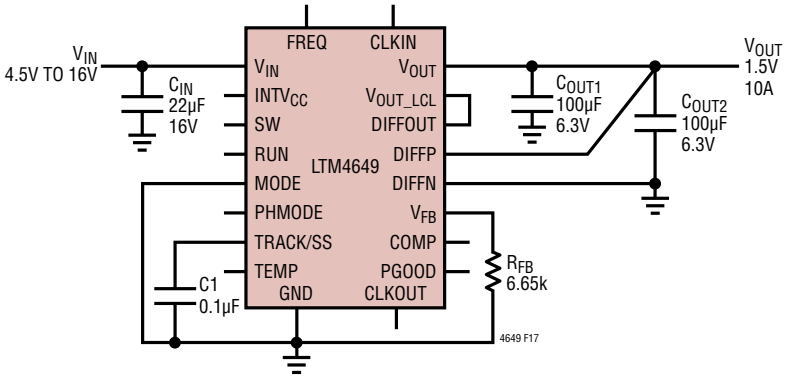


Figure 17. 4.5V to 16V_{IN}, 1.5V at 10A Design

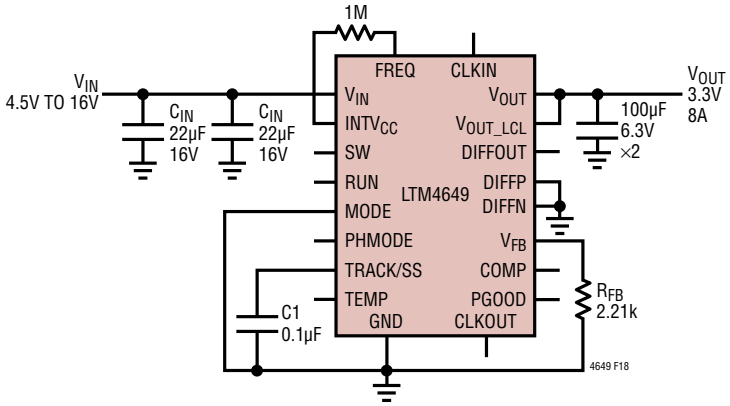


Figure 18. 4.5V to 16V V_{IN}, 3.3V_{OUT} at 8A Design with Increased 650kHz Frequency

TYPICAL APPLICATIONS

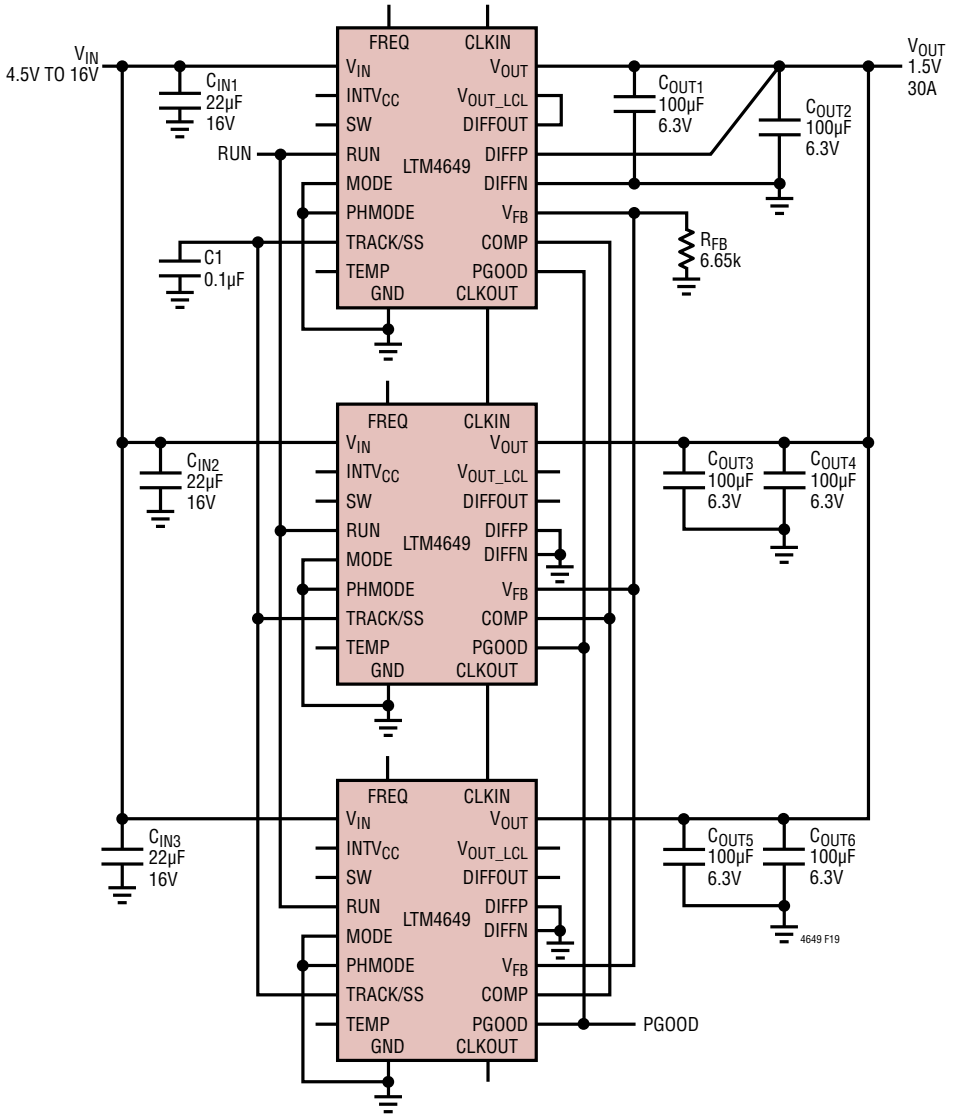


Figure 19. Three LTM4649 in Parallel, 1.5V at 30A Design

TYPICAL APPLICATIONS

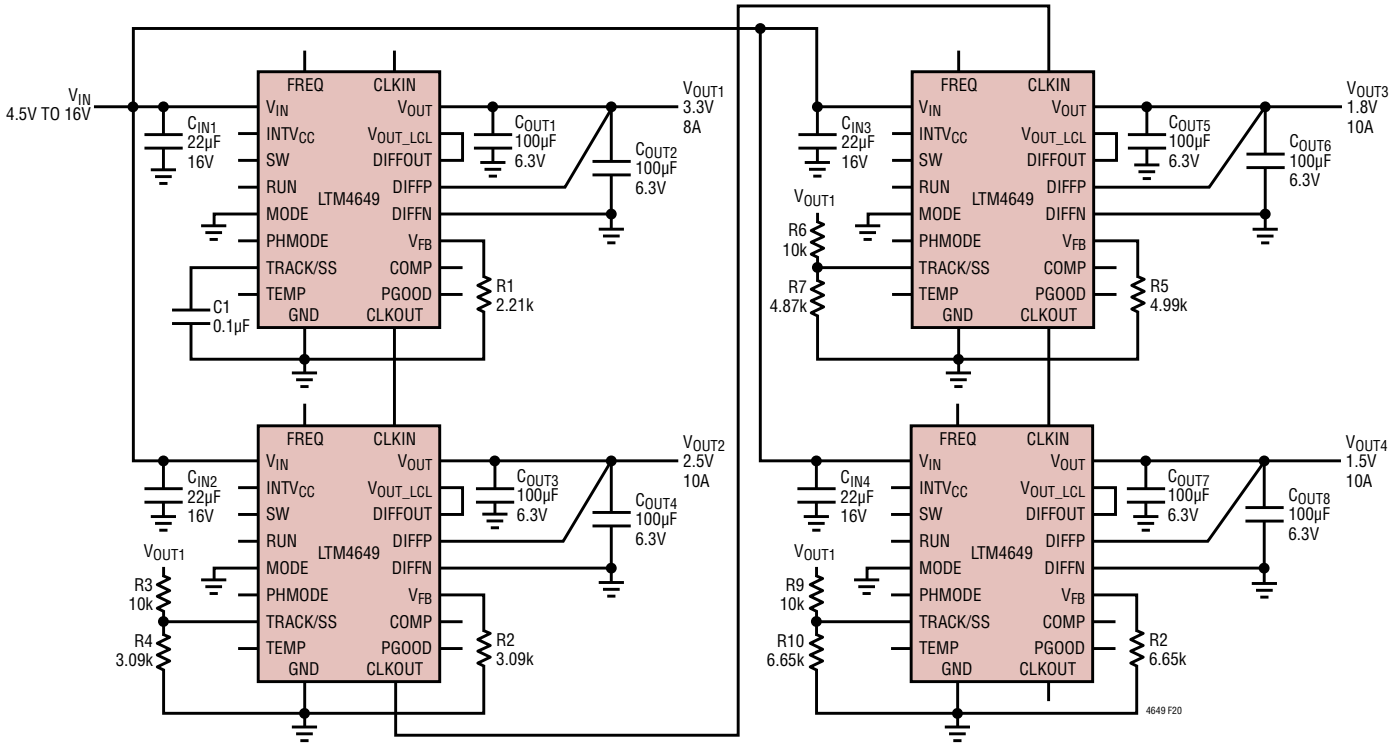


Figure 20. Quad Outputs 4-Phase LTM4649 Regulator with Tracking Function

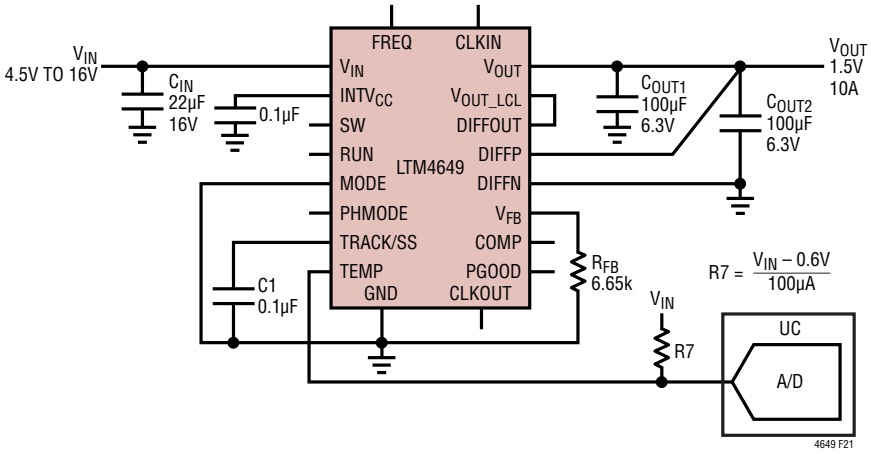
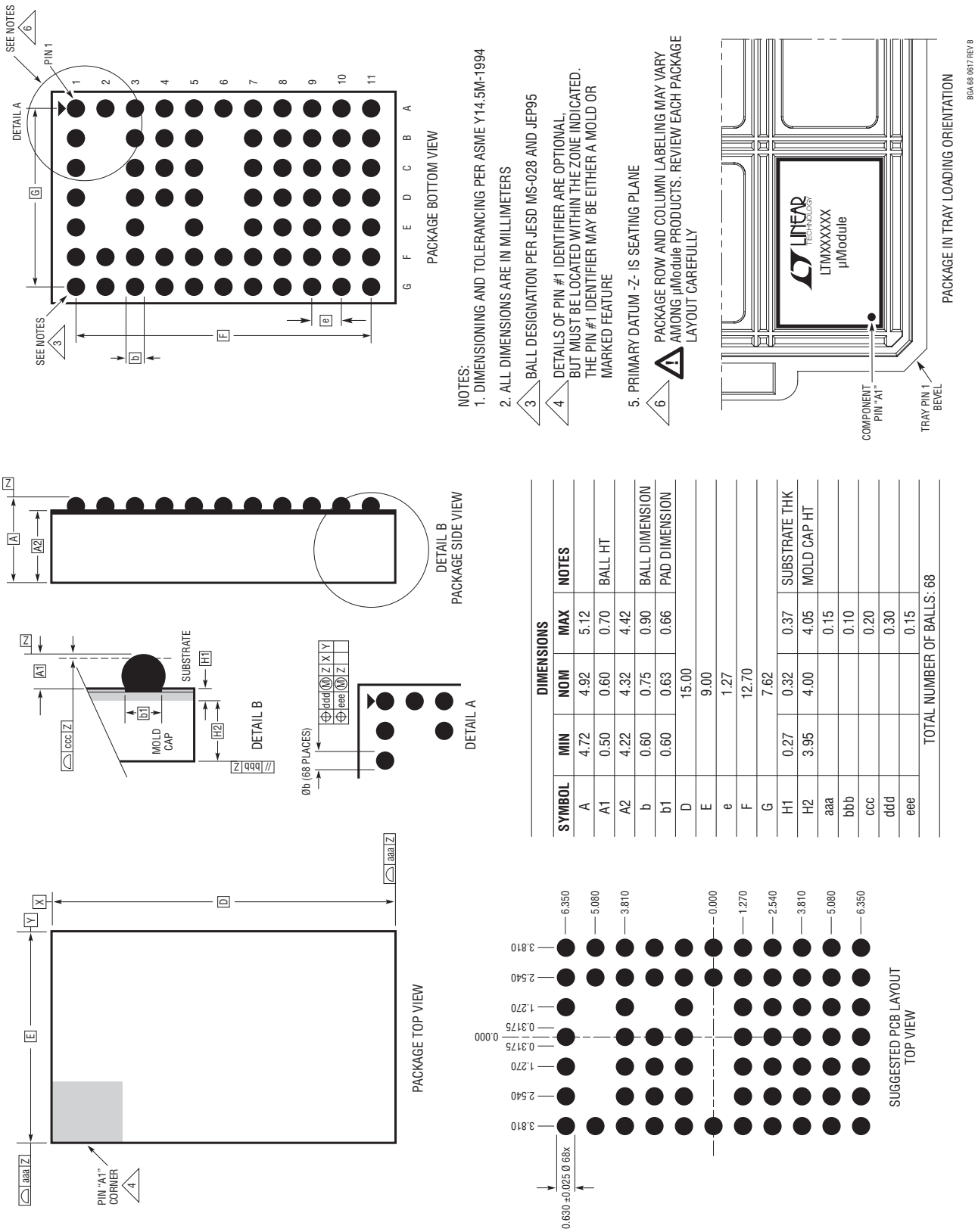


Figure 21. Single LTM4649 10A Design with Temperature Monitoring

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM4649#packaging/ for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	BALL HT
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.00		
E		9.00		
e		1.27		
F		12.70		
G		7.62		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 68				

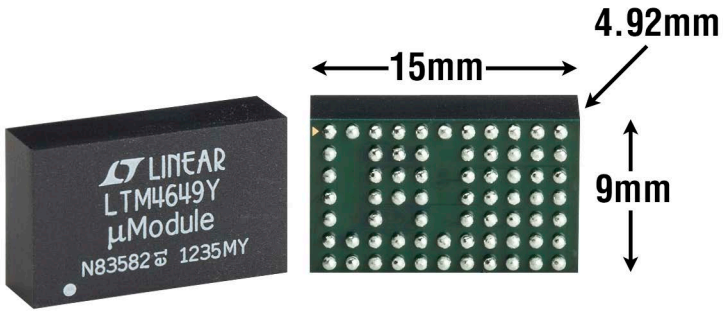
PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM4649 BGA Pin Assignment Table

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	B1	GND	C1	V_{IN}	D1	V_{IN}	E1	GND	F1	RUN	G1	GND
A2	GND	B2	–	C2	–	D2	–	E2	–	F2	CLCKOUT	G2	GND
A3	GND	B3	CLKIN	C3	NC	D3	V_{IN}	E3	FREQ	F3	GND	G3	GND
A4	GND	B4	PHMODE	C4	NC	D4	V_{IN}	E4	–	F4	INTVCC	G4	GND
A5	GND	B5	MODE	C5	SW	D5	V_{IN}	E5	TRACK/SS	F5	GND	G5	GND
A6	TEMP	B6	–	C6	–	D6	–	E6	–	F6	COMP	G6	GND
A7	GND	B7	NC	C7	PGOOD	D7	V_{IN}	E7	FB	F7	DIFFN	G7	GND
A8	GND	B8	NC	C8	V_{IN}	D8	V_{IN}	E8	V_{IN}	F8	DIFFP	G8	DIFFOUT
A9	GND	B9	GND	C9	V_{IN}	D9	V_{IN}	E9	V_{OUT}	F9	V_{OUT}	G9	V_{OUT_LCL}
A10	GND	B10	GND	C10	V_{OUT}	D10	V_{OUT}	E10	V_{OUT}	F10	V_{OUT}	G10	V_{OUT}
A11	GND	B11	GND	C11	V_{OUT}	D11	V_{OUT}	E11	V_{OUT}	F11	V_{OUT}	G11	V_{OUT}

PACKAGE PHOTO



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/14	Added SnPb (lead) BGA package.	1, 2
		Figures 9 and 10 changed Y-Axis to Power Loss (W).	20
B	12/15	Corrected R_{FB} (k) for 2.5V from 3.06 to 3.16.	11
		Revised Temperature Monitoring discussion.	17
		Added CLKOUT, PHMODE and SW pins on Block Diagram.	9
C	7/17	Corrected note number to COMP from Note 6 to Note 3.	2

TYPICAL APPLICATION

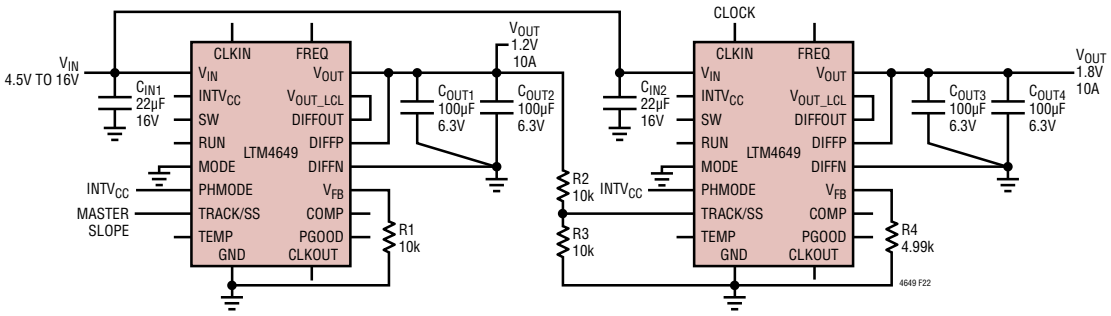


Figure 22. Dual Output 1.2V, 1.8V 2-Phase LTM4649 Regulator with Tracking

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4627	20V, 15A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5V$, PLL input, Remote Sense Amplifier, V_{OUT} Tracking, 15mm × 15mm × 4.3mm LGA and 15mm × 15mm × 4.9mm BGA
LTM4620A	Dual 16V, 13A or Single 26A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 5.3V$, PLL Input, Remote Sense Amplifier, V_{OUT} Tracking, 15mm × 15mm × 4.41mm LGA
LTM4613	$36V_{IN}$, 8A EN55022 Class B Certified DC/DC Step-Down µModule Regulator	$5V \le V_{IN} \le 36V$, $3.3V \le V_{OUT} \le 15V$, PLL Input, V_{OUT} Tracking and Margining, 15mm × 15mm × 4.32mm LGA
LTM8045	Inverting or SEPIC µModule DC/DC Converter with Up to 700mA Output Current	$2.8V \le V_{IN} \le 18V$, $\pm2.5V \le V_{OUT} \le \pm15V$, Synchronizable, 6.25mm × 11.25mm × 4.92mm BGA
LTM8061	32V, 2A Step-Down µModule Battery Charger with Programmable Input Current Limit	CC-CV Charging Single and Dual Cell Li-Ion or Li-Poly Batteries, $4.95V \le V_{IN} \le 32V$, C/10 or Adjustable Timer Charge Termination, 9mm × 15mm × 4.32mm LGA
LTM8048	1.5W, 725VDC Galvanically Isolated µModule Converter with LDO post regulator	$3.1V \le V_{IN} \le 32V$, $2.5V \le V_{OUT} \le 12V$, $1mV_{PP}$ Output Ripple, Internal Isolated Transformer, 9mm × 11.25mm × 4.92mm BGA
LTC2974	Quad Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, Per Channel Voltage, Current and Temperature Measurements

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