4.7 Ω R_{ON}, Quad SPDT Switch with 1.2 V and 1.8 V JEDEC Logic Compliance

FEATURES

- 4.7 Ω typical on resistance for ±5 V dual supply at 25°C
- 1.2 Ω on-resistance flatness for ±5 V dual supply at 25°C
- Fully specified at ±5 V, +12 V, +5 V, and +3.3 V
  - ±3.3 V to ±8 V dual-supply operation
  - 3.3 V to 16 V single-supply operation
- V_L supply for low logic level compatibility
  - 1.8 V JEDEC standard compliant
  - 1.2 V JEDEC standard compliant
- Rail-to-rail operation
- 24-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- Communication systems
- Medical systems
- Audio signal routing
- Video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- FPGA and microcontroller systems
- Sample-and-hold systems
- Relay replacements

GENERAL DESCRIPTION

The ADG1634L is a monolithic industrial CMOS (*i*CMOS®) analog switch comprising four independently selectable single-pole, double-throw (SPDT) switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An EN input on the ADG1634L is used to enable or disable the device. When disabled, all channels are switched off. The switch is enabled with a Logic 1 EN input, while the INx input defines the state of the SPDT switch (see Table 12).

The ultralow on resistance and on-resistance flatness of the switch makes it an ideal solution for data acquisition and gain switching applications, where low distortion is critical. *i*CMOS construction ensures ultra low power dissipation, making the device ideally suited for portable and battery-powered instruments.

An external V_L supply provides flexibility for lower logic control. The ADG1634L is both 1.2 V and 1.8 V JEDEC standard compliant.

FUNCTIONAL BLOCK DIAGRAM

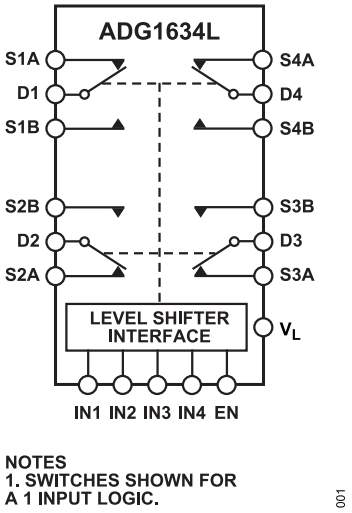

Figure 1.

PRODUCT HIGHLIGHTS

1. 8.2 Ω maximum on resistance over temperature.
2. Minimum distortion.
3. V_L supply for low logic level compatibility.
4. JEDEC standard compliant for both 1.2 V and 1.8 V logic levels.
5. Guaranteed switch off when digital inputs are floating.
6. 24-lead, 4 mm × 4 mm LFCSP.

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REVISION HISTORY

4/2022—Revision 0: Initial Version

SPECIFICATIONS

OPERATING SUPPLY VOLTAGES

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
Dual	±3.3		±8	V	V_{DD} to V_{SS}
Single	3.3		16	V	V_{DD} to GND, V_{SS} = GND = 0 V
DIGITAL VOLTAGE					
Single	1.1		1.3	V	V_L to GND, V_{INx} = 1.2 V logic
	1.65		1.95	V	V_L to GND, V_{INx} = 1.8 V logic

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, and V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +4.5 V, V_{SS} = −4.5 V
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	4.7			Ω typ	Source voltage (V_S) = ±4.5 V, source current (I_S) = −10 mA, see Figure 22
	5.2	7.2	8.2	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.12			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.2			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.5	1.9	2.1	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off, I_S (Off)	±0.01			nA typ	V_S = +4.5 V to −4.5 V , drain voltage (V_D) = −4.5 V to +4.5 V, see Figure 23
	±0.15	±1.5	±12	nA max	
Drain Off, I_D (Off)	±0.02			nA typ	V_S = +4.5 V to −4.5 V V_D = −4.5 V to +4.5 V, see Figure 23
	±0.15	±2	±20	nA max	
Drain Channel On, I_D (On), Source Channel On, I_S (On)	±0.02			nA typ	V_S = +4.5 V to −4.5 V, V_D = −4.5 V to +4.5 V, see Figure 24
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	
Input Low Voltage, V_{INL}			0.35 × V_L	V max	
Input High Current, I_{INH}	55			μA typ	INx voltage (V_{INx}) = V_L = 1.8 V, see the Theory of Operations section
			90	μA max	
	40			μA typ	V_{INx} = V_L = 1.2 V, see the Theory of Operations section
			65	μA max	
Input Low Current, I_{INL}	0.2			μA typ	V_{INx} = 0 V
			0.8	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	

SPECIFICATIONS

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS					
Transition Time, $t_{TRANSITION}$	174			ns typ	Load resistance (R_L) = 300 Ω, load capacitance (C_L) = 35 pF
	220	251	271	ns max	V_S = 2.5 V, see Figure 25
Enable Delay On Time, t_{ON} (EN)	161			ns typ	R_L = 300 Ω, C_L = 35 pF
	201	224	241	ns max	V_S = 2.5 V, see Figure 27
Enable Delay Off Time, t_{OFF} (EN)	190			ns typ	R_L = 300 Ω, C_L = 35 pF
	241	266	288	ns max	V_S = 2.5 V, see Figure 27
Break-Before-Make Time Delay, t_{BBM}	43			ns typ	R_L = 300 Ω, C_L = 35 pF
			29	ns min	S1x voltage (V_{S1x}) = S2x voltage (V_{S2x}) = 2.5 V, see Figure 26
Charge Injection, Q_{INJ}	−12.5			pC typ	V_S = 0 V, source resistance (R_S) = 0 Ω, C_L = 1 nF, see Figure 28
Off Isolation	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 29
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 31
Total Harmonic Distortion, THD	−102			dB typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 1 kHz to 20 kHz, Figure 20
	−95			dB typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 100 kHz, Figure 20
Total Harmonic Distortion Plus Noise, THD + N	0.002			% typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 100 kHz, see Figure 32
−3 dB Bandwidth	77			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 30
Insertion Loss	0.26			dB typ	R_L = 50 Ω, C_L = 5 pF, see Figure 30
Source Off Capacitance, C_S (Off)	19			pF typ	V_S = 0 V, frequency = 1 MHz
Drain Off Capacitance, C_D (Off)	33			pF typ	V_S = 0 V, frequency = 1 MHz
Drain On Capacitance C_D (On), Source On Capacitance, C_S (On)	57			pF typ	V_S = 0 V, frequency = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Positive Supply Current (I_{DD})	50			μA typ	V_{INx} = 0 V or V_L
			90	μA max	
Negative Supply Current (I_{SS})	0.001			μA typ	V_{INx} = 0 V or V_L
			1	μA max	
Digital Supply Current (I_{VL})	45			μA typ	V_{INx} = V_L = 1.8 V
			70	μA max	
	30			μA typ	V_{INx} = V_L = 1.2 V
			55	μA max	

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, and V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	4.1			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA, see Figure 22
	4.6	6.6	7.6	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V

SPECIFICATIONS

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
On-Resistance Match Between Channels, ΔR_{ON}	0.12			Ω typ	V_S = 10 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1.3	1.7	2	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off, I_S (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 23
	±0.15	±1.5	±12	nA max	
Drain Off, I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 23
	±0.15	±2	±20	nA max	
Drain Channel On, I_D (On), Source Channel On, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 10 V, see Figure 24
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	
Input Low Voltage, V_{INL}			0.35 × V_L	V max	
Input High Current, I_{INH}	55			µA typ	V_{INx} = V_L = 1.8 V, see the Theory of Operations section
			90	µA max	
	40			µA typ	V_{INx} = V_L = 1.2 V, see the Theory of Operations section
			65	µA max	
Input Low Current, I_{INL}	0.2			µA typ	V_{INx} = 0 V
			0.8	µA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time, $t_{TRANSITION}$	145			ns typ	R_L = 300 Ω, C_L = 35 pF
	185	208	231	ns max	V_S = 8 V, see Figure 25
Enable Delay On Time, t_{ON} (EN)	127			ns typ	R_L = 300 Ω, C_L = 35 pF
	154	166	177	ns max	V_S = 8 V, see Figure 27
Enable Delay Off Time, t_{OFF} (EN)	159			ns typ	R_L = 300 Ω, C_L = 35 pF
	195	218	241	ns max	V_S = 8 V, see Figure 27
Break-Before-Make Time Delay, t_{BBM}	44			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 8 V, see Figure 26
Charge Injection, Q_{INJ}	−12.4			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 28
Off Isolation	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 29
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 31
Total Harmonic Distortion, THD	−99			dB typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 1 kHz to 20 kHz, see Figure 20
	−97			dB typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 100 kHz, see Figure 20
Total Harmonic Distortion Plus Noise, THD + N	0.0018			% typ	R_L = 10 kΩ, V_S = 5 V p-p, frequency = 100 kHz, see Figure 32
−3 dB Bandwidth	77			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 30
Insertion Loss	−0.21			dB typ	R_L = 50 Ω, C_L = 5 pF, see Figure 30
Source Off Capacitance, C_S (Off)	19			pF typ	V_S = 6 V, frequency = 1 MHz
Drain Off Capacitance, C_D (Off)	32			pF typ	V_S = 6 V, frequency = 1 MHz
Drain On Capacitance C_D (On), Source On Capacitance, C_S (On)	56			pF typ	V_S = 6 V, frequency = 1 MHz

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Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 12 V
Positive Current, I_{DD}	55			µA typ	V_{INx} = 0 V or V_{VL}
			95	µA max	
Digital Supply Current, I_{VL}	45			µA typ	V_{INx} = V_L = 1.8 V
			70	µA max	
	30			µA typ	V_{INx} = V_L = 1.2 V
			55	µA max	

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, and V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	8.5			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA, see Figure 22
	10	12.5	14	Ω max	V_{DD} = 4.5 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.15			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.3	0.35	0.4	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	2			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	2.6	3	3.3	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V, V_{SS} = 0 V
Source Off, I_S (Off)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, see Figure 23
	±0.15	±1.5	±12	nA max	
Drain Off, I_D (Off)	±0.02			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, see Figure 23
	±0.15	±2	±20	nA max	
Drain Channel On, I_D (On), Source Channel On, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 4.5 V, see Figure 24
	±0.15	±2	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	
Input Low Voltage, V_{INL}			0.35 × V_L	V max	
Input High Current, I_{INH}	55			µA typ	V_{INx} = V_L = 1.8 V, see the Theory of Operations section
			90	µA max	
	40			nA typ	V_{INx} = V_L = 1.2 V, see the Theory of Operations section
			65	µA max	
Input Low Current, I_{INL}	0.2			µA typ	V_{INx} = 0 V
			0.8	µA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time, $t_{TRANSITION}$	218			ns typ	R_L = 300 Ω, C_L = 35 pF
	274	314	342	ns max	V_S = 2.5 V, see Figure 25
Enable Delay On Time, t_{ON} (EN)	190			ns typ	R_L = 300 Ω, C_L = 35 pF
	247	273	294	ns max	V_S = 2.5 V, see Figure 27
Enable Delay Off Time, t_{OFF} (EN)	220			ns typ	R_L = 300 Ω, C_L = 35 pF
	271	308	336	ns max	V_S = 2.5 V, see Figure 27

SPECIFICATIONS

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Break-Before-Make Time Delay, t_{BBM}	55			ns typ	R_L = 300 Ω, C_L = 35 pF
			36	ns min	V_{S1} = V_{S2} = 2.5 V, see Figure 26
Charge Injection, Q_{INJ}	−5			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF, see Figure 28
Off Isolation	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 29
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 31
Total Harmonic Distortion (THD)	−83			dB typ	R_L = 10 kΩ, frequency = 1 kHz to 20 kHz, V_S = 3.5 V p-p, see Figure 20
	−80			dB typ	R_L = 10 kΩ, frequency = 100 kHz, V_S = 3.5 V p-p, see Figure 20
Total Harmonic Distortion Plus Noise (THD + N)	0.011			% typ	R_L = 10 kΩ, frequency = 100 kHz, V_S = 3.5 V p-p, see Figure 32
−3 dB Bandwidth	77			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 30
Insertion Loss	−0.44			dB typ	R_L = 50 Ω, C_L = 5 pF, see Figure 30
Source Off Capacitance, C_S (Off)	21			pF typ	V_S = 2.5 V, frequency = 1 MHz
Drain Off Capacitance, C_D (Off)	37			pF typ	V_S = 2.5 V, frequency = 1 MHz
Drain On Capacitance, C_D (On), Source On Capacitance, C_S (On)	62			pF typ	V_S = 2.5 V, frequency = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V, V_{SS} = 0 V
Positive Current, I_{DD}	50			μA typ	V_{INx} = V_L = 0 V
			90	μA max	
Digital Supply Current, I_{VL}	45			μA typ	V_{INx} = V_L = 1.8 V
			70	μA max	
	30			μA typ	V_{INx} = V_L = 1.2 V
			55	μA max	

3.3 V SINGLE SUPPLY

V_{DD} = 3.3 V, V_{SS} = 0 V, GND = 0 V, and V_L = 1.1 V to 1.95 V, unless otherwise noted.

Table 5.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	13.5	15	16.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA, see Figure 22, V_{DD} = 3.3 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.25	0.28	0.3	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
On-Resistance Flatness, $R_{FLAT(ON)}$	5	5.5	6.5	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V, V_{SS} = 0 V
Source Off, I_S (Off)	±0.01			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V, see Figure 23
	±0.15	±1.5	±12	nA max	
Drain Off, I_D (Off)	±0.02			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V, see Figure 23
	±0.15	±2	±20	nA max	
Drain Channel On, I_D (On), Source Channel On, I_S (On)	±0.02			nA typ	V_S = V_D = 0.6 V or 3 V, see Figure 24
	±0.15	±2	±20	nA max	

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Table 5.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	
Input Low Voltage, V_{INL}			0.35 × V_L	V max	
Input High Current, I_{INH}	55			µA typ	V_{INx} = V_L = 1.8 V, see the Theory of Operations section
			90	µA max	
	40			nA typ	V_{INx} = V_L = 1.2 V, see the Theory of Operations section
			65	µA max	
Input Low Current, I_{INL}	0.2			µA typ	V_{INx} = 0 V
			0.8	µA max	
Digital Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time, $t_{TRANSITION}$	300			ns typ	R_L = 300 Ω, C_L = 35 pF
	397	449	477	ns max	V_S = 1.5 V, see Figure 25
Enable Delay On Time, t_{ON} (EN)	307			ns typ	R_L = 300 Ω, C_L = 35 pF
	420	437	495	ns max	V_S = 1.5 V, see Figure 27
Enable Delay Off Time, t_{OFF} (EN)	293			ns typ	R_L = 300 Ω, C_L = 35 pF
	337	414	443	ns max	V_S = 1.5 V, see Figure 27
Break-Before-Make Time Delay, t_{BBM}	78			ns typ	R_L = 300 Ω, C_L = 35 pF
			51	ns min	V_{S1} = V_{S2} = 1.5 V, see Figure 26
Charge Injection, Q_{INJ}	−10			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF, see Figure 28
Off Isolation	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 29
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency = 1 MHz, see Figure 31
Total Harmonic Distortion, THD	−77			% typ	R_L = 10 kΩ, frequency = 1 kHz to 20 kHz, V_S = 2 V p-p, see Figure 20
	−76			% typ	R_L = 10 kΩ, frequency = 100 kHz, V_S = 2 V p-p, see Figure 20
Total Harmonic Distortion Plus Noise, THD + N	0.016			% typ	R_L = 10 kΩ, frequency = 100 kHz, V_S = 2 V p-p, see Figure 32
−3 dB Bandwidth	83			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 30
Insertion Loss	−1.15			dB typ	R_L = 50 Ω, C_L = 5 pF, see Figure 30
Source Off Capacitance, C_S (Off)	22			pF typ	V_S = 1.5 V, frequency = 1 MHz
Drain Off Capacitance, C_D (Off)	39			pF typ	V_S = 1.5 V, frequency = 1 MHz
Drain On Capacitance, C_D (On), Source On Capacitance, C_S (On)	64			pF typ	V_S = 1.5 V, frequency = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V
Positive Current, I_{DD}	45			µA typ	V_{INx} = V_L = 0 V
			90	µA max	
Digital Supply Current, I_{VL}	45			µA typ	V_{INx} = V_L = 1.8 V
			75	µA max	
	30			µA typ	V_{INx} = V_L = 1.2 V
			55	µA max	

SPECIFICATIONS

CONTINUOUS CURRENT PER CHANNEL, SxA, SxB, OR Dx

Table 6. Four Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, SxA, SxB, OR Dx[1] (θ_{JA} = 49.18°C/W)				
V_{DD} = +5 V, V_{SS} = −5 V	186	118	69	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V	197	123	70	mA maximum
V_{DD} = 5 V, V_{SS} = 0 V	143	96	60	mA maximum
V_{DD} = 3.3 V, V_{SS} = 0 V	118	82	54	mA maximum

[1] SxA and SxB refer to the S1A to S4A pins and the S1B to S4B pins, and Dx refers to the D1 to D4 pins.

Table 7. One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, SxA, SxB, OR Dx[1] (θ_{JA} = 49.18°C/W)				
V_{DD} = +5 V, V_{SS} = −5 V	340	184	85	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V	359	191	86	mA maximum
V_{DD} = 5 V, V_{SS} = 0 V	262	154	79	mA maximum
V_{DD} = 3.3 V, V_{SS} = 0 V	215	133	74	mA maximum

[1] SxA and SxB refer to the S1A to S4A pins and the S1B to S4B pins, and Dx refers to the D1 to D4 pins.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −18 V
V_L to GND	−0.3 V to +2.25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[2]	GND − 0.3 V to 2.25 V or 30 mA, whichever occurs first
Peak Current, SxA, SxB or Dx[3]	317 mA (pulsed at 1 ms, 10% duty-cycle maximum)
Continuous Current, SxA, SxB, or Dx Pins[4]	Data + 15%
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb free	260°C

[1] Overvoltages at the SxA, SxB, and Dx analog input pins are clamped by internal diodes. Limit the current to the maximum ratings given.

[2] Overvoltages at the INx digital input pins are clamped by internal diodes.

[3] SxA and SxB refers to the S1A to S4A pins and the S1B to S4B, and Dx refers to the D1 to D4 pins.

[4] See Table 6 and Table 7.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction-to-case thermal resistance.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-17[1]	49.18	9.35	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADG1634L

Table 10. ADG1634L, 24-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±3000	2
FICDM	±1250	C3

[1] For the input and output port to the supplies, the input and output port to the input and output port, and all other inputs.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

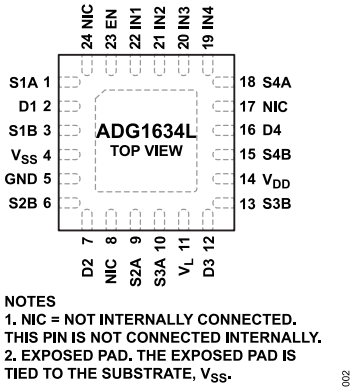

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1A	Source Terminal 1A. S1A can be an input or an output.
2	D1	Drain Terminal 1. D1 can be an input or an output.
3	S1B	Source Terminal 1B. S1B can be an input or an output.
4	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, the V_{SS} pin can be connected to ground.
5	GND	Ground (0 V) Reference.
6	S2B	Source Terminal 2B. S2B can be an input or an output.
7	D2	Drain Terminal 2. D2 can be an input or an output.
8, 17, 24	NIC	Not Internally Connected. This pin is not connected internally.
9	S2A	Source Terminal 2A. S2A can be an input or an output.
10	S3A	Source Terminal 3A. S3A can be an input or an output.
11	V_L	Logic Control Power Supply Potential.
12	D3	Drain Terminal 3. D3 can be an input or an output.
13	S3B	Source Terminal 3B. S3B can be an input or an output.
14	V_{DD}	Most Positive Power Supply Potential.
15	S4B	Source Terminal 4B. S4B can be an input or an output.
16	D4	Drain Terminal 4. D4 can be an input or an output.
18	S4A	Source Terminal 4A. S4A can be an input or an output.
19	IN4	Logic Control Input 4.
20	IN3	Logic Control Input 3.
21	IN2	Logic Control Input 2.
22	IN1	Logic Control Input 1.
23	EN	Active High Digital Input. When the EN pin is low, the device is disabled, and all switches are off. When the EN pin is high, the INx logic inputs determine the on switches.
Not applicable	EPAD	Exposed Pad. The exposed pad is tied to the substrate, V_{SS}.

Table 12. Truth Table

EN	INx	SxA	SxB
0	Don't care	Off	Off
1	0	Off	On
1	1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

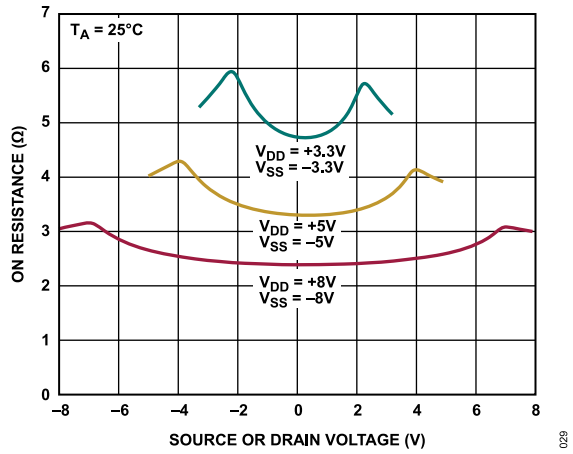

Figure 3. On Resistance vs. V_D (V_S), Dual Supply

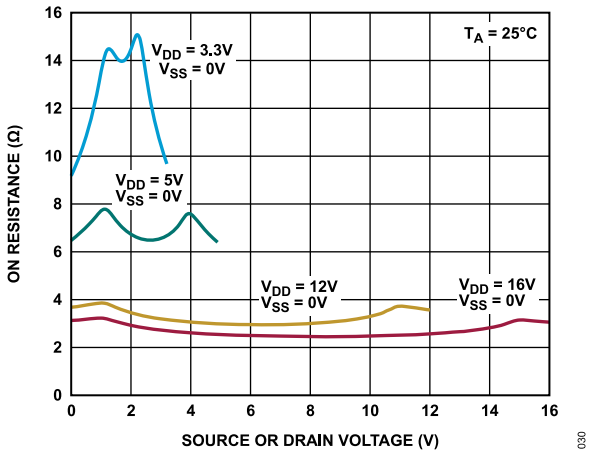

Figure 4. On Resistance vs. V_D (V_S), Single Supply

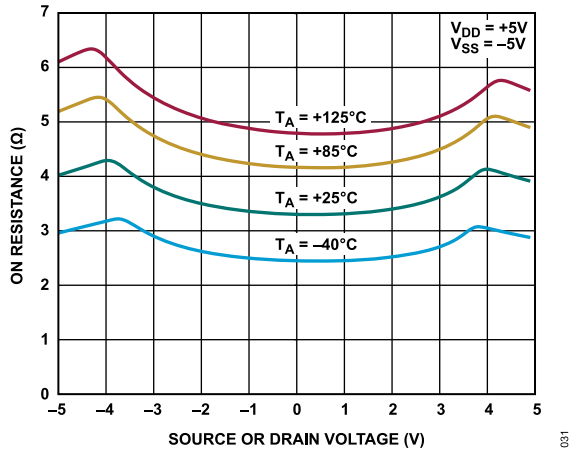

Figure 5. On Resistance vs. V_D (V_S) for Different Temperatures, ±5 V Dual Supply

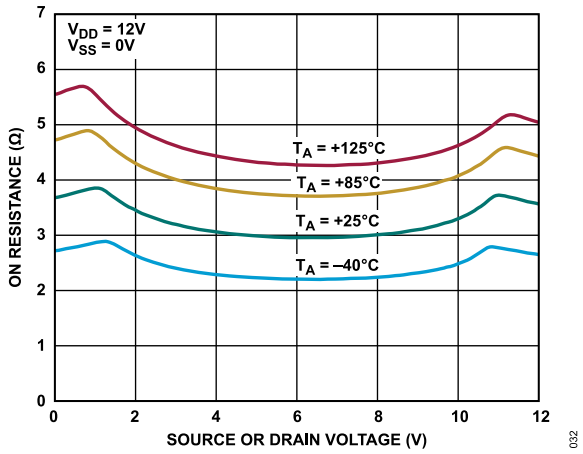

Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures, 12 V Single Supply

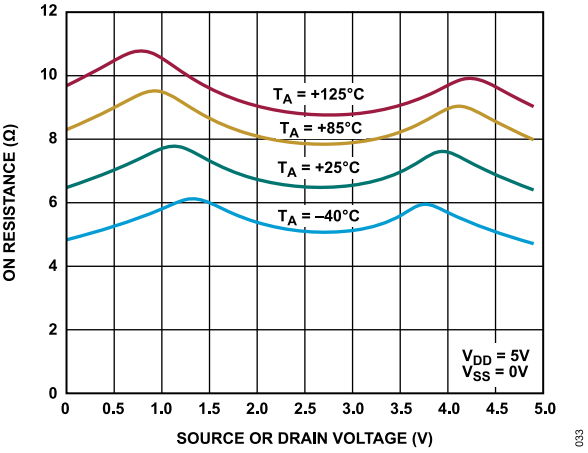

Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures, 5 V Single Supply

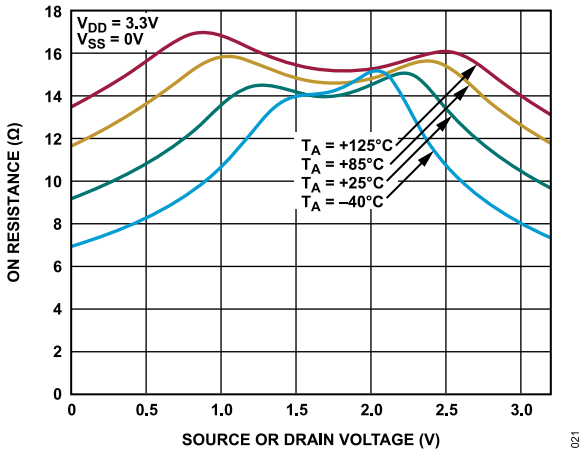

Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures, 3.3 V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

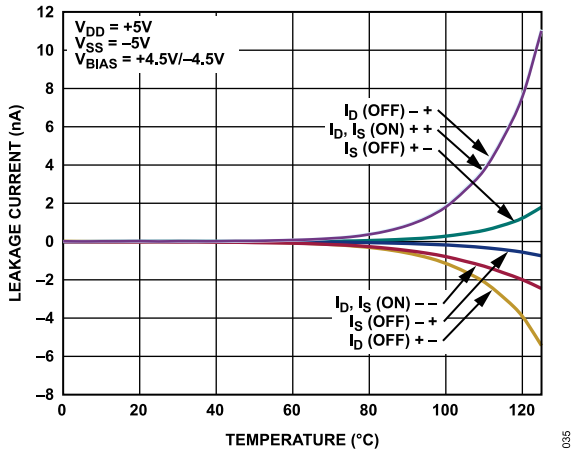

Figure 9. Leakage Current vs. Temperature, ±5 V Dual Supply

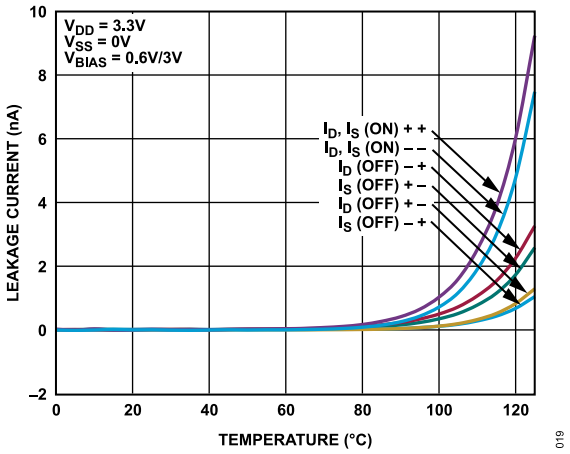

Figure 12. Leakage Current vs. Temperature, 3.3 V Single Supply

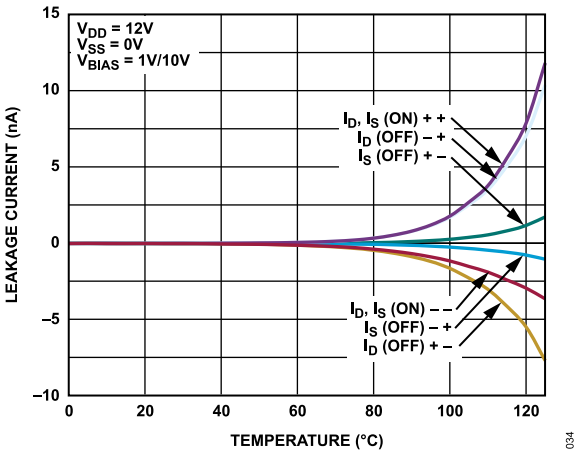

Figure 10. Leakage Current vs. Temperature, 12 V Single Supply

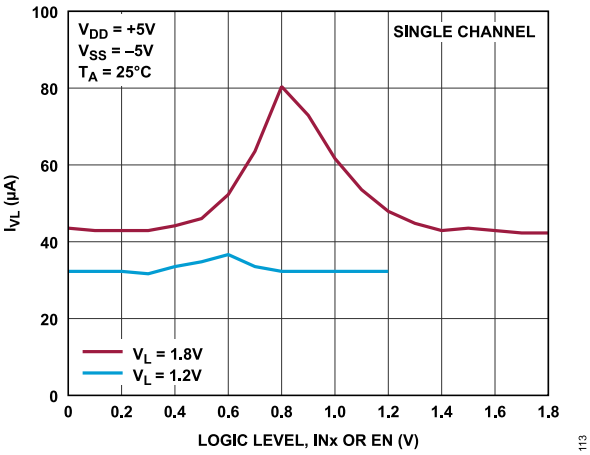

Figure 13. I_{VL} vs. Logic Level, INx or EN

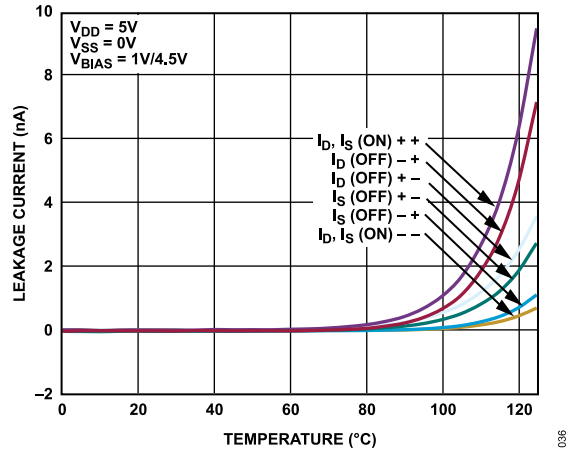

Figure 11. Leakage Current vs. Temperature, 5 V Single Supply

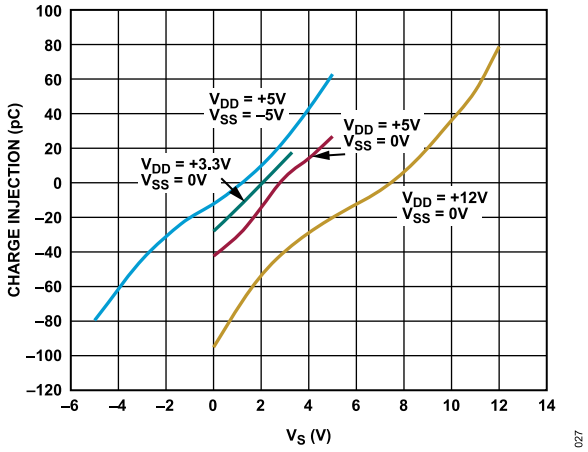

Figure 14. Charge Injection vs. V_S

TYPICAL PERFORMANCE CHARACTERISTICS

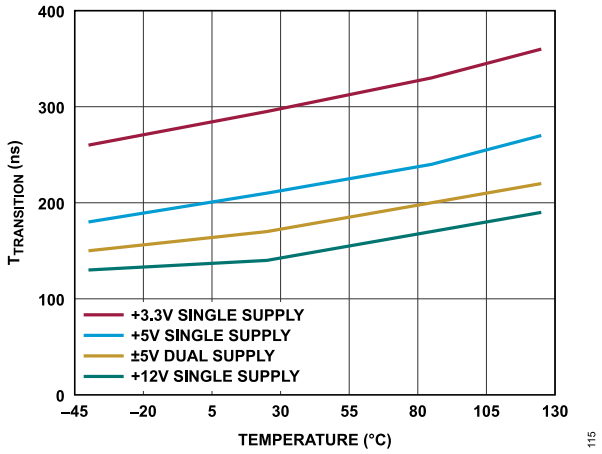

Figure 15. $T_{TRANSITION}$ vs. Temperature

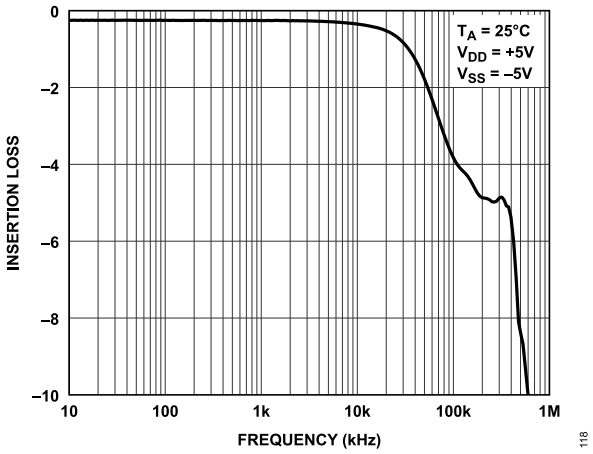

Figure 18. Insertion Loss vs. Frequency

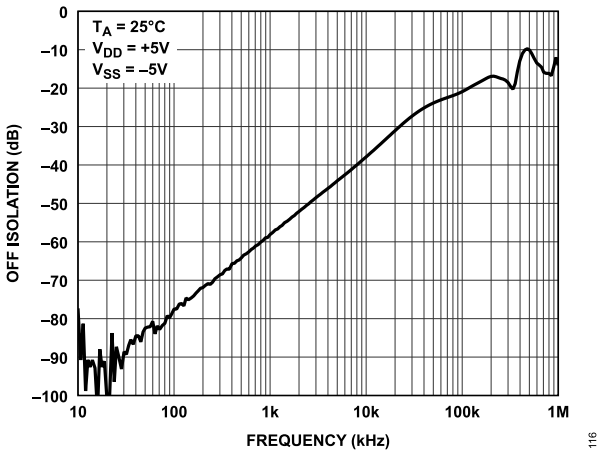

Figure 16. Off Isolation vs. Frequency

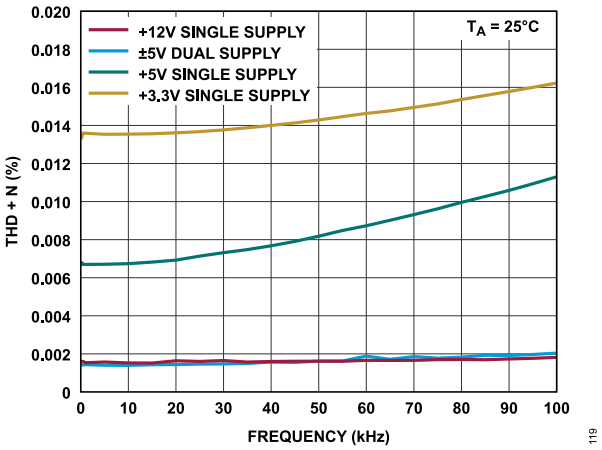

Figure 19. THD + N vs. Frequency

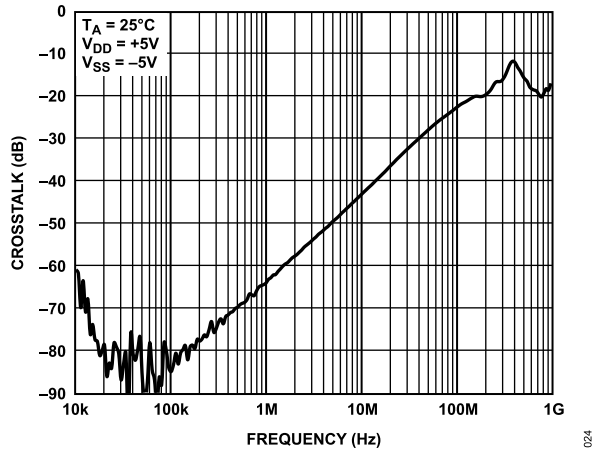

Figure 17. Crosstalk vs. Frequency

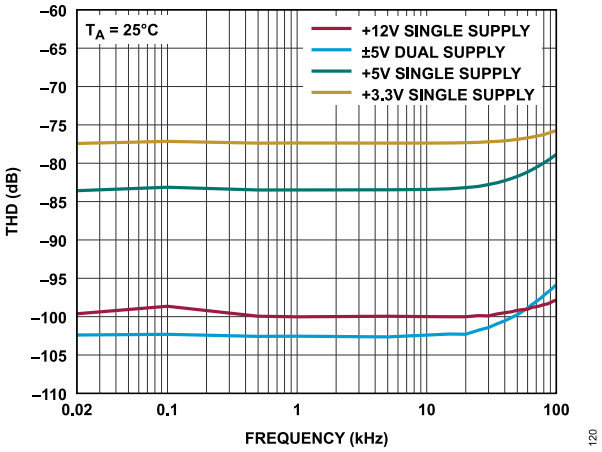

Figure 20. THD vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

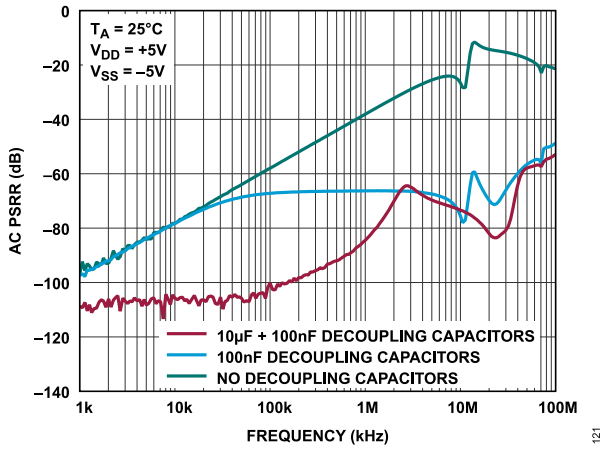

Figure 21. AC PSRR vs. Frequency

TEST CIRCUITS

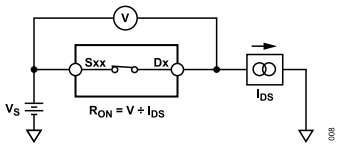

Figure 22. On Resistance

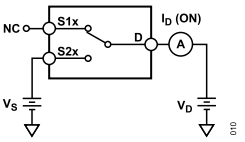

Figure 24. On Leakage

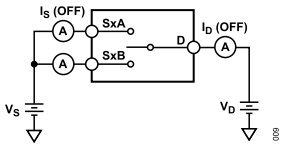

Figure 23. Off Leakage

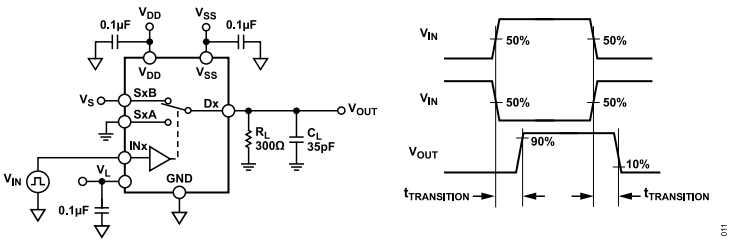

Figure 25. Transition Time, $t_{TRANSITION}$ (V_{IN} Is the Input Voltage, and V_{OUT} Is the Output Voltage.)

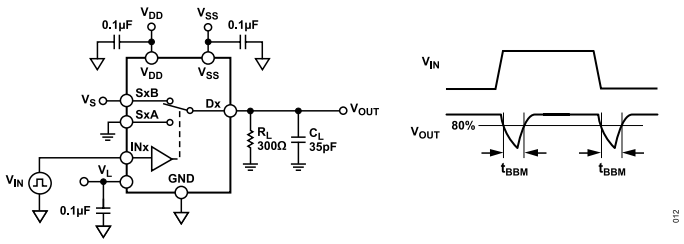

Figure 26. Break-Before-Make Delay, t_{BBM}

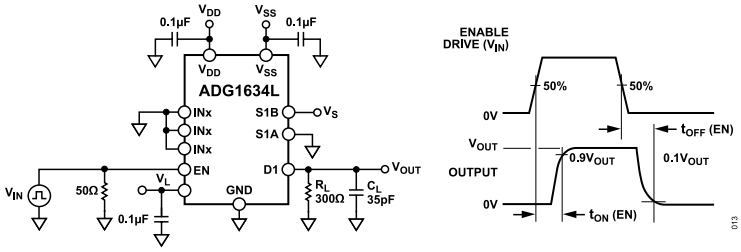

Figure 27. Enable Delay On Time, t_{ON} (EN) and Enable Delay Off Time, t_{OFF} (EN)

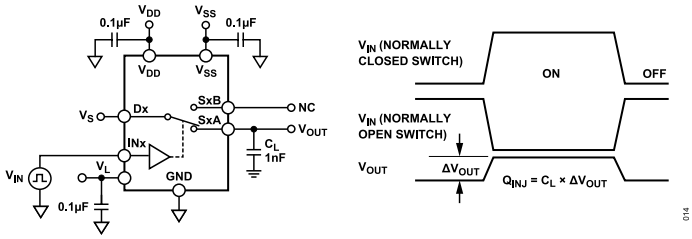

Figure 28. Charge Injection

TEST CIRCUITS

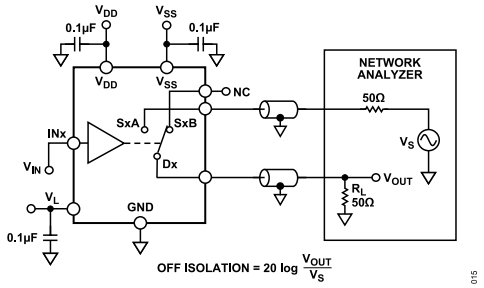

Figure 29. Off Isolation

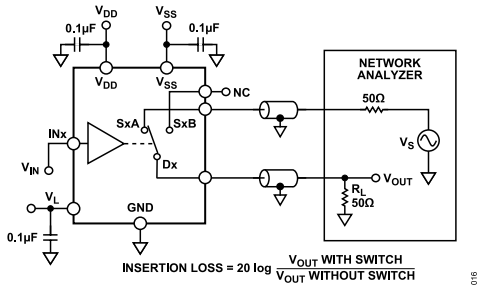

Figure 30. Bandwidth

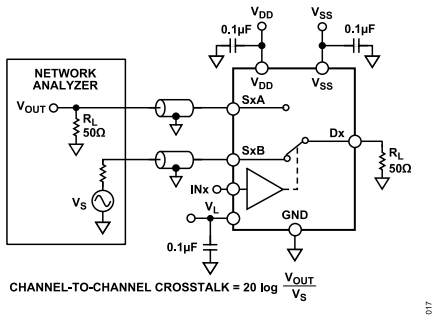

Figure 31. Channel-to-Channel Crosstalk

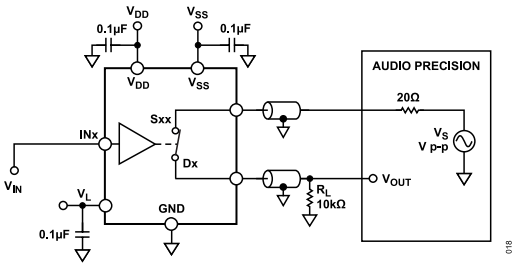

Figure 32. THD + Noise

TERMINOLOGY

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

The difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of the on resistance measured.

I_S Off

Source leakage current when the switch is off.

I_D Off

Drain leakage current when the switch is off.

I_D (On) and I_S (On)

Channel drain and source leakage currents when the switch is on.

V_D and V_S

Analog voltages on Terminal D and Terminal S.

C_S (Off) and C_D (Off)

Channel source and drain capacitance for off condition.

C_D (On) and C_S (On)

On switch drain and source capacitance.

C_{IN}

Digital input capacitance.

t_{ON} (EN)

Enable delay on time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

Enable delay off time between the 50% and 10% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}

Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INH}

Input high current of the digital input.

I_{INL}

Input low current of the digital input.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

I_{VL}

The digital supply current.

Off Isolation

A measure of unwanted signal coupling through an off channel.

Channel-to-Channel Crosstalk

A measure of unwanted signal coupling through an off switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion (THD)

THD is the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

Total Harmonic Distortion Plus Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)

A measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.115 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the AC PSRR.

THEORY OF OPERATIONS

SWITCH ARCHITECTURE

The ADG1634L is a set of low logic controlled, quad SPDT switches that are compatible with 1.2 V or 1.8 V logic depending on the V_L input.

V_L FLEXIBILITY

An external V_L supply provides flexibility for lower logic levels. The following V_L conditions must be satisfied for the switch to operate in either 1.2 V or 1.8 V logic operation:

- V_L = 1.1 V to 1.3 V for 1.2 V logic
- V_L = 1.65 V to 1.95 V for 1.8 V logic

1.2 V AND 1.8 V JEDEC COMPLIANCE

The ADG1634L is both 1.2 V and 1.8 V JEDEC standard compliant (normal range) to the digital input threshold. This compliance with the digital input threshold ensures low voltage CMOS logic compatibility when operating with a valid logic power supply range.

Note that the switch digital input requirement for both the 1.2 V and 1.8 V logic levels are the following:

- $V_{INH} = 0.65 \times V_L$
- $V_{INL} = 0.35 \times V_L$

INITIALIZATION TIME

The digital section of the ADG1634L goes through an initialization phase during V_{DD}, V_{SS}, and V_L power-up. After V_{DD}, V_{SS}, and V_L power up, ensure that a minimum of 50 µs has passed and that V_{DD}, V_{SS}, and V_L do not drop before issuing an INx input.

SWITCHES IN A KNOWN STATE

The switches within the ADG1634L are off when the INx pins are floating, which prevents unwanted signals from passing through these switches. This built-in feature of the ADG1634L eliminates the need to install an external pull-down resistor. The ADG1634L can pull down the floating INx inputs against the leakage currents up to half of the I_{INH}.

APPLICATIONS INFORMATION

FIELD PROGRAMMABLE GRID ARRAY (FPGA) LOW LOGIC COMPLIANCE

Figure 33 shows a typical application where the ADG1634L is used together with an FPGA or microcontroller. The flexible V_L pin can be tied to the digital supply voltage (V_{CCO}), and the INx input can be tied directly to the digital IOx ports for ease of use.

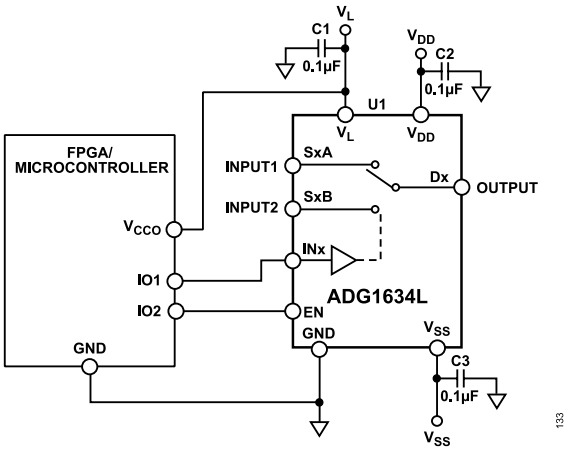

Figure 33. Typical Application

The ADG1634L is 1.2 V and 1.8 V JEDEC standard compliant, which ensures that the logic input specifications, V_{INH} and V_{INL}, meet the digital output specifications, minimum V_{OH} and maximum V_{OL}, of the FPGA or microcontroller. Common implementations do not guarantee logic level compatibility, which can introduce implementation risks. The ADG1634L eliminates these risks by complying with the widely accepted 1.2 V and 1.8 V logic level standard.

V_{OH} AND V_{OL} AND V_{INH} AND V_{INL} RELATIONSHIP

It is recommended to confirm that the logic output high, V_{OH}, of the FPGA or microcontroller is higher than the input logic high, V_{INH}. In addition, the logic output low, V_{OL}, of the FPGA or microcontroller must be lower than the input low, V_{INL}.

Figure 34 shows the 1.2 V logic compatibility relationship between V_{OH} and V_{OL} of the FPGA or the microcontroller with the INx inputs of the ADG1634L, V_{INH} and V_{INL}.

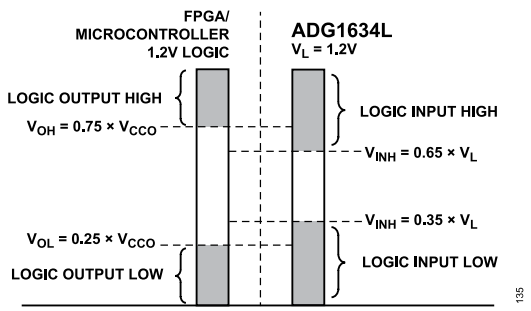

Figure 34. 1.2 V Logic Compatibility Between V_{OH} and V_{OL} and V_{INH} and V_{INL}

Figure 35 shows the 1.8 V logic compatibility relationship between V_{OH} and V_{OL} of the FPGA or the microcontroller with the INx inputs of the ADG1634L, V_{INH} and V_{INL}.

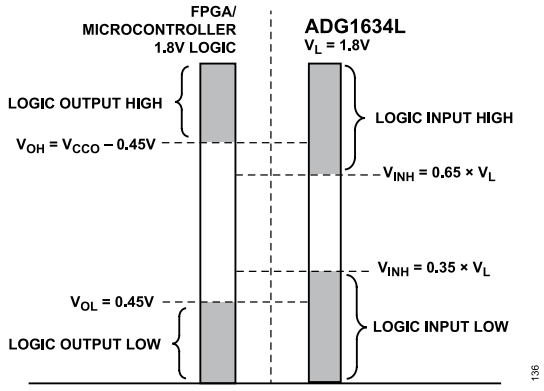

Figure 35. 1.8 V Logic Compatibility Between V_{OH} and V_{OL} and V_{INH} and V_{INL}

POWER SUPPLY RAILS

To guarantee correct operation of the ADG1634L, a minimum of 0.1 µF and 10 µF decoupling capacitors are required on the V_{DD}, V_{SS}, and V_L supply pins.

The ADG1634L can operate with V_{DD} and V_{SS} dual supplies between ±3.3 V to ±8 V. This device can also operate with a V_{DD} single supply between 3.3 V to 16 V and a V_L of between 1.1 V to 1.95 V. However, the V_{DD} to V_{SS} range must not exceed 18 V, and the V_L range must not exceed 2.25 V, as stated in the Absolute Maximum Ratings section.

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a symmetrical bipolar power solution is shown in Figure 36. The ADP5070 (dual switching regulator) generates a positive and negative supply rail for the ADG1634L. Also shown in Figure 36 are two optional positive and negative, low dropout (LDO) regulators, the ADP7118 and ADP7182, respectively, that can reduce the output ripple of the ADP5070 in ultralow noise sensitive applications.

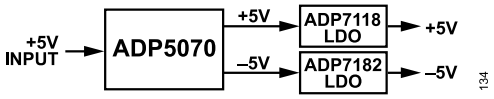

Figure 36. Bipolar Power Solution

OUTLINE DIMENSIONS

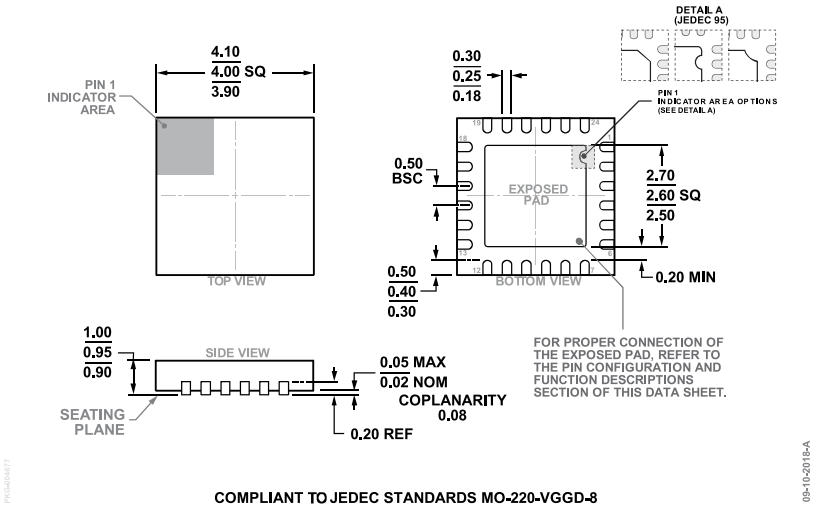

Figure 37. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.95 mm Package Height
(CP-24-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Package Quantity
ADG1634LYCPZ-REEL7	−40°C to +125°C	24-Lead LFCSP	CP-24-17	Reel, 1500

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADG1634LEBZ	Evaluation Board

[1] Z = RoHS Compliant Part.