Single 12-/10-/8-Bit Rail-to- Rail DACs with 10ppm/°C Reference in SC70

FEATURES

- **Integrated Precision Reference**
  2.5V Full Scale 10ppm/°C (LTC2630-L)
  4.096V Full Scale 10ppm/°C (LTC2630-H)
- **Maximum INL Error: 1 LSB (LTC2630A-12)**
- **Low Noise: 0.7mV$_{P-P}$, 0.1Hz to 200kHz**
- Guaranteed Monotonic over Temperature
- Selectable Internal Reference or Supply as Reference
- 2.7V to 5.5V Supply Range (LTC2630-L)
- Low Power Operation: 180µA at 3V
- Power Down to 1.8µA Maximum (C and I Grades)
- Power-on Reset to Zero or Mid-Scale Options
- SPI Serial Interface
- Double-Buffered Data Latches
- Tiny 6-Lead SC70 Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Automatic Test Equipment
- Portable Equipment
- Automotive

DESCRIPTION

The LTC®2630 is a family of 12-, 10-, and 8-bit voltage-output DACs with an integrated, high-accuracy, low-drift reference in a 6-lead SC70 package. It has a rail-to-rail output buffer and is guaranteed monotonic.

The LTC2630-L has a full-scale output of 2.5V, and operates from a single 2.7V to 5.5V supply. The LTC2630-H has a full-scale output of 4.096V, and operates from a 4.5V to 5.5V supply. Each DAC can also operate in supply as reference mode, which sets the full-scale output to the supply voltage.

The parts use a simple SPI/MICROWIRE™ compatible 3-wire serial interface which operates at clock rates up to 50MHz.

The LTC2630 incorporates a power-on reset circuit. Options are available for reset to zero or reset to mid-scale after power-up.

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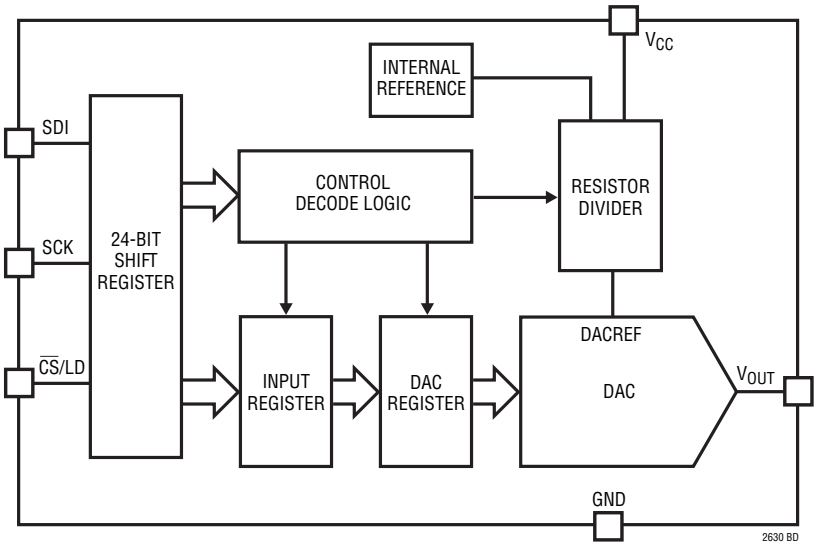
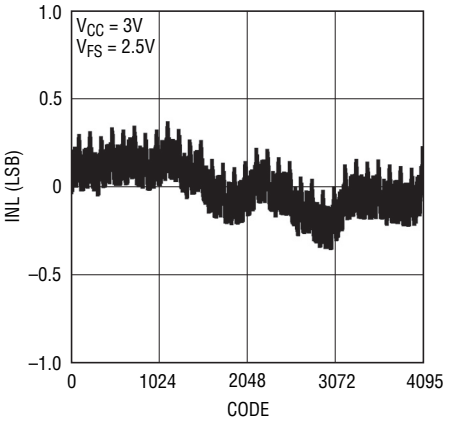
BLOCK DIAGRAM



Integral Nonlinearity (LTC2630A-LZ12)



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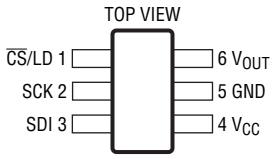
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 6V
$\overline{CS}$/LD, SCK, SDI ..... –0.3V to 6V
V_{OUT} ..... –0.3V to min(V_{CC} + 0.3V, 6V)
Operating Temperature Range
LTC2630C ..... 0°C to 70°C
LTC2630I ..... –40°C to 85°C
LTC2630H ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



SC6 PACKAGE
6-LEAD PLASTIC SC70

T_{JMAX} = 150°C (Note 5), θ_{JA} = 300°C/W

ORDER INFORMATION

http://www.linear.com/product/LTC2630#orderinfo

LTC2630 A C SC6 –L M 12 #TRM PBF

LEAD FREE DESIGNATOR

TAPE AND REEL
TR = 2,500-Piece Tape and Reel
TRM = 500-Piece Tape and Reel

RESOLUTION
12 = 12-Bit
10 = 10-Bit
8 = 8-Bit

POWER-ON RESET
M = Reset to Mid-Scale
Z = Reset to Zero-Scale

FULL-SCALE VOLTAGE, INTERNAL REFERENCE MODE
L = 2.5V
H = 4.096V

PACKAGE TYPE
SC6 = 6-Lead SC70

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)
H = Automotive Temperature Range (–40°C to 125°C)

ELECTRICAL GRADE (OPTIONAL)
A = ±1 LSB Maximum INL (12-Bit)

PRODUCT PART NUMBER

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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PRODUCT SELECTION GUIDE

PART NUMBER	PART MARKING*	V_{FS} WITH INTERNAL REFERENCE	POWER-ON RESET TO CODE	RESOLUTION	V_{CC}	MAXIMUM INL
LTC2630A-LM12	LCZB	2.5V • (4095/4096)	Mid-Scale	12-Bit	2.7V–5.5V	±1LSB
LTC2630A-LZ12	LCSB	2.5V • (4095/4096)	Zero	12-Bit	2.7V–5.5V	±1LSB
LTC2630A-HM12	LCWR	4.096V • (4095/4096)	Mid-Scale	12-Bit	4.5V–5.5V	±1LSB
LTC2630A-HZ12	LCZC	4.096V • (4095/4096)	Zero	12-Bit	4.5V–5.5V	±1LSB
LTC2630-LM12	LCZB	2.5V • (4095/4096)	Mid-Scale	12-Bit	2.7V–5.5V	±2LSB
LTC2630-LM10	LCZF	2.5V • (1023/1024)	Mid-Scale	10-Bit	2.7V–5.5V	±1LSB
LTC2630-LM8	LCYW	2.5V • (255/256)	Mid-Scale	8-Bit	2.7V–5.5V	±0.5LSB
LTC2630-LZ12	LCSB	2.5V • (4095/4096)	Zero	12-Bit	2.7V–5.5V	±2LSB
LTC2630-LZ10	LCZD	2.5V • (1023/1024)	Zero	10-Bit	2.7V–5.5V	±1LSB
LTC2630-LZ8	LCYV	2.5V • (255/256)	Zero	8-Bit	2.7V–5.5V	±0.5LSB
LTC2630-HM12	LCWR	4.096V • (4095/4096)	Mid-Scale	12-Bit	4.5V–5.5V	±2LSB
LTC2630-HM10	LCZH	4.096V • (1023/1024)	Mid-Scale	10-Bit	4.5V–5.5V	±1LSB
LTC2630-HM8	LCYY	4.096V • (255/256)	Mid-Scale	8-Bit	4.5V–5.5V	±0.5LSB
LTC2630-HZ12	LCZC	4.096V • (4095/4096)	Zero	12-Bit	4.5V–5.5V	±2LSB
LTC2630-HZ10	LCZG	4.096V • (1023/1024)	Zero	10-Bit	4.5V–5.5V	±1LSB
LTC2630-HZ8	LCYX	4.096V • (255/256)	Zero	8-Bit	4.5V–5.5V	±0.5LSB

*The temperature grade is identified by a label on the shipping container.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2630-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2630A-LM12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		LTC2630-8 MIN	LTC2630-8 TYP	LTC2630-8 MAX	LTC2630-10 MIN	LTC2630-10 TYP	LTC2630-10 MAX	LTC2630-12 MIN	LTC2630-12 TYP	LTC2630-12 MAX	LTC2630A-12 MIN	LTC2630A-12 TYP	LTC2630A-12 MAX	UNITS
DC Performance																
	Resolution		●	8			10			12			12			Bits
	Monotonicity	V_{CC} = 3V, Internal Ref. (Note 3)	●	8			10			12			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 3)	●			±0.5			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 3)	●		±0.05	±0.5		±0.2	±1		±1	±2		±0.5	±1	LSB
ZSE	Zero Scale Error	V_{CC} = 3V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 3V, Internal Ref. (Note 4)	●		±0.5	±5		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 3V, Internal Ref. (Note 4)			±10			±10			±10			±10		µV/°C
FSE	Full Scale Error	V_{CC} = 3V, Internal Ref.	●		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8	%FSR
V_{FSTC}	Full Scale Voltage Temperature Coefficient	V_{CC} = 3V, Internal Ref. (Note 9) C-Grade I-Grade H-Grade			 ±10 ±10 ±10			 ±10 ±10 ±10			 ±10 ±10 ±10			 ±10 ±10 ±10		 ppm/°C ppm/°C ppm/°C
	Load Regulation	Internal Ref., Mid-Scale, V_{CC} = 3V ±10%, –5mA ≤ I_{OUT} ≤ 5mA V_{CC} = 5V ±10%, –10mA ≤ I_{OUT} ≤ 10mA	 ● ●		 0.008 0.008	 0.016 0.016		 0.03 0.03	 0.064 0.064		 0.13 0.13	 0.256 0.256		 0.13 0.13	 0.256 0.256	 LSB/mA LSB/mA
R_{OUT}	DC Output Impedance	Internal Ref., Mid-Scale, V_{CC} = 3V ±10%, –5mA ≤ I_{OUT} ≤ 5mA V_{CC} = 5V ±10%, –10mA ≤ I_{OUT} ≤ 10mA	 ● ●		 0.08 0.08	 0.156 0.156		 0.08 0.08	 0.156 0.156		 0.08 0.08	 0.156 0.156		 0.08 0.08	 0.156 0.156	 Ω Ω

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	Supply as Reference Internal Reference			0V to V_{CC} 0V to 2.5		V V
PSR	Power Supply Rejection	V_{CC} = 3V ±10% or 5V ±10%			–80		dB
I_{SC}	Short Circuit Output Current (Note 5) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero Scale; V_{OUT} Shorted to V_{CC} Full Scale; V_{OUT} Shorted to GND	 ● ●		 27 –28	 50 –50	 mA mA
Power Supply							
V_{CC}	Power Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current (Note 6)	V_{CC} = 3V, Supply as Reference V_{CC} = 3V, Internal Reference V_{CC} = 5V, Supply as Reference V_{CC} = 5V, Internal Reference	● ● ● ●		160 180 180 190	220 240 250 260	µA µA µA µA
I_{SD}	Supply Current in Power-Down Mode (Note 6)	V_{CC} = 5V, C-Grade, I-Grade V_{CC} = 5V, H-Grade	● ●		0.36 0.36	1.8 5	µA µA
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 3.6V to 5.5V V_{CC} = 2.7V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 4.5V	● ●			0.8 0.6	V V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 7)	●			2.5	pF

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2630-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2630A-LM12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
t_S	Settling Time	V_{CC} = 3V (Note 8) ±0.39% (±1LSB at 8 Bits) ±0.098% (±1LSB at 10 Bits) ±0.024% (±1LSB at 12 Bits)			 3.2 3.9 4.4		 µs µs µs
	Voltage Output Slew Rate				1.0		V/µs
	Capacitive Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			2		nV•s
e_n	Output Voltage Noise Density	At f = 1kHz, Supply as Reference At f = 10kHz, Supply as Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			140 130 160 150		nV/√Hz nV/√Hz nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz, Supply as Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, Supply as Reference 0.1Hz to 200kHz, Internal Reference			20 20 650 700		μV_{P-P} μV_{P-P} μV_{P-P} μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V. (See Figure 1) (Note 7).

LTC2630-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2630A-LM12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_1	SDI Valid to SCK Setup		●	4			ns
t_2	SDI Valid to SCK Hold		●	4			ns
t_3	SCK High Time		●	9			ns
t_4	SCK Low Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse width		●	10			ns
t_6	SCK High to $\overline{CS}$/LD High		●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2630-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2630A-HM12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		LTC2630-8 MIN	LTC2630-8 TYP	LTC2630-8 MAX	LTC2630-10 MIN	LTC2630-10 TYP	LTC2630-10 MAX	LTC2630-12 MIN	LTC2630-12 TYP	LTC2630-12 MAX	LTC2630A-12 MIN	LTC2630A-12 TYP	LTC2630A-12 MAX	UNITS
DC Performance																
	Resolution		●	8			10			12			12			Bits
	Monotonicity	V_{CC} = 5V, Internal Ref. (Note 3)	●	8			10			12			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 5V, Internal Ref. (Note 3)	●			±0.5			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 5V, Internal Ref. (Note 3)	●		±0.05	±0.5		±0.2	±1		±1	±2		±0.5	±1	LSB
ZSE	Zero Scale Error	V_{CC} = 5V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 5V, Internal Ref. (Note 4)	●		±0.5	±5		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 5V, Internal Ref. (Note 4)			±10			±10			±10			±10		µV/°C
FSE	Full Scale Error	V_{CC} = 5V, Internal Ref.	●		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8		±0.2	±0.8	%FSR
V_{FSTC}	Full Scale Voltage Temperature Coefficient	V_{CC} = 5V, Internal Ref. (Note 9) C-Grade I-Grade H-Grade			 ±10 ±10 ±10			 ±10 ±10 ±10			 ±10 ±10 ±10			 ±10 ±10 ±10		 ppm/°C ppm/°C ppm/°C
	Load Regulation	V_{CC} = 5V ±10%, Internal Ref., Mid-Scale, –10mA ≤ I_{OUT} ≤ 10mA	●		0.006	0.01		0.025	0.04		0.10	0.16		0.10	0.16	LSB/mA
R_{OUT}	DC Output Impedance	V_{CC} = 5V ±10%, Internal Ref., Mid-Scale, –10mA ≤ I_{OUT} ≤ 10mA	●		0.1	0.156		0.1	0.156		0.1	0.156		0.1	0.156	Ω

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	Supply as Reference Internal Reference			0V to V_{CC} 0V to 4.096		V V
PSR	Power Supply Rejection	V_{CC} = 5V ±10%			–80		dB
I_{SC}	Short Circuit Output Current (Note 5) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero Scale; V_{OUT} Shorted to V_{CC} Full Scale; V_{OUT} Shorted to GND	 ● ●		 27 –28	 50 –50	 mA mA
Power Supply							
V_{CC}	Power Supply Voltage	For Specified Performance	●	4.5		5.5	V
I_{CC}	Supply Current (Note 6)	V_{CC} = 5V, Supply as Reference V_{CC} = 5V, Internal Reference	● ●		180 200	260 280	µA µA
I_{SD}	Supply Current in Power-Down Mode (Note 6)	V_{CC} = 5V, C-Grade, I-Grade V_{CC} = 5V, H-Grade	● ●		0.36 0.36	1.8 5	µA µA
Digital I/O							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 7)	●			2.5	pF

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2630-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2630A-HM12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
t_S	Settling Time	V_{CC} = 5V (Note 8) ±0.39% (±1LSB at 8 Bits) ±0.098% (±1LSB at 10 Bits) ±0.024% (±1LSB at 12 Bits)			 3.7 4.4 4.8		 µs µs µs
	Voltage Output Slew Rate				1.0		V/µs
	Capacitive Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			2.4		nV•s
e_n	Output Voltage Noise Density	At f = 1kHz, Supply as Reference At f = 10kHz, Supply as Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			140 130 210 200		nV/√Hz nV/√Hz nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz, Supply as Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, Supply as Reference 0.1Hz to 200kHz, Internal Reference			20 20 650 750		μV_{P-P} μV_{P-P} μV_{P-P} μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V. (See Figure 1) (Note 7).

LTC2630-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2630A-HM12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_1	SDI Valid to SCK Setup		●	4			ns
t_2	SDI Valid to SCK Hold		●	4			ns
t_3	SCK High Time		●	9			ns
t_4	SCK Low Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse width		●	10			ns
t_6	SCK High to $\overline{CS}$/LD High		●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND.

Note 3: Linearity and monotonicity are defined from code k_L to code 2^N–1, where N is the resolution and k_L is given by $k_L = 0.016 \bullet (2^N / V_{FS})$, rounded to the nearest whole code. For V_{FS} = 2.5V and N = 12, k_L = 26 and linearity is defined from code 26 to code 4,095. For V_{FS} = 4.096V and N = 12, k_L = 16 and linearity is defined from code 16 to code 4,095.

Note 4: Inferred from measurement at code 16 (LTC2630-12), code 4 (LTC2630-10) or code 1 (LTC2630-8).

Note 5: This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: Digital inputs at 0V or V_{CC}.

Note 7: Guaranteed by design and not production tested.

Note 8: Internal Reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 100pF to GND.

Note 9: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

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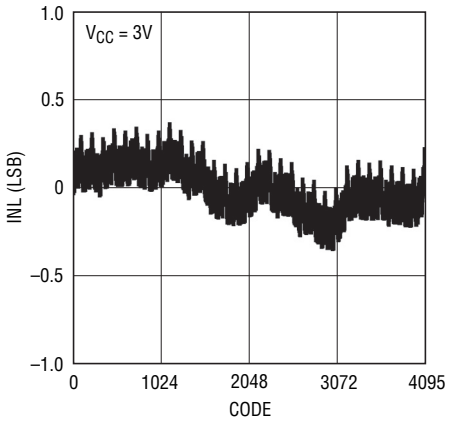
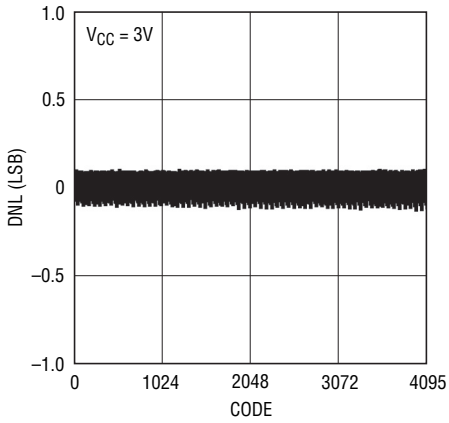
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2630-LM12/-LZ12 (V_{FS} = 2.5V)

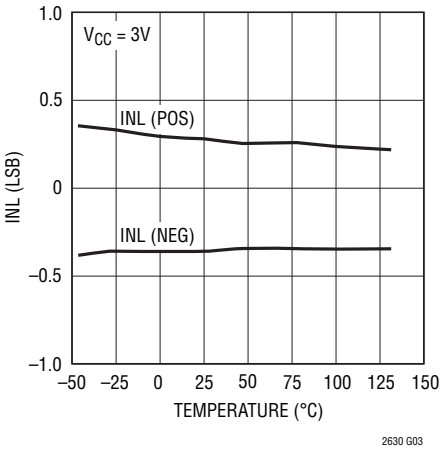
Integral Nonlinearity (INL)



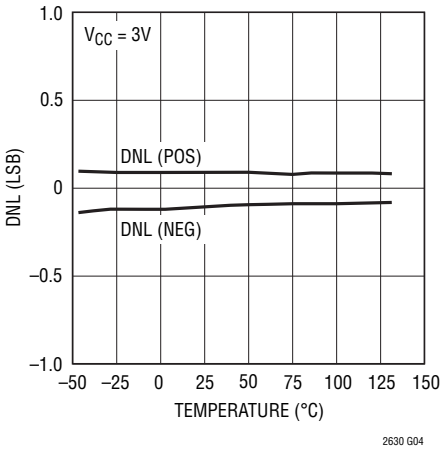
Differential Nonlinearity (DNL)



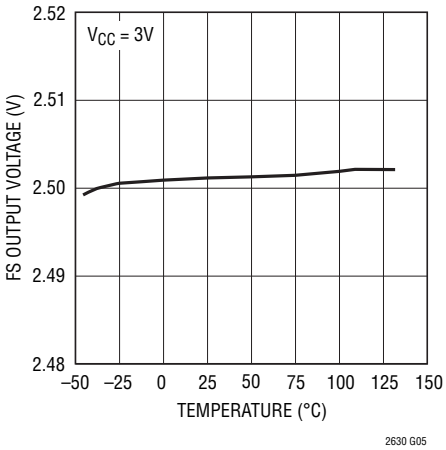
INL vs Temperature



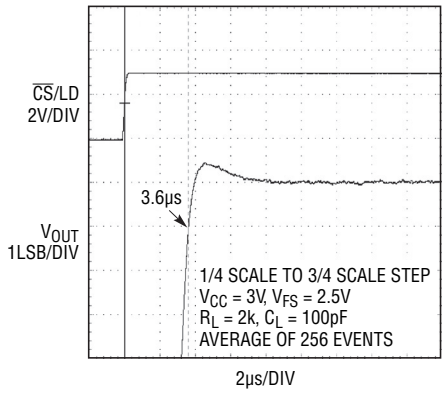
DNL vs Temperature



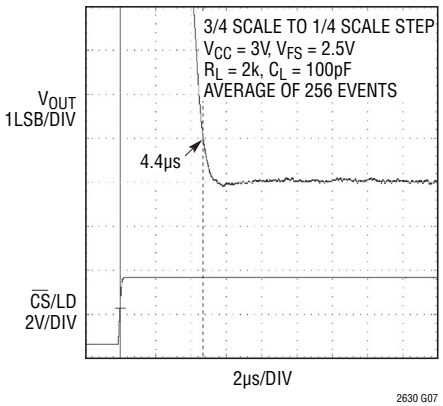
Full-Scale Output Voltage vs Temperature



Settling to ±1LSB



Settling to ±1LSB



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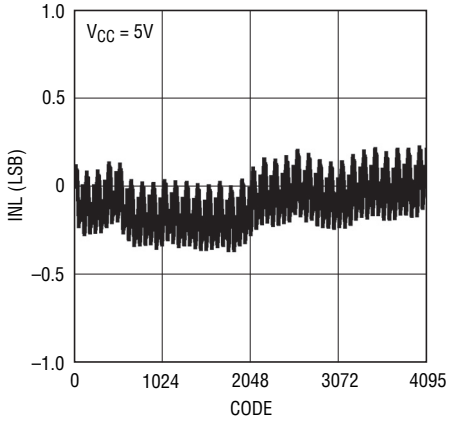
TYPICAL PERFORMANCE CHARACTERISTICS

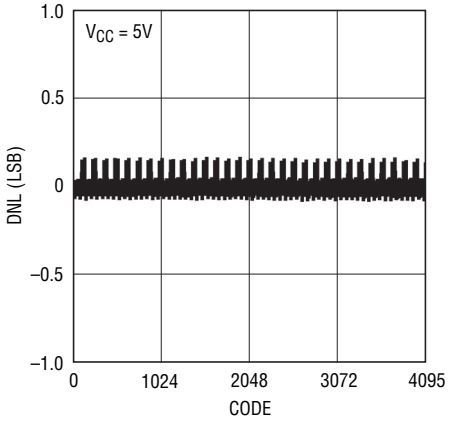
LTC2630-HM12/-HZ12 (V_{FS} = 4.096V)

Integral Nonlinearity (INL)



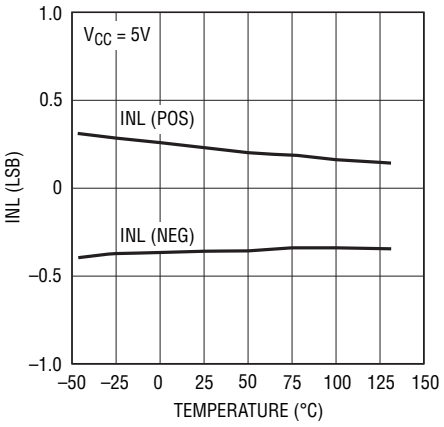
2630 G08

Differential Nonlinearity (DNL)



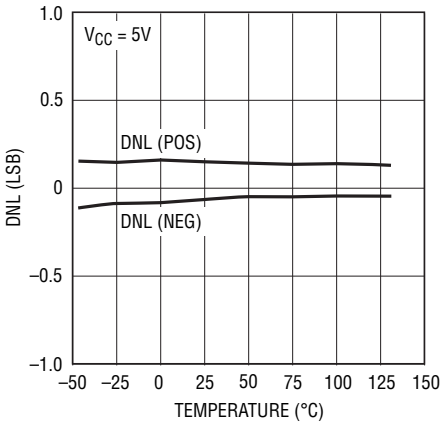
2630 G09

INL vs Temperature



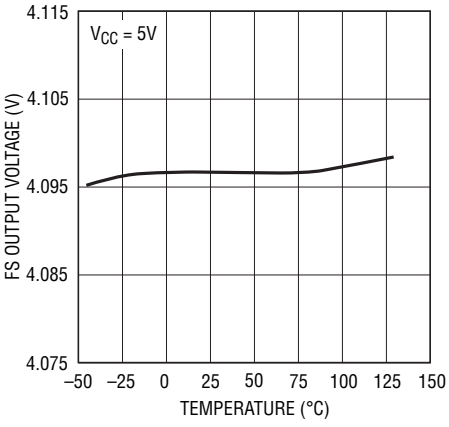
2630 G10

DNL vs Temperature



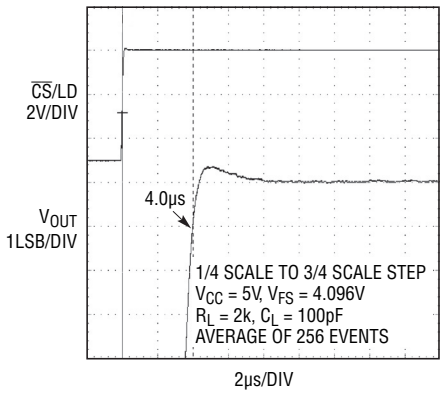
2630 G11

Full-Scale Output Voltage vs Temperature



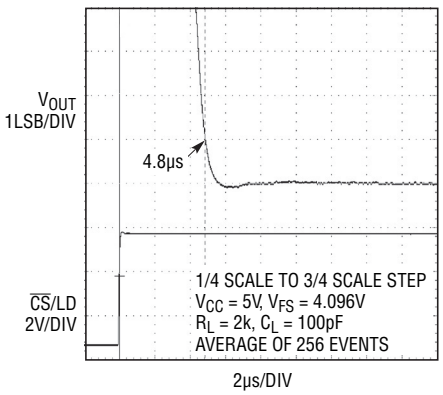
2630 G12

Settling to ±1LSB



2630 G13

Settling to ±1LSB



2630 G14

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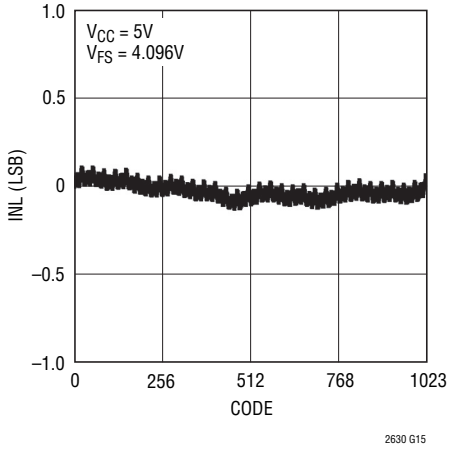
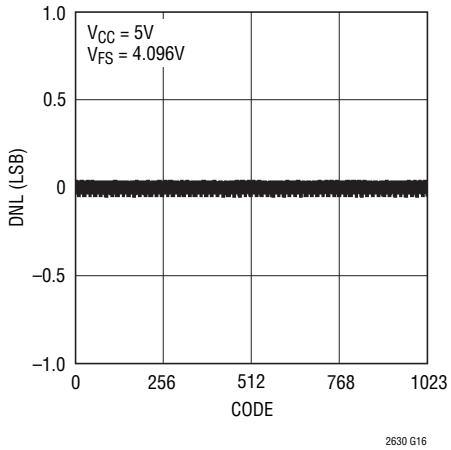
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2630-10

Integral Nonlinearity (INL)

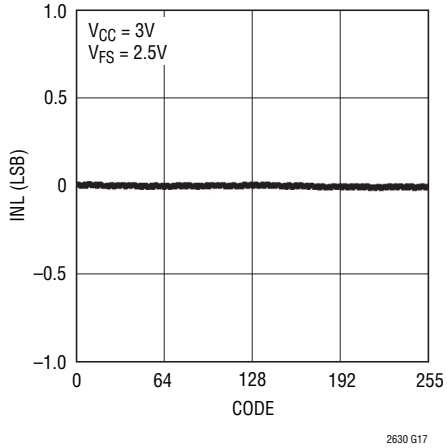


Differential Nonlinearity (DNL)

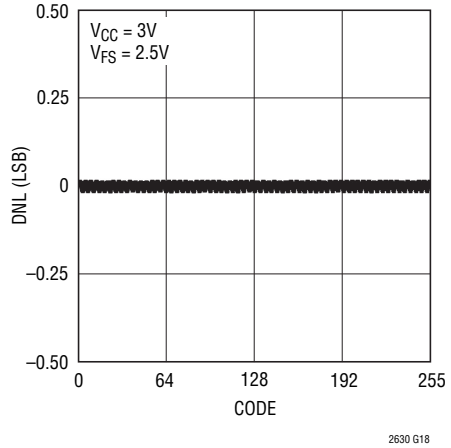


LTC2630-8

Integral Nonlinearity (INL)

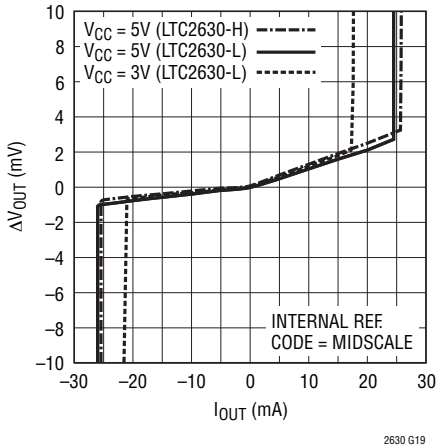


Differential Nonlinearity (DNL)

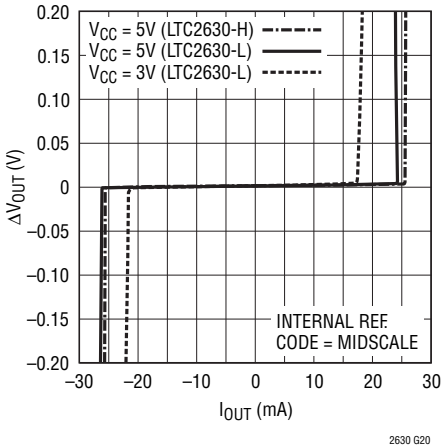


LTC2630

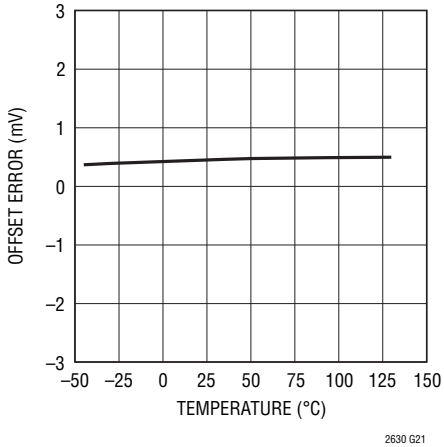
Load Regulation



Current Limiting



Offset Error vs Temperature



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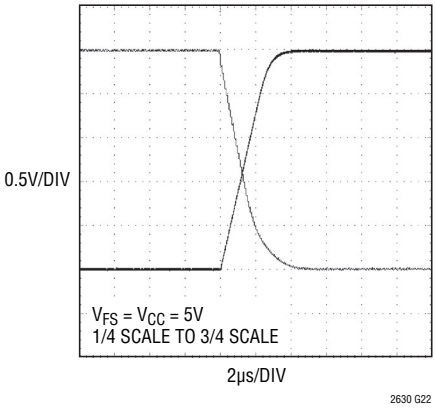
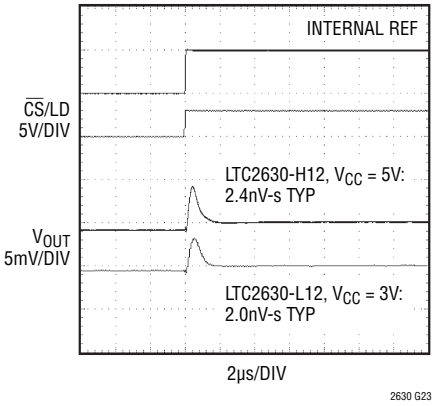
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2630

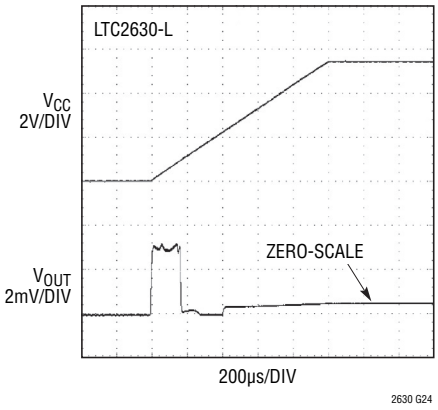
Large-Signal Response



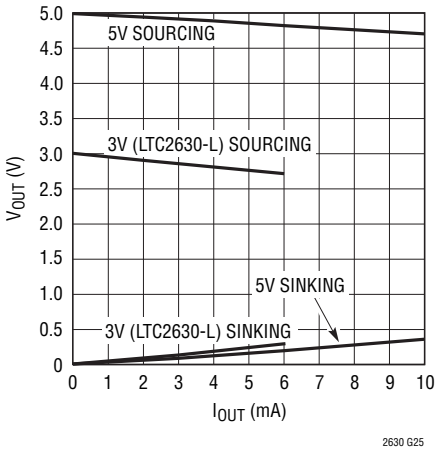
Mid-Scale-Glitch Impulse



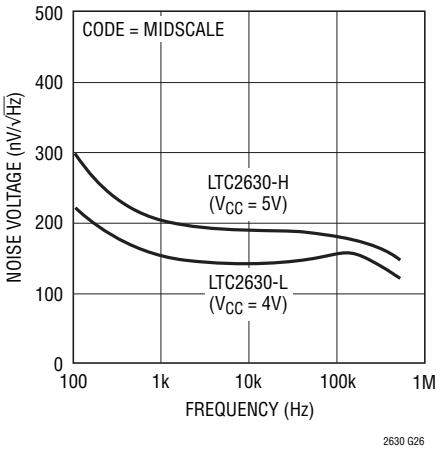
Power-On Reset Glitch



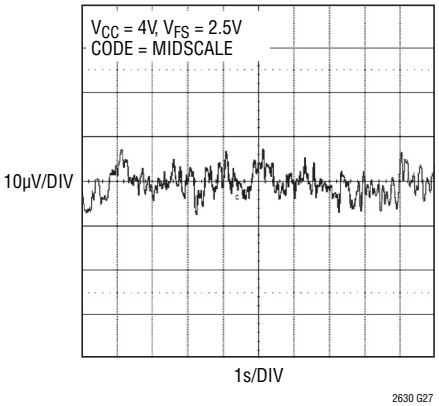
Headroom at Rails vs Output Current



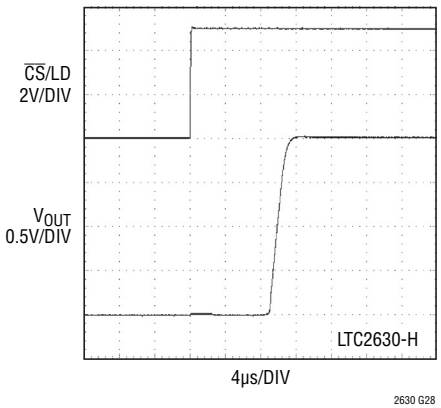
Noise Voltage vs Frequency



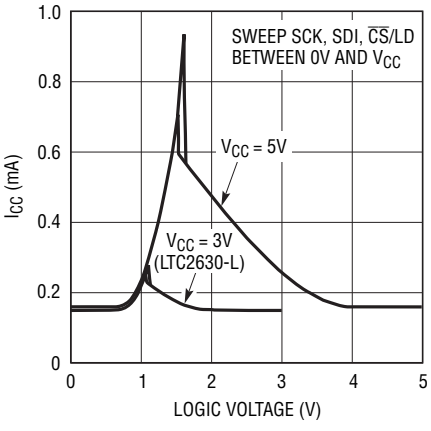
0.1Hz to 10Hz Voltage Noise



Exiting Power-Down to Mid-Scale



Supply Current vs Logic Voltage



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PIN FUNCTIONS

$\overline{CS}$/LD (Pin 1): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

SCK (Pin 2): Serial Interface Clock Input. CMOS and TTL compatible.

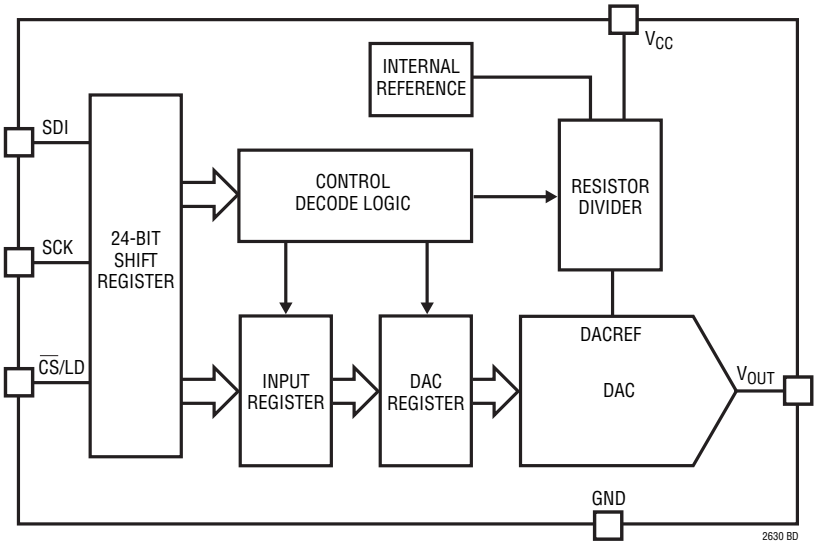
SDI (Pin 3): Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2630 accepts input word lengths of either 24 or 32 bits.

V_{CC} (Pin 4): Supply Voltage Input. 2.7V ≤ V_{CC} ≤ 5.5V (LTC2630-L) or 4.5V ≤ V_{CC} ≤ 5.5V (LTC2630-H). Also used as the reference input when the part is programmed to operate in supply as reference mode. Bypass to GND with a 0.1µF capacitor.

GND (Pin 5): Ground.

V_{OUT} (Pin 6): DAC Analog Voltage Output.

BLOCK DIAGRAM



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TIMING DIAGRAM

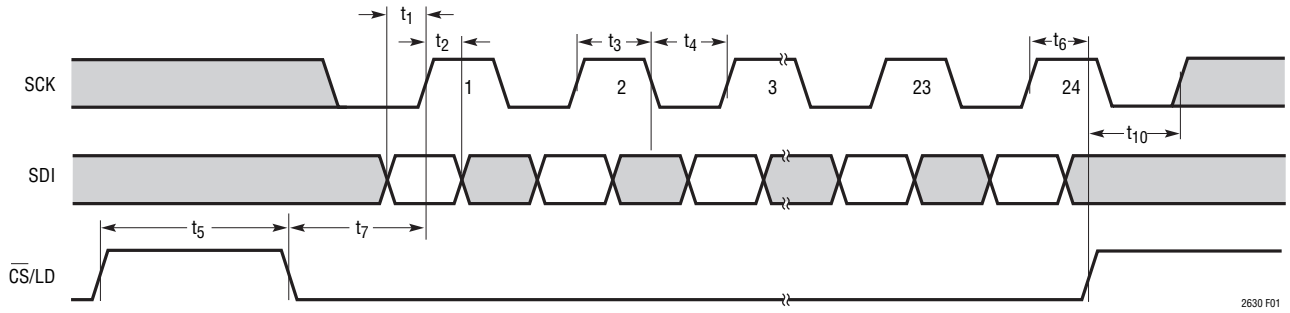

Figure 1. Serial Interface Timing

OPERATION

The LTC2630 is a family of single voltage output DACs in 6-lead SC70 packages. Each DAC can operate rail-to-rail referenced to the input supply, or with its full-scale voltage set by an integrated reference. Twelve combinations of accuracy (12-, 10-, and 8-bit), power-on reset value (zero or mid-scale), and full-scale voltage (2.5V or 4.096V) are available. The LTC2630 is controlled using a 3-wire SPI/MICROWIRE compatible interface.

Power-On Reset

The LTC2630-HZ/-LZ clear the output to zero scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2630 contains circuitry to reduce the power-on glitch: the analog output typically rises less than 5mV above zero scale during power on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased. See “Power-On Reset Glitch” in the Typical Performance Characteristics section.

The LTC2630-HM/-LM provide an alternative reset, setting the output to mid-scale when power is first applied.

Transfer Function

The digital-to-analog transfer function is

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution, and V_{REF} is either 2.5V (LTC2630-L) or 4.096V (LTC2630-H) in internal reference mode, and V_{CC} in Supply as reference mode.

Table 1. Command Codes

Command*				
C3	C2	C1	C0	
0	0	0	0	Write to Input Register
0	0	0	1	Update (Power up) DAC Register
0	0	1	1	Write to and Update (Power up) DAC Register
0	1	0	0	Power down
0	1	1	0	Select Internal Reference (Power-on Reset Default)
0	1	1	1	Select Supply as Reference ($V_{REF} = V_{CC}$)

*Command codes not shown are reserved and should not be used.

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OPERATION

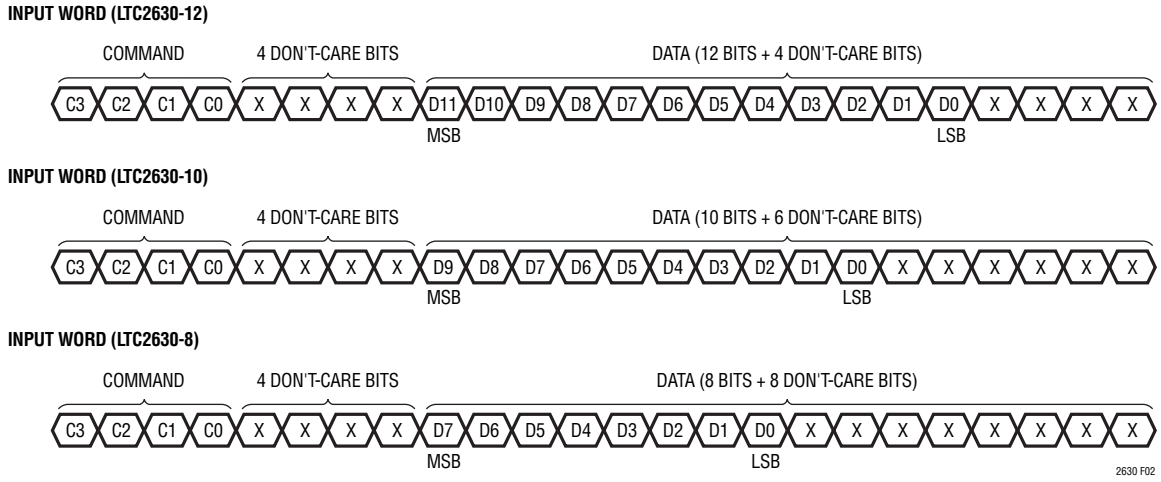

Figure 2. Command and Data Input Format

Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, enabling the SDI and SCK buffers and the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then 4 don't-care bits; and finally the 16-bit data word. The data word comprises the 12-, 10- or 8-bit input code, ordered MSB-to-LSB, followed by 4, 6 or 8 don't-care bits (LTC2630-12, -10 and -8 respectively; see Figure 2). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low, beginning on the first rising edge of SCK. SCK may be high or low at the falling edge of $\overline{CS}$/LD. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to execute the command specified in the 24-bit input sequence. The complete sequence is shown in Figure 3a.

The command (C3-C0) assignments are shown in Table 1. The first three commands in the table consist of write and update operations. A Write operation loads a 16-bit data word from the 24-bit shift register into the input register. In an Update operation, the input register is copied to the DAC register and converted to an analog voltage at the DAC output. Write to and Update combines the first two commands. The Update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

While the minimum input sequence is 24-bits, it may optionally be extended to 32-bits to accommodate microprocessors that have a minimum word width of 16-bits (2 bytes). To use the 32-bit width, 8 don't-care bits are transferred to the device first, followed by the 24-bit sequence described. Figure 3b shows the 32-bit sequence.

The 16-bit data word is ignored for all commands that do not include a Write operation.

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OPERATION

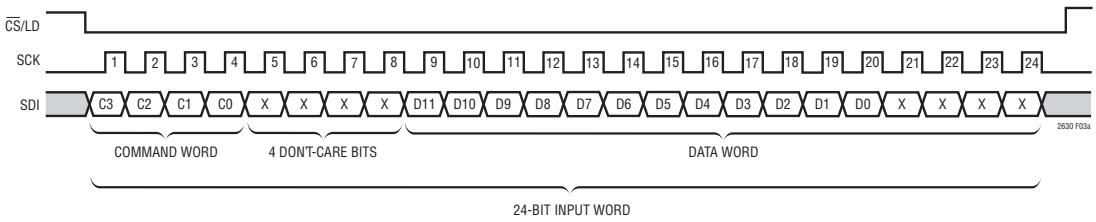

Figure 3a. 24-Bit Load Sequence (Minimum Input Word)
LTC2630-12 SDI Data Word: 12-Bit Input Code + 4 Don't-Care Bits (Shown);
LTC2630-10 SDI Data Word: 10-Bit Input Code + 6 Don't-Care Bits;
LTC2630-8 SDI Data Word: 8-Bit Input Code + 8 Don't-Care Bits

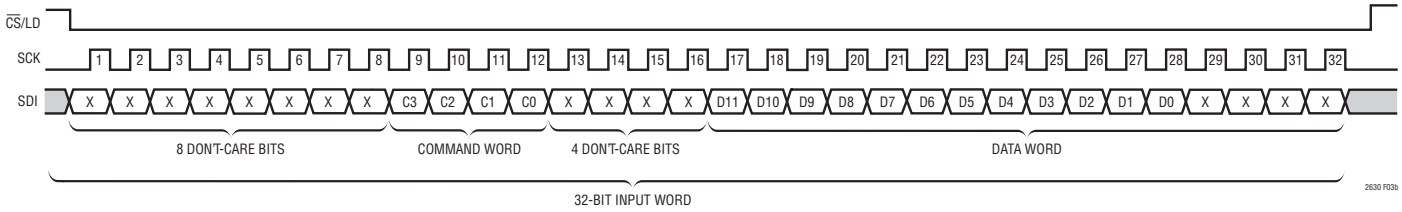

Figure 3b. 32-Bit Load Sequence
LTC2630-12 SDI Data Word: 12-Bit Input Code + 4 Don't-Care Bits (Shown);
LTC2630-10 SDI Data Word: 10-Bit Input Code + 6 Don't-Care Bits;
LTC2630-8 SDI Data Word: 8-Bit Input Code + 8 Don't-Care Bits

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OPERATION

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever the DAC output is not needed. When in power-down, the buffer amplifier, bias circuit, and reference circuit are disabled and draw essentially zero current. The DAC output is put into a high-impedance state, and the output pin is passively pulled to ground through a 200kΩ resistor. Input and DAC register contents are not disturbed during power-down.

The DAC can be put into power-down mode by using command 0100. The supply current is reduced to 1.8µA maximum when the DAC is powered down.

Normal operation resumes after executing any command that includes a DAC update, as shown in Table 1. The DAC is powered up and its voltage output is updated. Normal settling is delayed while the bias, reference, and amplifier circuits are re-enabled. The power-up delay time is 18µs for settling to 12-bits.

Reference Modes

For applications where an accurate external reference is not available, the LTC2630 has a user-selectable, integrated reference. The LTC2630-LM and LTC2630-LZ provide a full-scale output of 2.5V. The LTC2630-HM and LTC2630-HZ provide a full-scale output of 4.096V.

The internal reference can be useful in applications where the supply voltage is poorly regulated. Internal Reference mode can be selected by using command 0110, and is the power-on default.

The DAC can also operate in supply as reference mode using command 0111. In this mode, V_{CC} supplies the DAC's reference voltage and the supply current is reduced.

Voltage Output

The LTC2630's integrated rail-to-rail amplifier has guaranteed load regulation when sourcing or sinking up to 10mA at 5V, and 5mA at 3V.

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load current. The measured change in output voltage per change in forced load current is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to ohms. The amplifier's DC output impedance is 0.1Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 50Ω typical channel resistance of the output devices (e.g., when sinking 1mA, the minimum output voltage is 50Ω • 1mA, or 50mV). See the graph "Headroom at Rails vs. Output Current" in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 500pF.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the DAC cannot go below ground, it may limit for the lowest codes as shown in Figure 4b. Similarly, limiting can occur near full scale when using the supply as reference. If $V_{FS} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC}, as shown in Figure 4. No full-scale limiting can occur if V_{FS} is less than V_{CC}–FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

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OPERATION

Board Layout

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane. The resistance from the LTC2630 GND pin to the ground plane should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.1Ω). Note that the LTC2630 is no more susceptible to this effect than any other parts of this type; on the contrary, it allows layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Another technique for minimizing errors is to use a separate power ground return trace on another board layer. The trace should run between the point where the power supply is connected to the board and the DAC ground pin. Thus the DAC ground pin becomes the common point for analog ground, digital ground, and power ground. When the LTC2630 is sinking large currents, this current flows out the ground pin and directly to the power ground trace without affecting the analog ground plane voltage.

It is sometimes necessary to interrupt the ground plane to confine digital ground currents to the digital portion of the plane. When doing this, make the gap in the plane only as long as it needs to be to serve its purpose and ensure that no traces cross over the gap.

Opto-Isolated 4mA to 20mA Process Controller

Figure 5 shows how to use an LTC2630Hz to make an opto-isolated, digitally-controlled 4mA to 20mA transmitter. The transmitter circuitry, including opto-isolation, is powered by the loop voltage which has a wide range of 5.4V to 80V. The 5V output of the LT®3010-5 is used to set the 4mA offset current and V_{OUT} is used to digitally control the 0mA to 16mA signal current. The supply current for the regulator, DAC, and op amp is well below the 4mA budget at zero scale. R_S senses the total loop current, which includes the quiescent supply current and additional current through Q1. Note that at the maximum loop voltage of 80V, Q1 will dissipate 1.6W when I_{OUT} = 20mA and must have an appropriate heat sink.

R_{OFFSET} and R_{GAIN} are the closest 0.1% values to ideal for controlling a 4mA to 20mA output as the digital input varies from zero scale to full scale. Alternatively, R_{OFFSET} can be a 365k, 1% resistor in series with a 20k trim pot and R_{GAIN} can be a 75.0k, 1% resistor in series with a 5k trim pot. The opto-isolators shown will limit the speed of the serial bus; the 6N139 is an alternative that will allow higher data rates.

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OPERATION

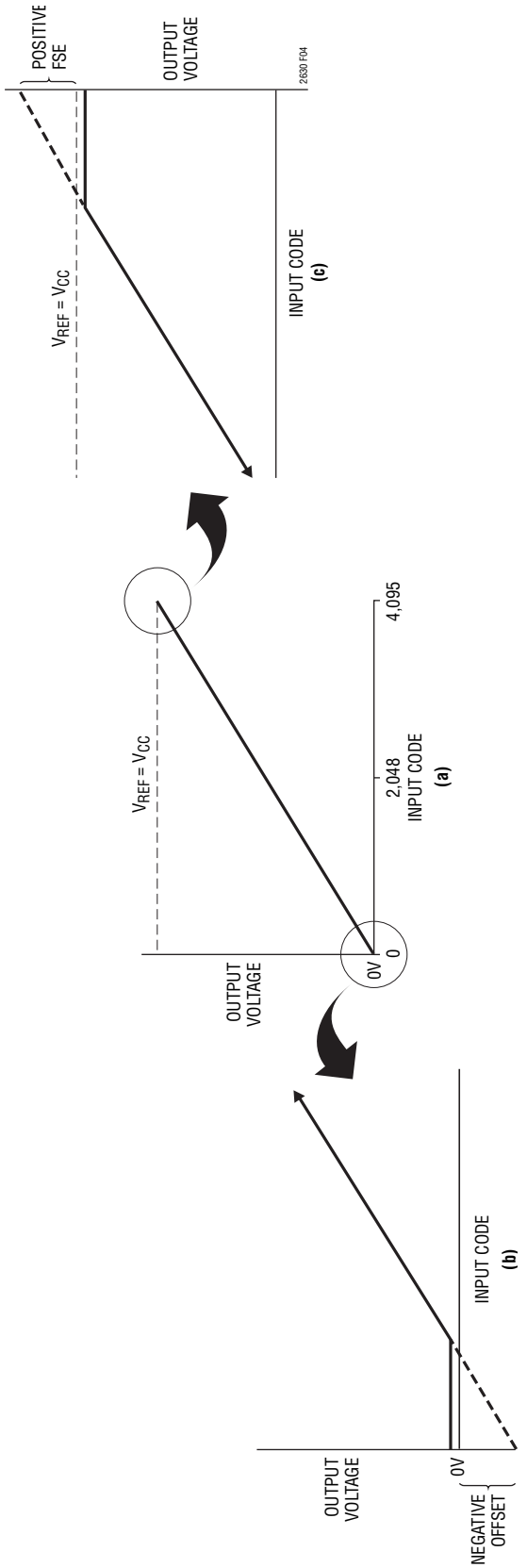

Figure 4. Effects of Rail-to-Rail Operation on a DAC Transfer Curve (Shown for 12-Bits).
(a) Overall Transfer Function
(b) Effect of Negative Offset for Codes Near Zero
(c) Effect of Positive Full-Scale Error for Codes Near Full Scale

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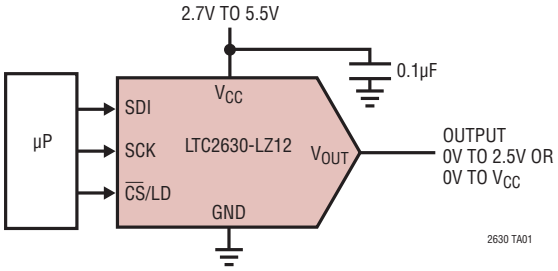
TYPICAL APPLICATION

12-Bit, 2.7V to 5.5V Single Supply, Voltage Output DAC



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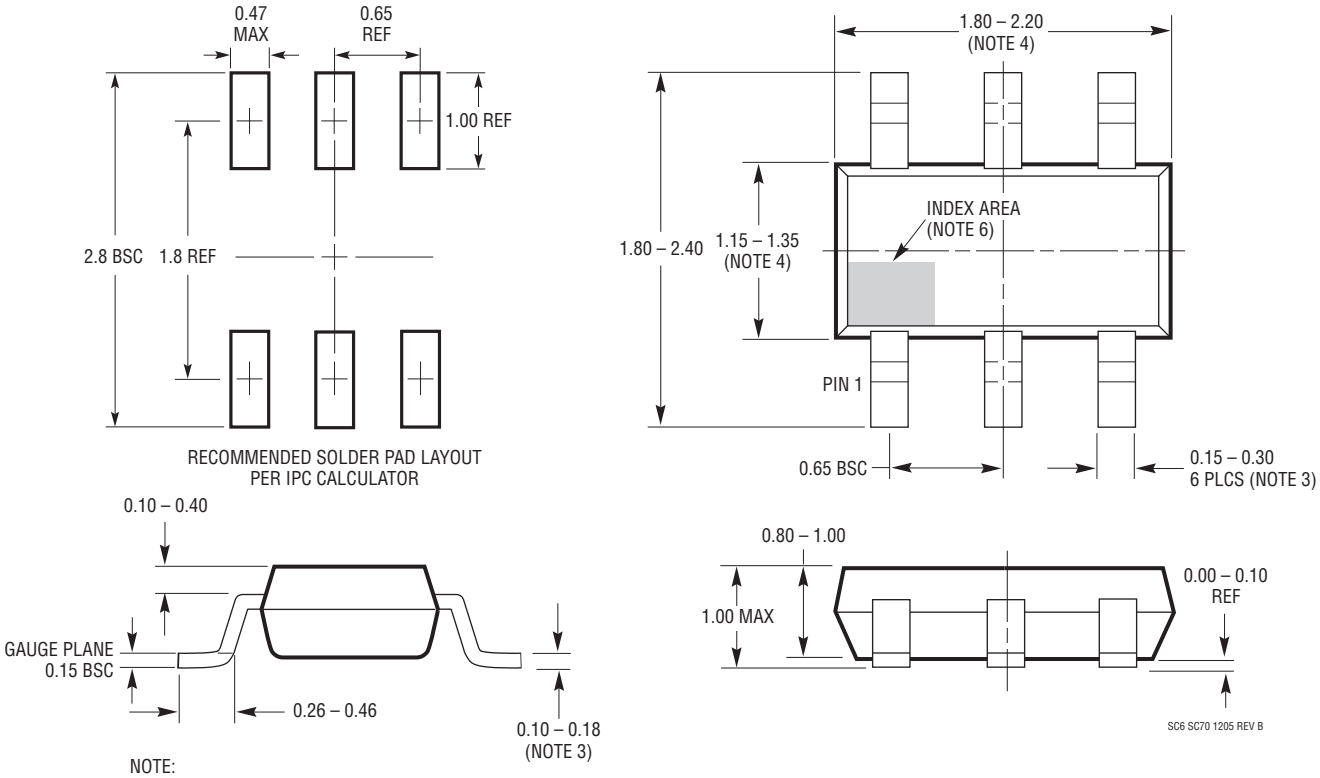
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2630#packaging for the most recent package drawings.

SC6 Package
6-Lead Plastic SC70
(Reference LTC DWG # 05-08-1638 Rev B)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. DETAILS OF THE PIN 1 IDENTIFIER ARE OPTIONAL,
   BUT MUST BE LOCATED WITHIN THE INDEX AREA
7. EIAJ PACKAGE REFERENCE IS EIAJ SC-70
8. JEDEC PACKAGE REFERENCE IS MO-203 VARIATION AB

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REVISION HISTORY (Revision history begins at Rev F)

REV	DATE	DESCRIPTION	PAGE NUMBER
F	06/12	Corrected units on parameter V_{OSTC} from mV/°C to µV/°C	6
G	06/17	Removed Note 3	7

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TYPICAL APPLICATION

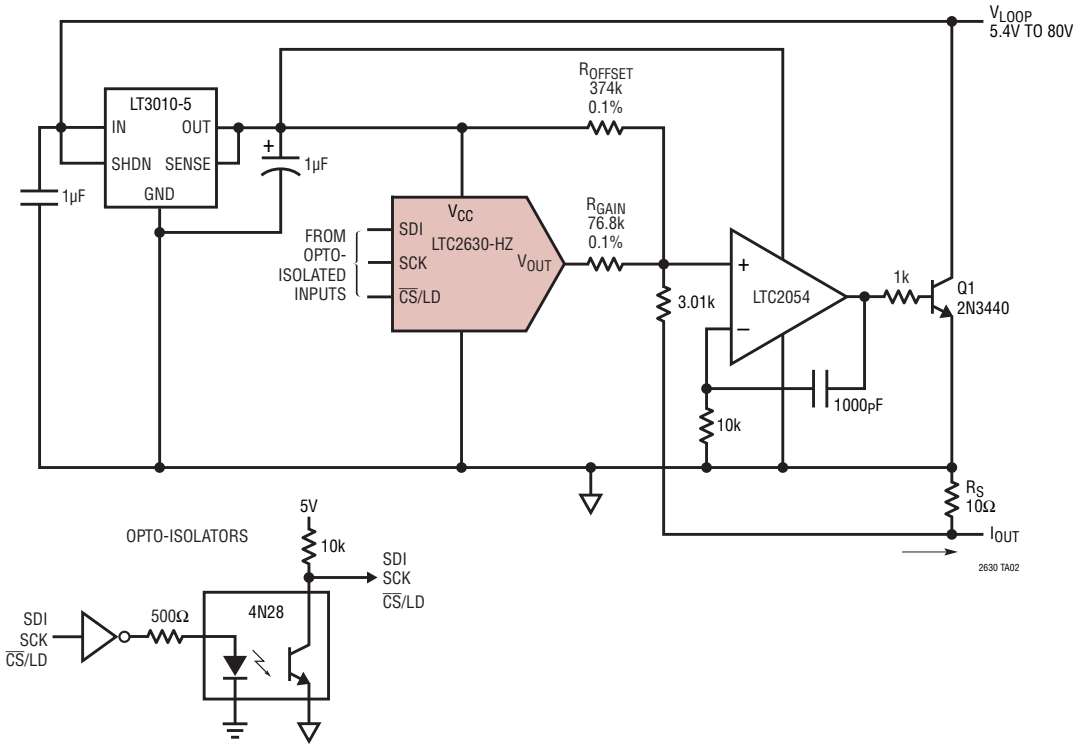

Figure 5. An Opto-Isolated 4mA to 20mA Process Controller

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1660/LTC1665	Octal 10-/8-Bit V_{OUT} DACs in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1663	Single 10-Bit V_{OUT} DAC in SOT-23	V_{CC} = 2.7V to 5.5V, 60µA, Internal reference, SMBus Interface
LTC1664	Quad 10-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1669	Single 10-Bit V_{OUT} DAC in SOT-23	V_{CC} = 2.7V to 5.5V, 60µA, Internal reference, I^2C Interface
LTC1821	Parallel 16-Bit Voltage Output DAC	Precision 16-Bit Settling in 2µs for 10V Step
LTC2600/LTC2610/LTC2620	Octal 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2601/LTC2611/LTC2621	Single 16-/14-/12-Bit V_{OUT} DACs in 10-Lead DFN	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2602/LTC2612/LTC2622	Dual 16-/14-/12-Bit V_{OUT} DACs in 8-Lead MSOP	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2604/LTC2614/LTC2624	Quad 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2631	Single 12-/10-/8-Bit I^2C V_{OUT} DACs with 10ppm/°C Reference in ThinSOT	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Selectable External Ref. Mode, Rail-to-Rail Output, I^2C Interface
LTC2640	Single 12-/10-/8-Bit SPI V_{OUT} DACs with 10ppm/°C Reference in ThinSOT	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Selectable External Ref. Mode, Rail-to-Rail Output, SPI Interface

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