

FEATURES

- 0.8 Ω typical on resistance
- Less than 1 Ω maximum on resistance at 85°C
- 1.8 V to 5.5 V single supply
- High current carrying capability: 300 mA continuous
- Rail-to-rail switching operation
- Fast-switching times: <17 ns
- Typical power consumption: <0.1 μ W
- 1.30 mm \times 1.60 mm, 10-lead mini LFCSP

APPLICATIONS

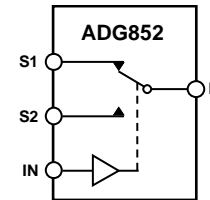
- Cellular phones
- PDA's
- MP3 players
- Power routing
- Battery-powered systems
- PCMCIA cards
- Modems
- Audio and video signal routing
- Communication systems

GENERAL DESCRIPTION

The ADG852 is a low voltage CMOS single-pole, double-throw (SPDT) switch. This device offers ultralow on resistance of less than 1 Ω over the full temperature range. The ADG852 is fully specified for 5.5 V and 3.3 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. The ADG852 exhibits break-before-make switching action.

The ADG852 is available in a 1.30 mm \times 1.60 mm 10-lead mini LFCSP.

FUNCTIONAL BLOCK DIAGRAM

NOTES
1. SWITCHES SHOWN
FOR A LOGIC 1 INPUT.

07461-001

Figure 1.

PRODUCT HIGHLIGHTS

- <1 Ω over full temperature range of -40°C to $+85^{\circ}\text{C}$.
- Single 1.8 V to 5.5 V operation.
- Compatible with 1.8 V CMOS logic.
- High current handling capability (300 mA continuous current per channel).
- Low THD + N: 0.08% typical.
- 1.30 mm \times 1.60 mm, 10-lead mini LFCSP.

Rev. B

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REVISION HISTORY

5/12—Rev. A to Rev. B

Changes to Ordering Guide	13
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10/08—Rev. 0 to Rev. A

Change to Title.....	1
Changes to Features Section.....	1
Changes to Product Highlights Section.....	1

8/08—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 4.2\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance, R_{ON}	0.8		Ω typ	$V_{DD} = 4.2\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 100\text{ mA}$; see Figure 16
	0.85	1	Ω max	
On Resistance Match Between Channels, ΔR_{ON}	0.02		Ω typ	$V_{DD} = 4.2\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 100\text{ mA}$
		0.04	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.17		Ω typ	$V_{DD} = 4.2\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 100\text{ mA}$
		0.23	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 10		pA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 0.6\text{ V}/4.2\text{ V}$, $V_D = 4.2\text{ V}/0.6\text{ V}$; see Figure 17
Channel On Leakage, I_D , I_S (On)	± 30		pA typ	$V_S = V_D = 0.6\text{ V or }4.2\text{ V}$; see Figure 18
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.002		μA typ	$V_{IN} = V_{GND}$ or V_{DD}
		0.05	μA max	
C_{IN} , Digital Input Capacitance	2.5		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	17		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	23	28	ns max	$V_S = 3\text{ V}/0\text{ V}$; see Figure 19
t_{OFF}	6		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	8.5	9.2	ns max	$V_S = 3\text{ V}$; see Figure 19
Break-Before-Make Time Delay, t_{BBM}	14		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
		8	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$; see Figure 20
Charge Injection	30		pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 21
Off Isolation	-75		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 22
Channel-to-Channel Crosstalk	-73		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 24
Total Harmonic Distortion, THD + N	0.08		%	$R_L = 32\ \Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_S = 3.5\text{ V p-p}$
Insertion Loss	-0.6		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 23
-3 dB Bandwidth	100		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 23
C_S (Off)	19.5		pF typ	
C_D , C_S (On)	50		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.002		μA typ	$V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or 5.5 V
		1.0	μA max	

¹ Guaranteed by design, not subject to production test.

$V_{DD} = 2.7\text{ V}$ to 3.6 V , $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance, R_{ON}	1.3		Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 100\text{ mA}$; see Figure 16
	1.5	1.7	Ω max	
On Resistance Match Between Channels, ΔR_{ON}	0.03		Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0.6\text{ V}$, $I_{DS} = 100\text{ mA}$
		0.05	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.48		Ω typ	$V_{DD} = 4.2\text{ V}$, $V_S = 0\text{ V}$ to V_{DD} , $I_{DS} = 100\text{ mA}$
		0.66	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 10		pA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$; see Figure 17
Channel On Leakage, I_D , I_S (On)	± 30		pA typ	$V_S = V_D = 0.6\text{ V}$ or 3.3 V ; see Figure 18
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.35	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.002		μA typ	$V_{IN} = V_{GND}$ or V_{DD}
		0.05	μA max	
C_{IN} , Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS¹				
t_{ON}	25		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	37	43	ns max	$V_S = 1.5\text{ V}/0\text{ V}$; see Figure 19
t_{OFF}	7		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	7.4	8	ns max	$V_S = 1.5\text{ V}$; see Figure 19
Break-Before-Make Time Delay, t_{BBM}	22		ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
		13	ns min	$V_{S1} = V_{S2} = 1\text{ V}$; see Figure 20
Charge Injection	23		pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\text{ V}$, $C_L = 1\text{ nF}$; see Figure 21
Off Isolation	-75		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 22
Channel-to-Channel Crosstalk	-73		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 24
Total Harmonic Distortion, THD	0.15		%	$R_L = 32\ \Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_S = 1.5\text{ V}$ p-p
Insertion Loss	-0.07		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 23
-3 dB Bandwidth	100		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 23
C_S (Off)	20		pF typ	
C_D , C_S (On)	52		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.002		μA typ	$V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V
		1.0	μA max	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	-0.3 V to +6 V
Analog Inputs ¹	-0.3 V to $V_{DD} + 0.3$ V
Digital Inputs ¹	-0.3 V to $V_{DD} + 0.3$ V or 10 mA, whichever occurs first
Peak Current, S or D Pins	500 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D Pins	300 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Mini LFCSP	
θ_{JA} Thermal Impedance, 3-Layer Board	131.6°C/W
Reflow Soldering, Pb-Free	
Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at the IN, S, or D pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

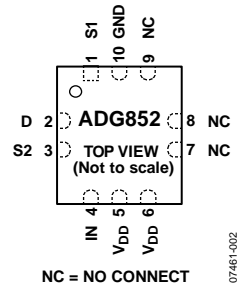


Figure 2. Pin Configurations

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1	Source Terminal. Can be an input or output.
2	D	Drain Terminal. Can be an input or output.
3	S2	Source Terminal. Can be an input or output.
4	IN	Logic Control Input.
5, 6	VDD	Most Positive Power Supply Potential.
7, 8, 9	N/C	No Connect.
10	GND	Ground (0 V) Reference.

Table 5. ADG852 Truth Table

Logic	Switch 1	Switch 2
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

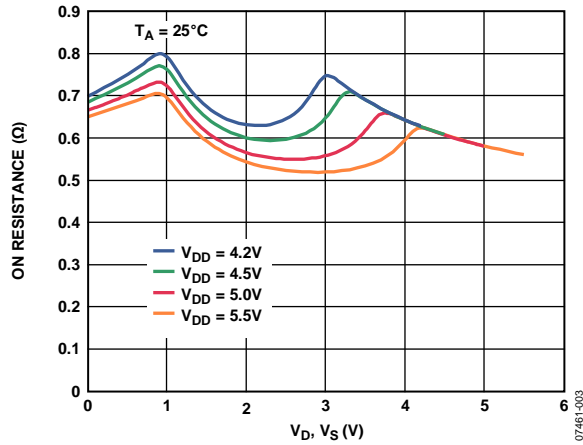


Figure 3. On Resistance vs. V_D (V_S), $V_{DD} = 4.2$ V to 5.5 V

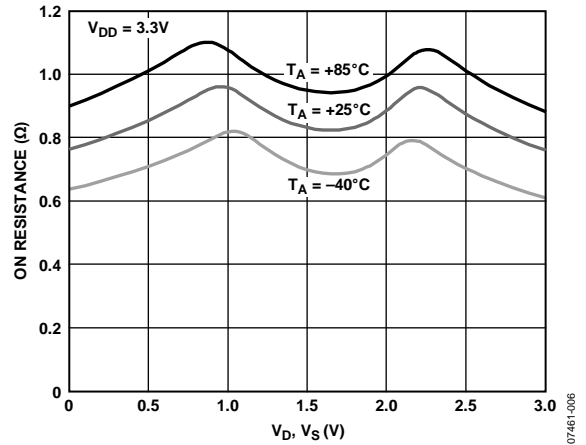


Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 3.3$ V

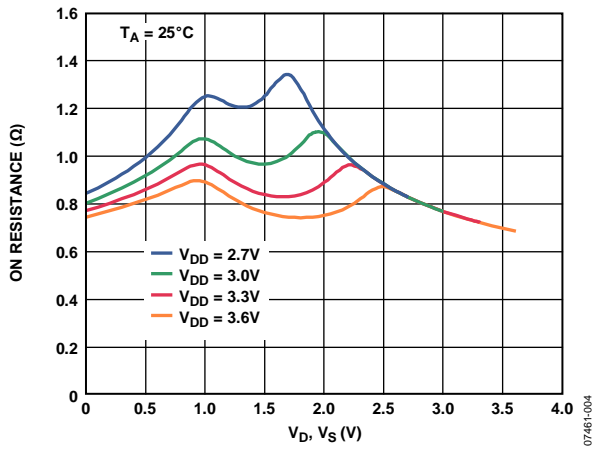


Figure 4. On Resistance vs. V_D (V_S), $V_{DD} = 2.7$ V to 3.6 V

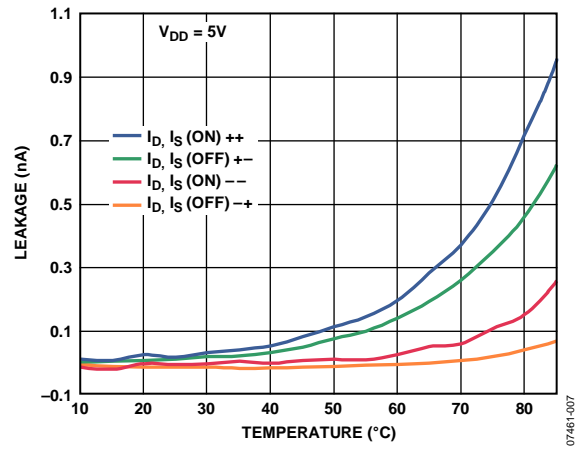


Figure 7. Leakage Current vs. Temperature, $V_{DD} = 5$ V

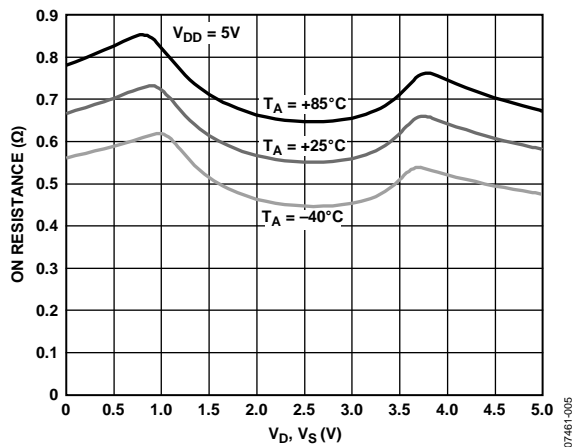


Figure 5. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 5$ V

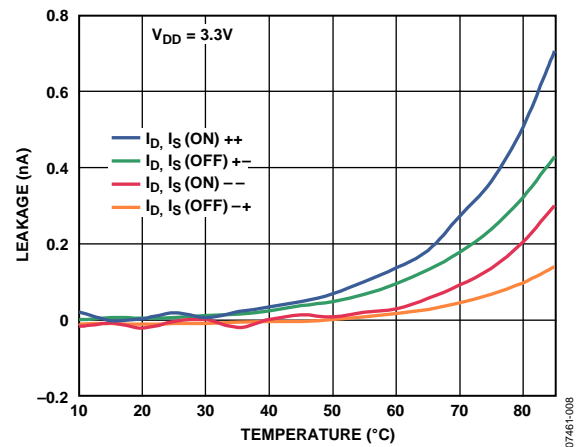


Figure 8. Leakage Current vs. Temperature, $V_{DD} = 3.3$ V

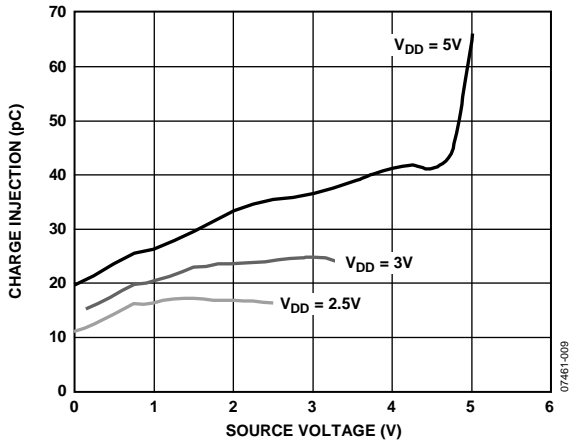


Figure 9. Charge Injection vs. Source Voltage

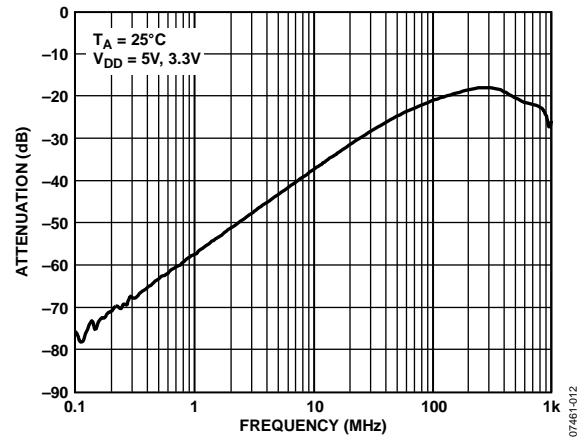


Figure 12. Off isolation vs. Frequency

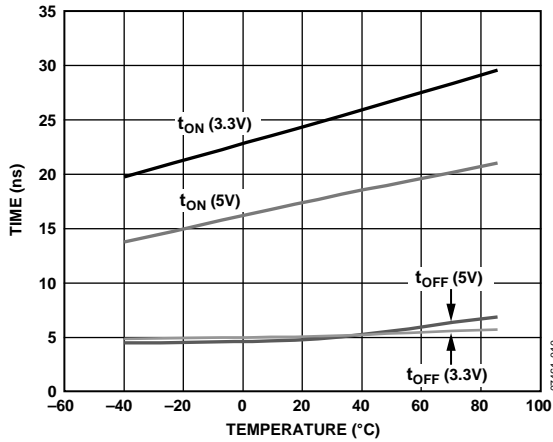


Figure 10. t_{ON}/t_{OFF} Times vs. Temperature

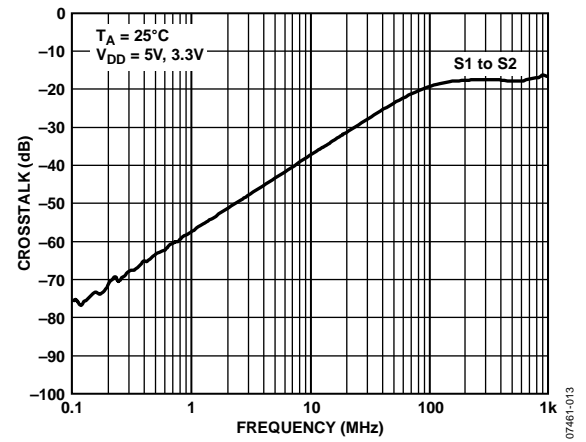


Figure 13. Crosstalk vs. Frequency

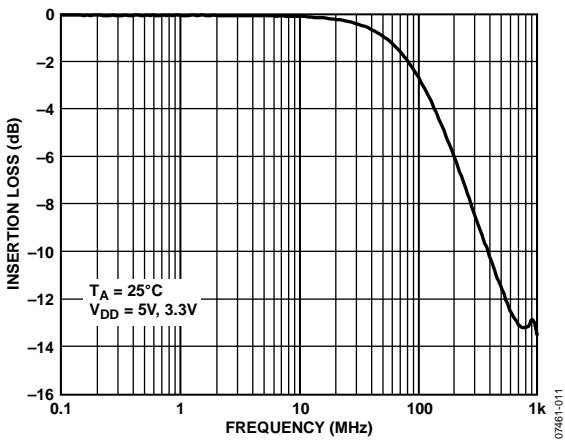


Figure 11. Bandwidth

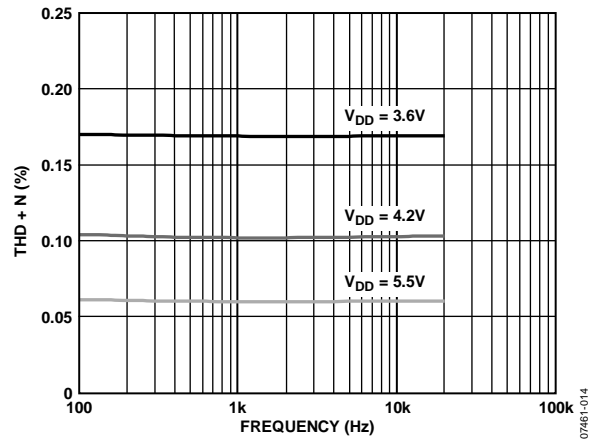


Figure 14. Total Harmonic Distortion + Noise (THD+N) vs. Frequency

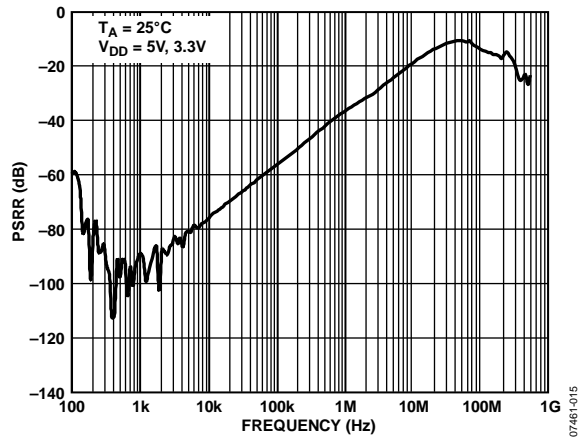


Figure 15. PSRR vs. Frequency

TEST CIRCUITS

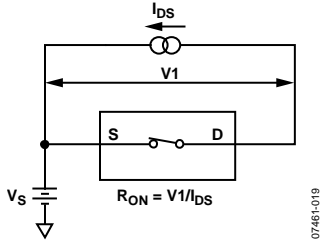


Figure 16. On Resistance

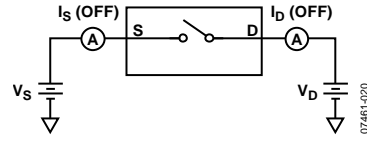


Figure 17. Off Leakage

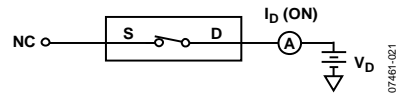


Figure 18. On Leakage

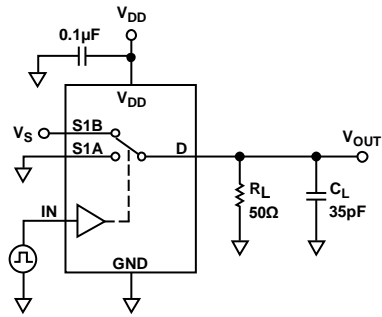


Figure 19. Switching Times, t_{ON} , t_{OFF}

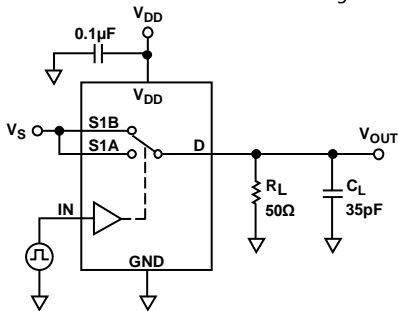
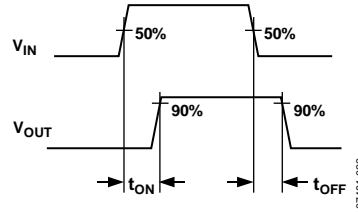


Figure 20. Break-Before-Make Time Delay, t_{BBM}

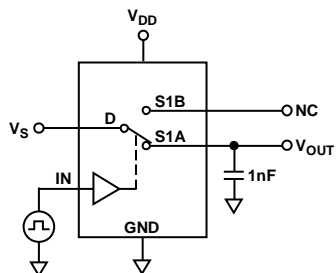
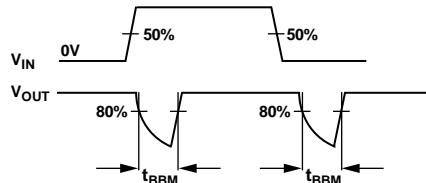
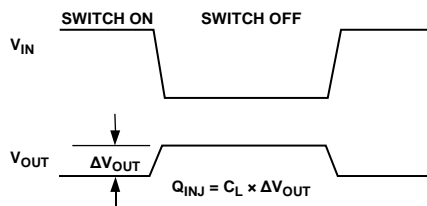


Figure 21. Charge Injection



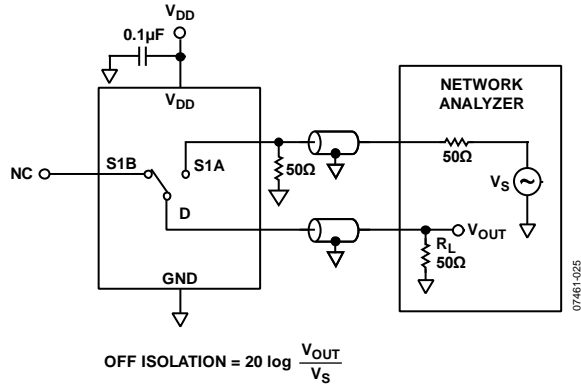


Figure 22. Off Isolation

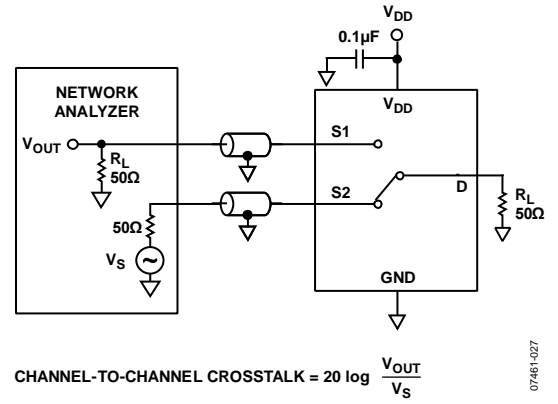


Figure 24. Channel-to-Channel Crosstalk (S1 to S2)

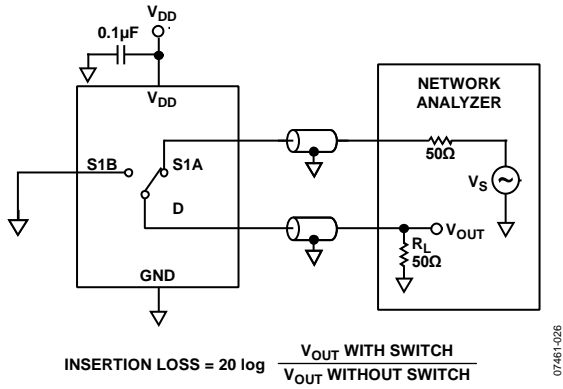


Figure 23. Bandwidth

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{FLAT} (On)

The difference between the maximum and minimum values of on resistance as measured on the switch.

ΔR_{ON}

On resistance match between any two channels.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

Off switch source capacitance. Measured with reference to ground.

C_D, C_S (On)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation

Measure of unwanted signal coupling through an off switch.

Crosstalk

Measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.

-3 dB Bandwidth

Frequency at which the output is attenuated by 3 dB.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

OUTLINE DIMENSIONS

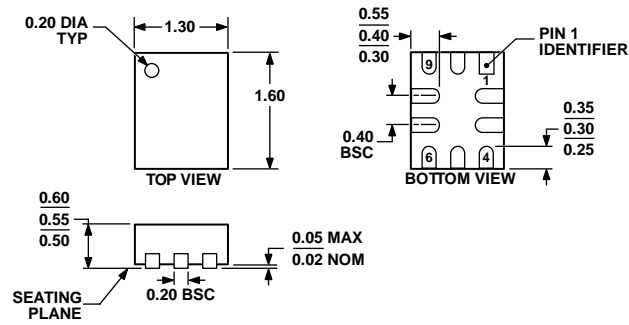


Figure 25. 10-Lead Lead Frame Chip Scale Package [LFCSP_UQ]
 1.30 mm × 1.60 mm Body, Ultrathin Quad
 (CP-10-10)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADG852BCPZ-REEL7	-40°C to +85°C	10-Lead Lead Frame Chip Scale Package (LFCSP_UQ)	CP-10-10	F

¹Z = RoHS Compliant Part.

NOTES

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