LC²MOS Quad SPST Switches

Data Sheet

ADG211A/ADG212A

FEATURES

44 V supply maximum rating
±15 V analog signal range
Low R_{ON}: 115 Ω maximum
Low leakage: 0.5 nA typical
Break-before-make switching
Single supply operation possible
Extended plastic temperature range: −40°C to +85°C
TTL/CMOS compatible
Available in 16-lead PDIP/SOIC and 20-pead PLCC packages
Pin compatible to DG211/DG212

FUNCTIONAL BLOCK DIAGRAM

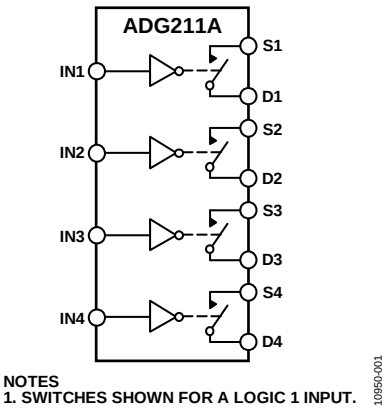

Figure 1.

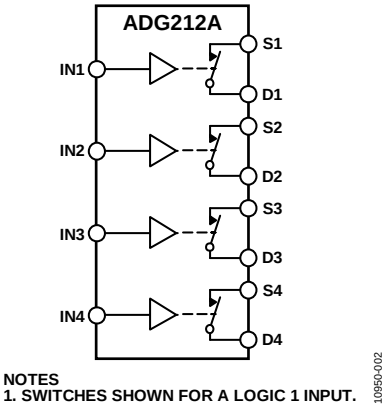

Figure 2.

GENERAL DESCRIPTION

The ADG211A and ADG212A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process, which gives an increased signal handling capability of ±15 V. These switches also feature high switching speeds and low R_{ON}.

The ADG211A and ADG212A consist of four SPST switches. They differ only in that the digital control logic is inverted. In multiplexer applications, all switches exhibit break-before-make switching action when driven simultaneously. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range.
   These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15 V.
2. Single Supply Operation.
   For applications where the analog signal is unipolar (0 V to 15 V), the switches can be operated from a single 15 V supply.
3. Low Leakage.
   Leakage currents in the range of 500 pA make these switches suitable for high precision circuits. The added feature of break-before-make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

Rev. C **Document Feedback**

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REVISION HISTORY

10/12—Rev. B to Rev. C

Updated Format ..... Universal
Added Pin Descriptions, Table 3 5
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Updated Outline Dimensions 13
Changes to Ordering Guide 14

9/02—Rev. A to Rev. B

SPECIFICATIONS

V_{DD} = +15 V, V_{SS} = −15 V, V_L = 5 V, unless otherwise noted.

Table 1.

Parameter	25°C Min	25°C Typ	25°C Max	−40°C to +85°C Min	−40°C to +85°C Typ	−40°C to +85°C Max	Unit	Test Conditions/Comments
ANALOG SWITCH								
Analog Signal Range		±15			±15		V	
R_{ON}			115			175	Ω	−10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA, see Figure 21
R_{ON} vs. V_D (V_S)		20					%	
R_{ON} Drift		0.5					%/°C	
R_{ON} Match		5					%	V_S = 0 V, I_{DS} = 1 mA
LEAKAGE CURRENTS								
I_S (Off)		0.5					nA	V_D = ±14 V; V_S = ∓ 14 V; see Figure 22
Off Input Leakage			5			100	nA	
I_D (Off)		0.5					nA	V_D = ±14 V; V_S = ∓ 14 V; see Figure 22
Off Output Leakage			5			100	nA	
I_D (On)		0.5					nA	V_D = V_S = ±14 V; see Figure 23
On Channel Leakage			5			200	nA	
DIGITAL CONTROL								
V_{INH}, Input High Voltage				2.4			V	TTL compatibility is independent of V_L
V_{INL}, Input Low Voltage						0.8	V	
I_{NL} or I_{NH}						1	μA	
C_{IN}, Digital Input Capacitance		5					pF	
DYNAMIC CHARACTERISTICS								
t_{OPEN}[1]		30					ns	See Figure 24
t_{ON}[1]			600				ns	See Figure 25
t_{OFF}[1]			450				ns	See Figure 25
Off Isolation		80					dB	V_S = 10 V (p-p); f = 100 kHz; R_L = 75 Ω; see Figure 26
Channel-to-Channel Crosstalk		80					dB	See Figure 27
C_S (Off)		5					pF	
C_D (Off)		5					pF	
C_S, C_D (On)		16					pF	
Q_{INJ}, Charge Injection		20					pC	R_S = 0 Ω; C_L = 1000 pF; V_S = 0 V; see Figure 28
POWER SUPPLY								
I_{DD}		0.6					mA	Digital inputs = V_{INL} or V_{INH}
I_{DD}			1				mA	
I_{SS}		0.1					mA	
I_{SS}			0.2				mA	
I_L			0.9				mA	

[1] Sample tested at 25°C to ensure compliance.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise stated.

Table 2.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	25 V
V_{SS} to GND	−25 V
V_L to GND	−0.3 V, 25 V
Analog Inputs[1]	
Voltage at S, D	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Continuous Current, S or D	30 mA
Pulsed Current S or D	
1 ms Duration, 10% Duty Cycle	70 mA
Digital Inputs[1]	
Voltage at IN	V_{SS} − 2 V to V_{DD} + 2 V or 20 mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470 mW
Derates above +75°C by	6 mW/°C
Operating Temperature	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

[1] Overvoltage at IN, S, or D will be clamped by diodes. Current should be limited to the Maximum Rating listed in Table 2.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

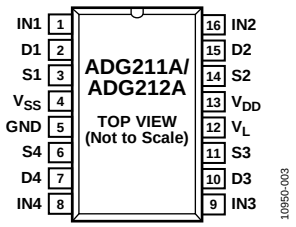


Figure 3. PDIP, SOIC Pin Configuration

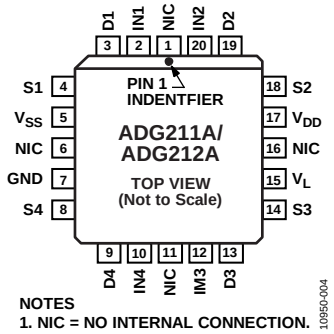


Figure 4. PLCC Pin Configuration

Table 3. Pin Function Descriptions

Pin No.			
PDIP, SOIC	**PLCC**	**Mnemonic**	**Description**
1	2	IN1	Logic Control Input.
2	3	D1	Drain Terminal. Can be an input or output.
3	4	S1	Source Terminal. Can be an input or output.
4	5	V_{SS}	Most Negative Power Supply Potential.
5	7	GND	Ground (0 V) Reference.
6	8	S4	Source Terminal. Can be an input or output.
7	9	D4	Drain Terminal. Can be an input or output.
8	10	IN4	Logic Control Input.
9	12	IN3	Logic Control Input.
10	13	D3	Drain Terminal. Can be an input or output.
11	14	S3	Source Terminal. Can be an input or output.
12	15	V_L	Logic Supply Voltage.
13	17	V_{DD}	Most Positive Power Supply Potential.
14	18	S2	Source Terminal. Can be an input or output.
15	19	D2	Drain Terminal. Can be an input or output.
16	20	IN2	Logic Control Input.
	1, 6, 11, 16	NIC	No Internal Connection.

Table 4. Truth Table

ADG211A In	**ADG212A In**	**Switch Condition**
0	1	On
1	0	Off

TYPICAL PERFORMANCE CHARACTERISTICS

The switches can comfortably operate anywhere in the 10 V to 15 V single or dual supply range, with only a slight degradation in performance. The following graphs show the relevant performance curves. The test circuits and test conditions are given in a following section, Test Circuits.

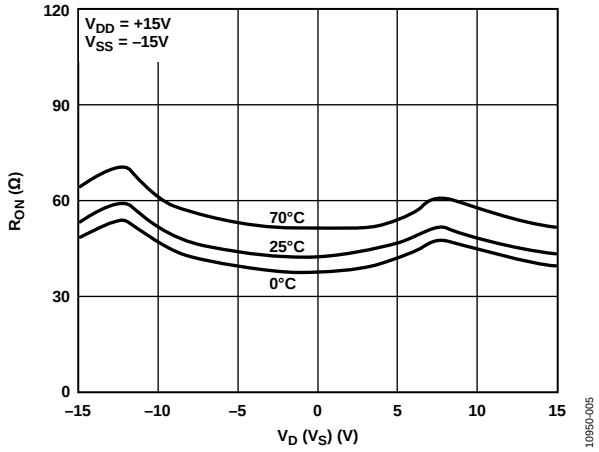


Figure 5. R_{ON} as a Function of V_D (V_S), Dual ±15 V Supplies

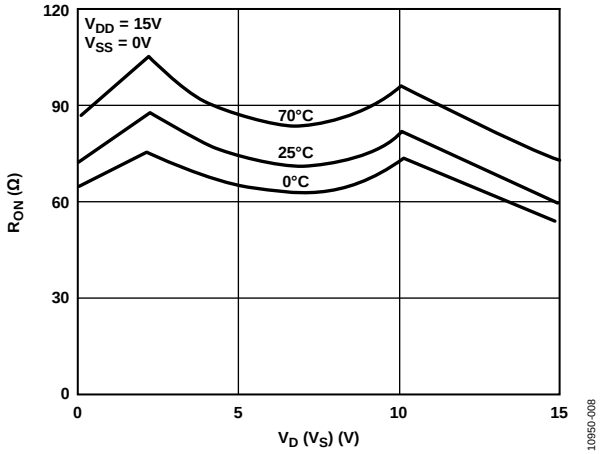


Figure 8. R_{ON} as a Function of V_D (V_S), Single +15 V Supply

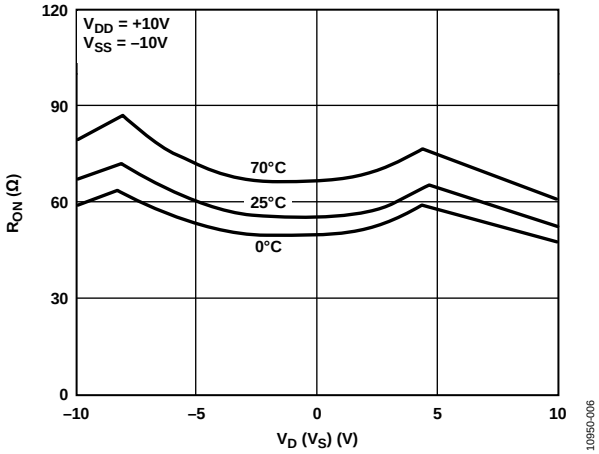


Figure 6. R_{ON} as a Function of V_D (V_S), Dual ±10 V Supplies

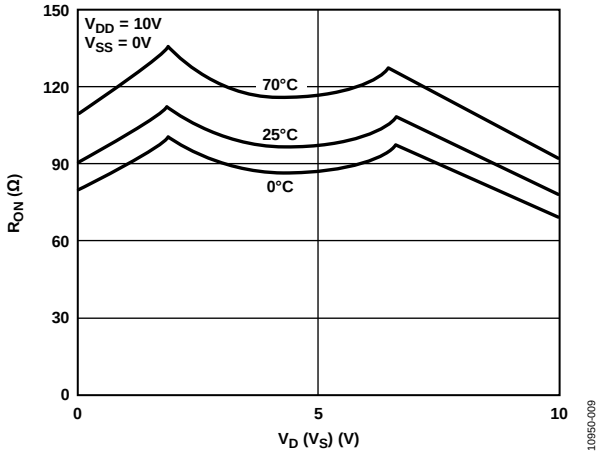


Figure 9. R_{ON} as a Function of V_D (V_S), Single +10 V Supply

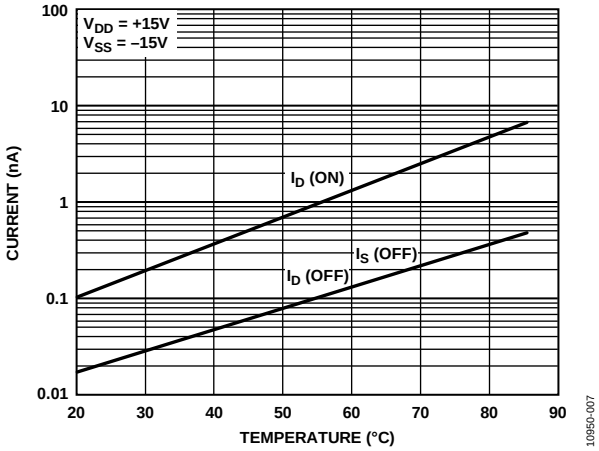


Figure 7. Leakage Current as a Function of Temperature (Note That Leakage Current Reduces as the Supply Voltages Reduce)

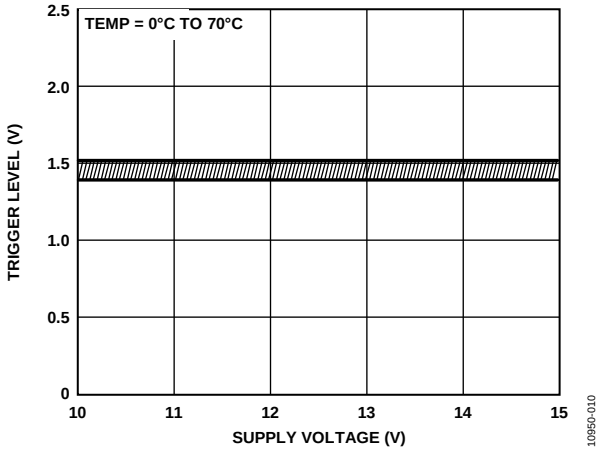


Figure 10. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply Voltage

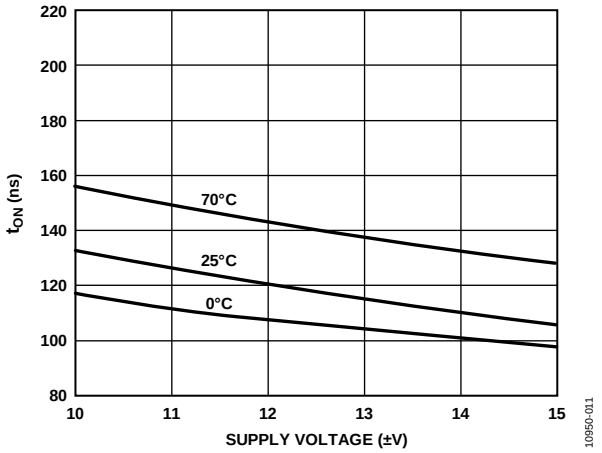


Figure 11. t_{ON} vs. Supply Voltage (Dual Supply)

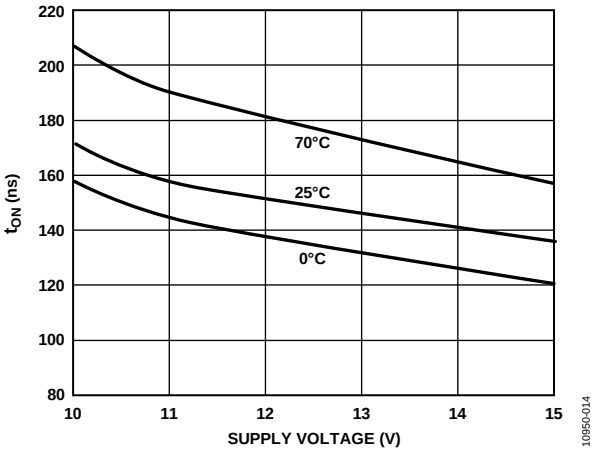


Figure 14. t_{ON} vs. Supply Voltage (Single Supply)

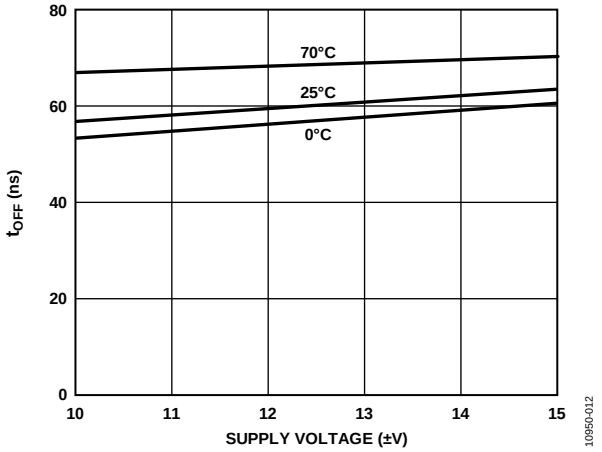


Figure 12. t_{OFF} vs. Supply Voltage (Dual Supply)

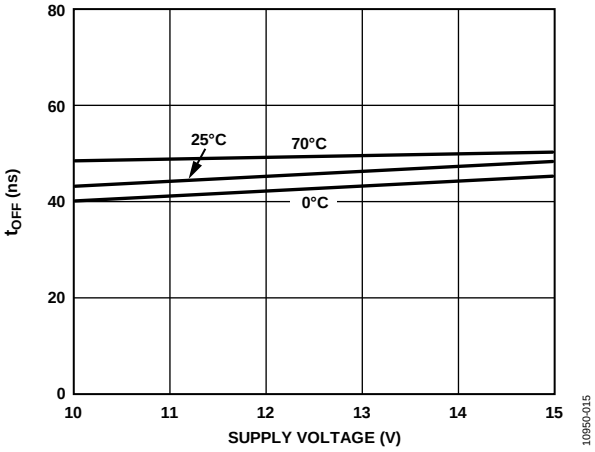


Figure 15. t_{OFF} vs. Supply Voltage (Single Supply)

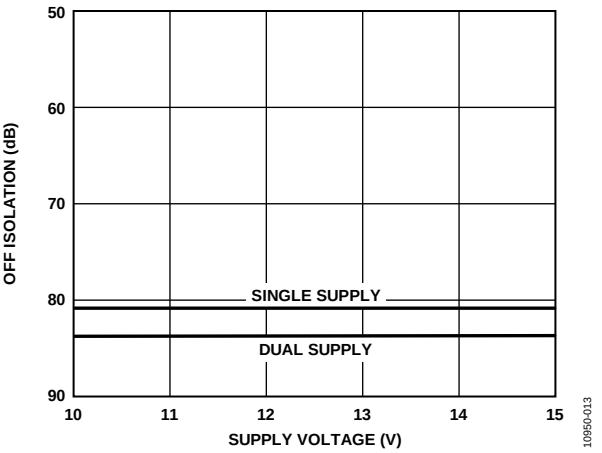


Figure 13. Off Isolation and Channel-to-Channel Crosstalk vs. Supply Voltage

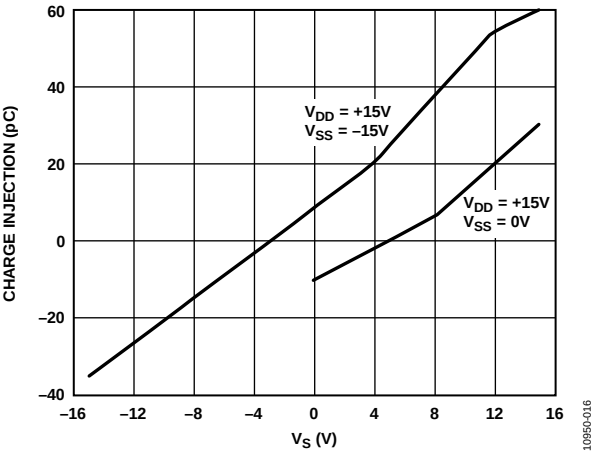


Figure 16. Charge Injection vs. Source Voltage (V_S) for Dual and Single 15 V Supplies

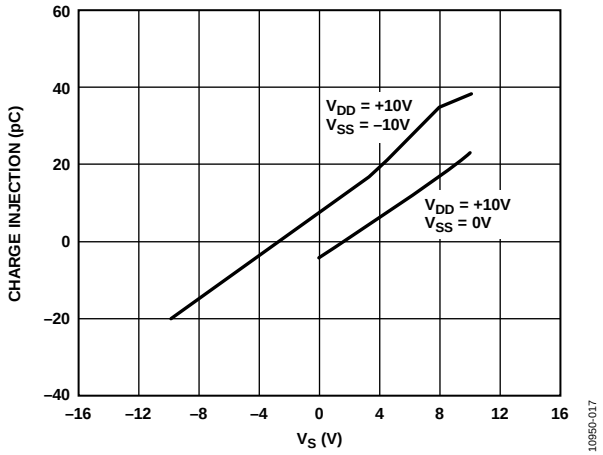


Figure 17. Charge Injection vs. Source Voltage for Dual and Single 10 V Supplies

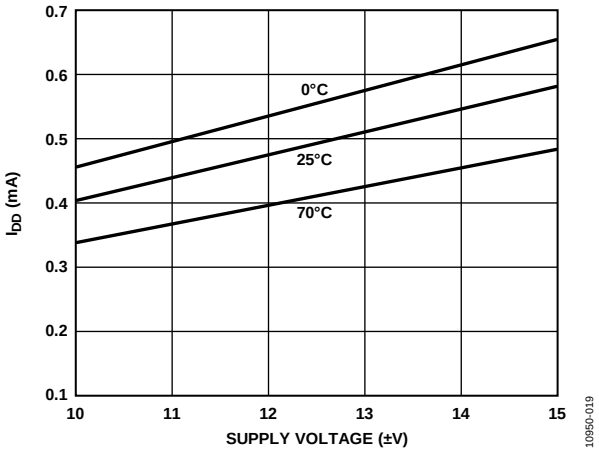


Figure 19. I_{DD} vs. Supply Voltage, (Dual Supply)

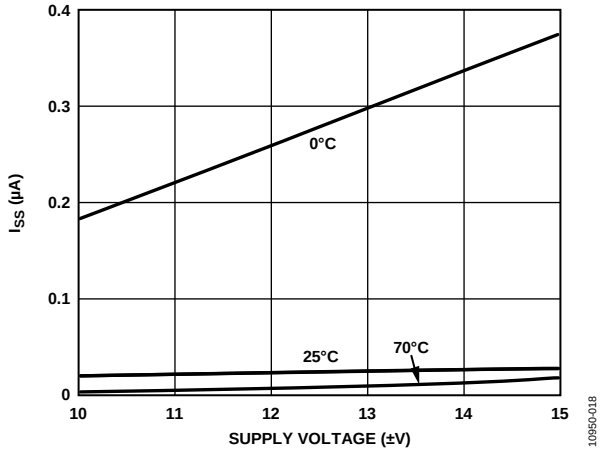


Figure 18. I_{SS} vs. Supply Voltage (Dual Supply)

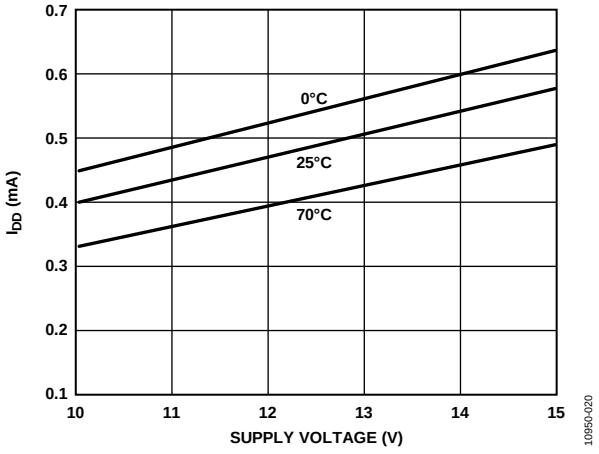


Figure 20. I_{DD} vs. Supply Voltage (Single Supply)

TERMINOLOGY

R_{ON}
Ohmic resistance between the out and S terminals.

R_{ON} Match
Difference between the R_{ON} of any two channels.

I_S (Off)
Source terminal leakage current when the switch is off.

I_D (Off)
Drain terminal leakage current when the switch is off.

I_D (On)
Leakage current that flows from the closed switch into the body.

V_D (V_S)
Analog voltage on the D, S terminals.

C_S (Off)
Switch input capacitance off condition.

C_D (Off)
Switch output capacitance off condition.

C_{IN}
Digital input capacitance.

C_D, C_S (On)
Input or output capacitance when the switch is on.

t_{ON}
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{OPEN}
Off time measured between 50% points of both switches, which are connected as a multiplexer when switching from one address state to another.

V_{INL}
Maximum input voltage for a logic low.

V_{INH}
Minimum input voltage for a logic high.

I_{INL} (I_{INH})
Input current of the digital input.

V_{DD}
Most positive voltage supply.

V_{SS}
Most negative voltage supply.

V_L
Logic supply voltage.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

TEST CIRCUITS

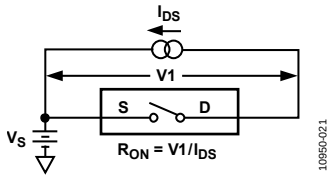


Figure 21.

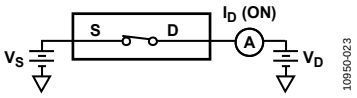


Figure 23.

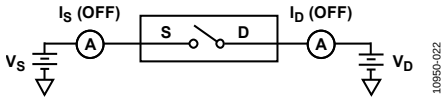
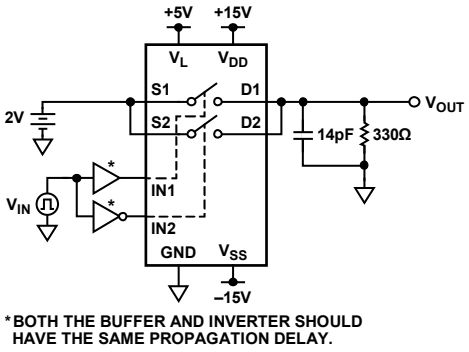


Figure 22.



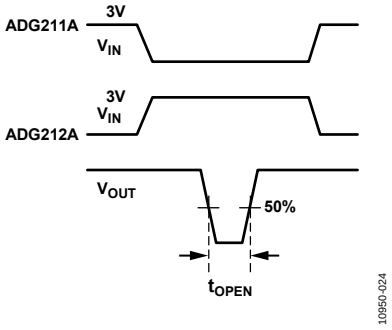
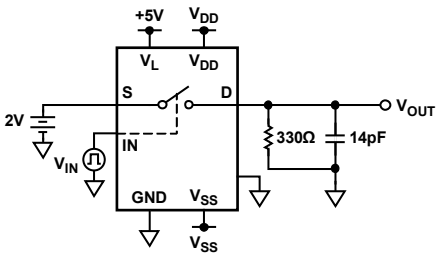


Figure 24.



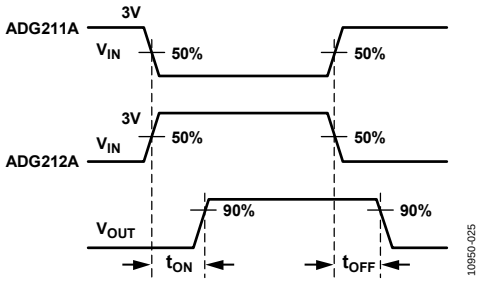


Figure 25.

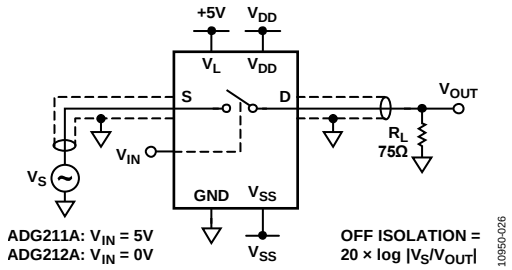


Figure 26. Off Isolation

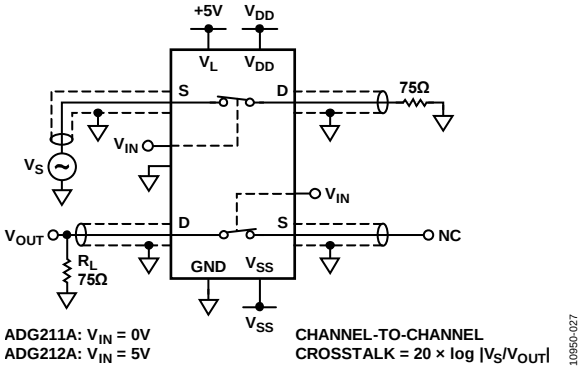


Figure 27. Channel-to-Channel Crosstalk

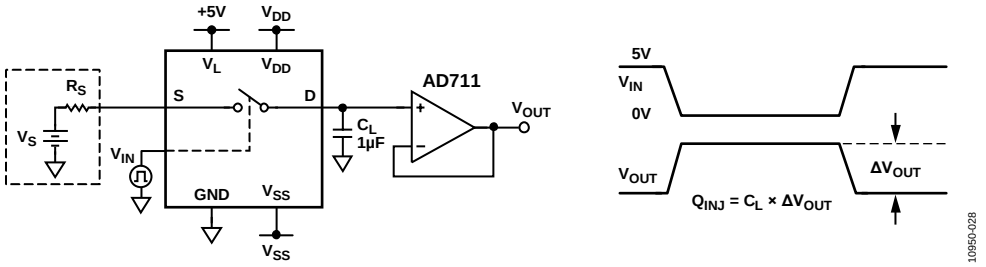
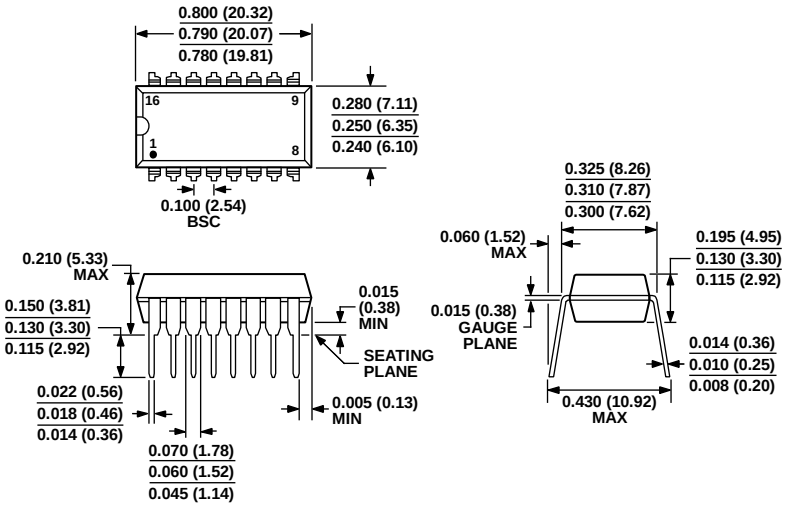


Figure 28. Charge Injection

OUTLINE DIMENSIONS

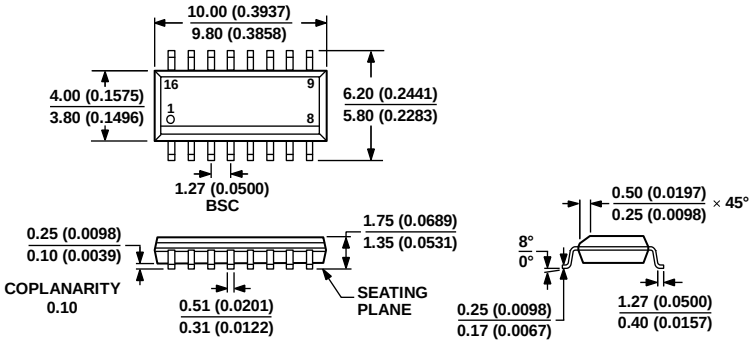


COMPLIANT TO JEDEC STANDARDS MS-001-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

073106-B

Figure 29. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches and (millimeters)

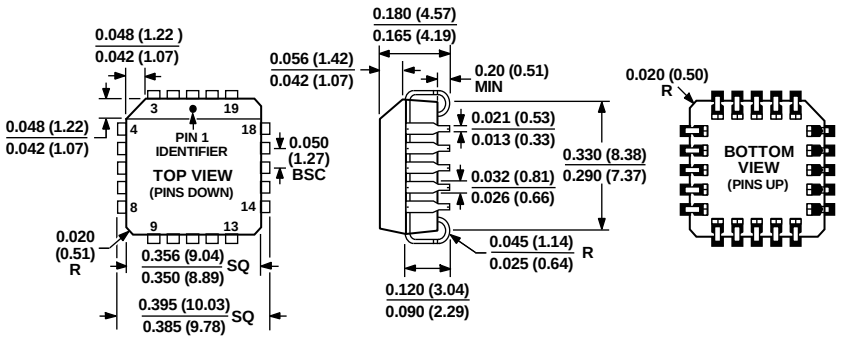


COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 30.16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-047-AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 31. 20-Lead Plastic Leaded Chip Carrier [PLCC] (P-20)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG211AKN	−40°C to +85°C	16-Lead PDIP	N-16
ADG211AKNZ	−40°C to +85°C	16-Lead PDIP	N-16
ADG211AKPZ	−40°C to +85°C	20-Lead PLCC	P-20
ADG211AKR	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG211AKRZ	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG211AKRZ-REEL	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG211AKRZ-REEL7	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG212AKNZ	−40°C to +85°C	16-Lead PDIP	N-16
ADG212AKPZ	−40°C to +85°C	20-Lead PLCC	P-20
ADG212AKPZ-REEL	−40°C to +85°C	20-Lead PLCC	P-20
ADG212AKR	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG212AKRZ	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG212AKRZ-REEL	−40°C to +85°C	16-Lead SOIC_N	R-16

[1] Z = RoHS Compliant Part.

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