REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make correction to the Output voltage differential test unit from “V” to “mV” as specified under Table I. - ro	14-12-02	C. SAFFLE
B	Add device type 02 and Single event phenomenon (SEP) requirements. Delete subgroup 9 from Group E end point electrical parameters as specified under Table IIA. - ro	16-09-27	C. SAFFLE

REV																				
SHEET																				
REV	B	B	B	B																
SHEET	15	16	17	18																

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
14-10-28

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, HIGH SPEED ECL CLOCK / DATA BUFFER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-13205**

SHEET 1 OF 18

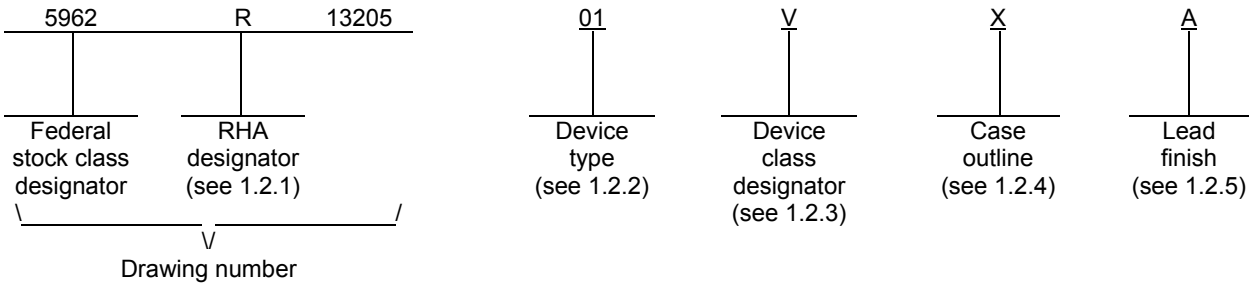
DSCC FORM 2233
APR 97

5962-E563-16

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADCLK925	High speed emitter coupled logic (ECL) clock / data buffer
02	ADCLK925	High speed emitter coupled logic (ECL) clock / data buffer

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP4-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Positive supply voltage (V_{CC}) – negative supply voltage (V_{EE}) ..... 6.0 V
Input voltage and input current:
Inputs D1, $\overline{D1}$ ..... V_{EE} – 0.5 V to V_{CC} + 0.5 V
Inputs D1, $\overline{D1}$ to center tap (V_T) pin :
(Current mode logic (CML) or positive emitter coupled logic (PECL) termination) .....±40 mA
Inputs D1 to $\overline{D1}$ ..... ±1.8 V
Maximum voltage on output pins ..... V_{CC} + 0.5 V
Maximum output current ..... 35 mA
Input termination, V_T to D1, $\overline{D1}$ ..... ±2 V
Voltage reference (V_{REF}) ..... V_{CC} – V_{EE}
Power dissipation (P_D) ..... 380 mW
Operating junction temperature (T_J) ..... 150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Thermal resistance, junction to case (θ_{JC}) ..... 125°C/W 2/
Thermal resistance, junction to ambient (θ_{JA}) ..... 132°C/W 2/

1.4 Recommended operating conditions.

Positive supply voltage (V_{CC}) – negative supply voltage (V_{EE}) ..... 3.3 V
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1.5 Operating performance characteristics.

Unless otherwise specified, T_A = +25°C, V_{CC} = V_{EE} = 3.3 V, output terminated to 50 Ω to (V_{CC} – 2.0 V).

Input capacitance (C_{IN}) – pins D1, $\overline{D1}$ ..... 1.0 pF
Propagation delay temperature coefficient ..... 50 fs/°C
Propagation delay skew (output to output) ..... 10 ps maximum
Random jitter ..... 60 fs rms maximum 3/
Power supply rejection ..... 3 ps/V 4/
Output Swing supply rejection ..... 26 dB 5/
Toggle rate V_{OD} differential at 7.5 GHz ..... 0.45 V_{PP} differential 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Measurement taken under absolute worst case conditions. Data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package θ_{JC} thermal numbers.
3/ V_{ID} = 1600 mV, 8 V/ns, V_{ICM} = 1.85 V.
4/ Change in t_{PD} per change in V_{CC}, V_{CC} - V_{EE} = 3.0V = ± 20%.
5/ Change in output swing per change in V_{CC}, V_{CC} - V_{EE} = 3.0V = ± 20%.
6/ V_{PP} differential is V_{OD} maximum – V_{OD} minimum, which is V_{PP} as measured by a differential probe.

1.5 Operating performance characteristics - continued.

Unless otherwise specified, T_A = +25°C, V_{CC} = V_{EE} = 3.3 V, output terminated to 50 Ω to (V_{CC} – 2.0 V).

Additive phase noise:

at 622.08 MHz, 10 Hz offset	-138 dBc/Hz
at 622.08 MHz, 100 Hz offset	-144 dBc/Hz
at 622.08 MHz, 1 kHz offset	-152 dBc/Hz
at 622.08 MHz, 10 kHz offset	-159 dBc/Hz
at 622.08 MHz, 100 kHz offset	-161 dBc/Hz
at 622.08 MHz, >1 MHz offset	-161 dBc/Hz
at 122.88 MHz, 10 Hz offset	-135 dBc/Hz
at 122.88 MHz, 100 Hz offset	-145 dBc/Hz
at 122.88 MHz, 1 kHz offset	-153 dBc/Hz
at 122.88 MHz, 10 kHz offset	-160 dBc/Hz
at 122.88 MHz, 100 kHz offset	-161 dBc/Hz
at 122.88 MHz, >1 MHz offset	-161 dBc/Hz

1.6 Radiation features.

Device type 01:

Maximum total dose available (dose rate = 50 – 300 rad(Si)/s) ..... 100 krad(Si) 7/

Device type 02:

Maximum total dose available (dose rate < 10 mrad(Si)/s) ..... 50 krad(Si) 8/

Single event phenomenon (SEP):

No single event latchup (SEL) occurs at effective linear energy transfer (LET) (see 4.4.4.2):

Device types 01 and 02 ..... ≤ 80 MeV/(cm^2/mg) 9/

7/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

8/ For device type 02, radiation end point limits for the noted parameters are guaranteed for the conditions specified in MIL-STD-883, method 1019, condition D.

9/ Limits are characterized at initial qualification and after any design or process changes that may affect the SEP characteristics, but are not production lot tested unless specified by the customer through the purchase order or contract. For more information on single event effect (SEE) test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $V_{CC} - V_{EE} = 3.3$ V, unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
DC input characteristics section.								
Input voltage high level	V_{IH}	$V_{ID} = V_{IH} - V_{IL}$, V_{IH}, V_{IL} applied during V_{OH}, V_{OL}, V_{OD} testing		1,2,3	01, 02	V_{EE} + 1.6	V_{CC}	V
			D,P,L,R	1	01	V_{EE} + 1.6	V_{CC}	
			D,P,L	1	02	V_{EE} + 1.6	V_{CC}	
Input voltage low level	V_{IL}	$V_{ID} = V_{IH} - V_{IL}$, V_{IH}, V_{IL} applied during V_{OH}, V_{OL}, V_{OD} testing		1,2,3	01, 02	V_{EE}	V_{CC} – 0.7	V
			D,P,L,R	1	01	V_{EE}	V_{CC} – 0.7	
			D,P,L	1	02	V_{EE}	V_{CC} – 0.7	
Input differential range	V_{ID}	$V_{ID} = V_{IH} - V_{IL}$, V_{IH}, V_{IL} applied during V_{OH}, V_{OL}, V_{OD} testing		1,2,3	01, 02	0.2	2.8	V_{P-P}
			D,P,L,R	1	01	0.2	2.8	
			D,P,L	1	02	0.2	2.8	
Input current, D, $\overline{D1}$	I_{IH}, I_{IL}	Open VT		1,2,3	01, 02		100	µA
			D,P,L,R	1	01		100	
			D,P,L	1	02		100	
Input resistance, single ended mode	R_{IN}			1,2,3	01, 02	45	58	Ω
			D,P,L,R	1	01	45	58	
			D,P,L	1	02	45	58	
Input resistance, differential mode	R_{IND}			1,2,3	01, 02	100	110	Ω
			D,P,L,R	1	01	100	110	
			D,P,L	1	02	100	110	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $V_{CC} - V_{EE} = 3.3$ V, unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
DC output characteristics.								
Output voltage high level	V_{OH}	4/		1,2	01, 02	V_{CC} – 1.26	V_{CC} – 0.76	V
				3		V_{CC} – 1.29	V_{CC} – 0.76	
			D,P,L,R	1	01	V_{CC} – 1.26	V_{CC} – 0.76	
			D,P,L	1	02	V_{CC} – 1.26	V_{CC} – 0.76	
Output voltage low level	V_{OL}	4/		1,2,3	01, 02	V_{CC} – 1.99	V_{CC} – 1.54	V
			D,P,L,R	1	01	V_{CC} – 1.99	V_{CC} – 1.54	
			D,P,L	1	02	V_{CC} – 1.99	V_{CC} – 1.54	
Output voltage differential	V_{OD}	4/		1,2,3	01, 02	610	1040	mV
			D,P,L,R	1	01	610	1040	
			D,P,L	1	02	610	1040	
Reference voltage, output voltage	V_{REF}	I_{REF} = 500 µA		1	01, 02	2.14	2.29	V
				2		2.05	2.35	
				3		2.10	2.40	
			D,P,L,R	1	01	2.14	2.29	
			D,P,L	1	02	2.14	2.29	
		I_{REF} = -500 µA		1	01, 02	1.90	2.05	
				2		1.80	2.10	
				3		1.85	2.15	
			D,P,L,R	1	01	1.90	2.05	
			D,P,L	1	02	1.90	2.05	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ $V_{CC} - V_{EE} = 3.3$ V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC output characteristics - continued.							
Reference voltage, output resistance	R_{REF}	$R_{REF} = V_{REF} / I_{REF}$, $I_{REF} = \pm 500\ \mu A$	1,2,3	01, 02	170	280	Ω
		D,P,L,R	1	01	170	280	
		D,P,L	1	02	170	280	
AC performance section.							
Propagation delay	t_{PD}	V_{CC} = 3.3 V ±10%, 5/ $V_{ICM} = V_{REF}$, V_{ID} = 0.5 V_{P-P}	9,10,11	01, 02	190	290	ps
Toggle rate	f_{min}	6/	4,5,6	01, 02	5		GHz
		> 0.6 V differential output 5/ swing, V_{CC} = 3.3 V ±10%			5		
		> 0.5 V differential output 5/ swing, V_{CC} = 3.3 V ±10 %			7		
Rise / fall time	t_R / t_F	Measured 20% to 80% 5/	9,10,11	01, 02	30	85	ps
Power supply section.							
Negative supply current	I_{VEE}	$V_{CC} - V_{EE}$ = 3.3 V ±10%	1,2,3	01, 02	-51		mA
		D,P,L,R	1	01	-51		
		D,P,L	1	02	-51		
Positive supply current	I_{VCC}	$V_{CC} - V_{EE}$ = 3.3 V ±10%	1,2,3	01, 02		97	mA
		D,P,L,R	1	01		97	
		D,P,L	1	02		97	

1/ Device type 01 supplied to this drawing has been characterized through all levels P, L, R of irradiation and tested at the "P, L and R" levels. Device type 02 has been characterized through levels P and L and is tested at the "L" level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A for device type 01 and condition D for device type 02. Device type 02 has been tested at low dose rate.

3/ Unless otherwise specified, $V_{CC} - V_{EE}$ = 3.3 V. Outputs terminated to 50 Ω to (V_{CC} – 2.0 V).

TABLE IA. Electrical performance characteristics - Continued.

4/ This test is terminated to 50 Ω to (V_{CC} – 2.0 V). Tested at (V_{CC}, V_{IH},V_{IL}): (3.3, 3.3, 0.0); (3.3, 1.75, 1.55); (2.5, 2.5, 0.0); (2.5, 1.35, 1.15); (2.375, 2.375, 0.0), (2.375, 1.73,1.53), (3.63, 1.9, 1.7).

5/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots. Parameter not tested post radiation.

6/ Functional automatic test equipment (ATE) production using nominal: V_{CC} / V_{EE} = 3.3 / 0.0 V, 50 Ω to 1.3 V termination, V_{ID} = 800 mV differential input swing. Detection level for V_{OD} > 712 mV differential output swing (-5.0 dBm).

TABLE IB. SEP test limits. 1/

Device types	SEP	Temperature T_C	Bias V_S	Linear energy transfer (LET)
01, 02	No SEL	+125°C	+4 V	LET≤ 80 MeV / (cm/mg^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

Device types	01, 02
Case outline	X
Terminal number	Terminal symbol
1	V_{REF}
2	V_T
3	D
4	$\overline{D}$
5	NC/GND
6	NC/GND
7	NC/GND
8	NC/GND
9	V_{EE}
10	V_{CC}
11	$\overline{Q2}$
12	Q2
13	$\overline{Q1}$
14	Q1
15	V_{CC}
16	V_{EE}

FIGURE 1. Terminal connections.

Terminal symbol	Description
D	Noninverting input.
$\overline{D}$	Inverting input.
NC/GND	No internal circuitry connected to NC/GND pins so user may ground pin if desired.
V_{EE}	Negative supply voltage.
V_{CC}	Positive supply voltage.
$\overline{Q2}$	Inverting output 2.
Q2	Noninverting output 2.
$\overline{Q1}$	Inverting output 1.
Q1	Noninverting output 1.
V_{REF}	Reference voltage. Reference voltage for biasing ac-coupled inputs.
V_T	Center tap. Venter tap of 100 Ω input resistor.

FIGURE 1. Terminal connections - continued.

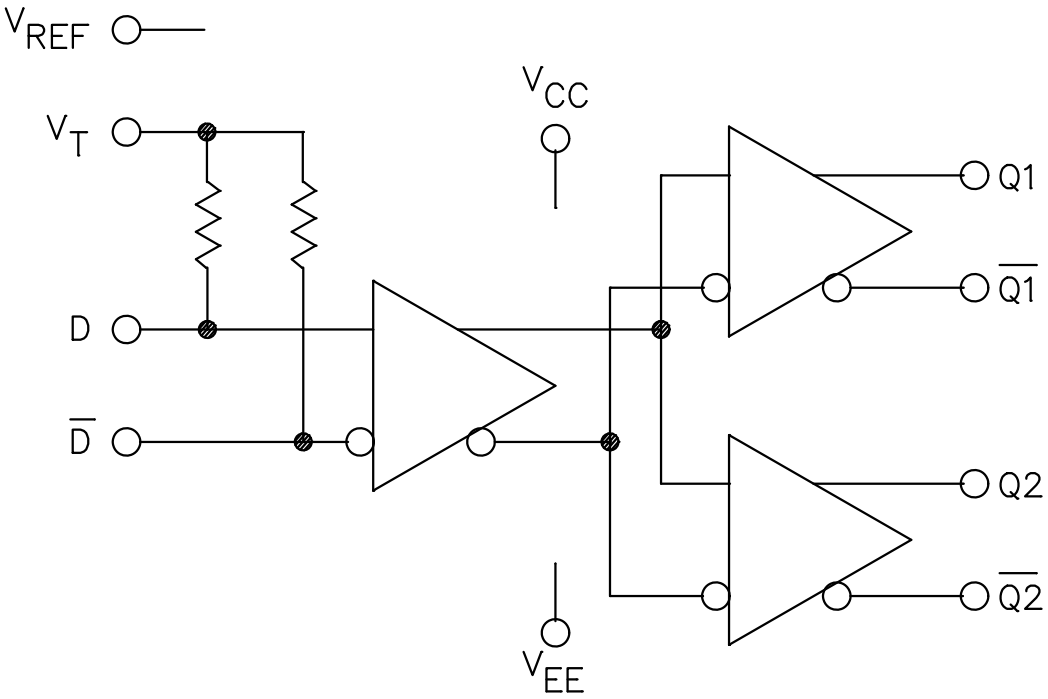


FIGURE 2. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 4, 5, 6, 9, 10, and 11 are tested as part of device initial characterization and after design and process changes or with subsequent wafer lots as indicated in Table IA.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3, 1/ 4,5,6,9,10,11	1,2,3, 1/ 2/ 3/ 4,5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3, 2/ 4,5,6,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3, 2/ 3/ 4,5,6,9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3, 2/ 4,5,6,9,10,11
Group E end-point electrical parameters (see 4.4)	1	1 2/

1/ PDA applies to subgroup 1.
2/ See table IA for parameters tested or characterized for subgroups 4, 5, 6, 9, 10, and 11.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/

Parameters	Symbol	Delta limits	Units
Negative supply current	I_{VEE}	±1	mA
Positive supply current	I_{VCC}	±1	mA
Output voltage high level	V_{OH}	±0.05	V
Output voltage low level	V_{OL}	±0.05	V
Output voltage differential	V_{OD}	±0.05	V
Input resistance, single ended mode	R_{IN}	±2	Ω
Input resistance, differential mode	R_{IND}	±2	Ω

1/ If device is tested at or below delta limit in table, no deltas are required. Deltas are performed at room temperature.
2/ Delta parameters are performed at $V_{CC} - V_{EE}$ = 3.3 V.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and condition D for device type 02, and as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0◦ ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +125°C and the maximum rated operating temperature ±10°C for single event latchup testing.

f. Bias conditions shall be V_S = +4 V for latchup measurements.

g. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Occurrence of single evnet latchup (SEL).

6.8 Application notes.

6.8.1 Power / ground layout and bypassing. The subject device buffers are designed for very high speed applications. Consequently, high speed design techniques must be used to achieve the specified performance. It is critically important to use low impedance supply planes for both the negative supply (V_{EE}) and the positive supply (V_{CC}) planes as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.
It is also important to adequately bypass the input and output supplies. A 1 μF electrolytic bypass capacitor should be placed within several inches of each power supply pin to ground. In addition, multiple high quality 0.001 μF bypass capacitors should be placed as close as possible to each of the V_{EE} and V_{CC} supply pins and should be connected to the GND plane with redundant vias. High frequency bypass capacitors should be carefully selected for minimum inductance and equivalent series resistance (ESR). Parasitic layout inductance should be strictly avoided to maximize the effectiveness of the bypass at high frequencies.

6.8.2 Output stages. The specified performance can be achieved only by using proper transmission line terminations. The outputs of the buffers are designed to directly drive 800 mV into 50 Ω cable or microstrip / stripline transmission lines terminated with 50 Ω referenced to V_{CC} − 2 V. The output stage is shown in figure 3. The outputs are designed for best transmission line matching. If high speed signals must be routed more than a centimeter, either the microstrip or the stripline technique is required to ensure proper transition times and to prevent excessive output ringing and pulse width-dependent propagation delay dispersion.

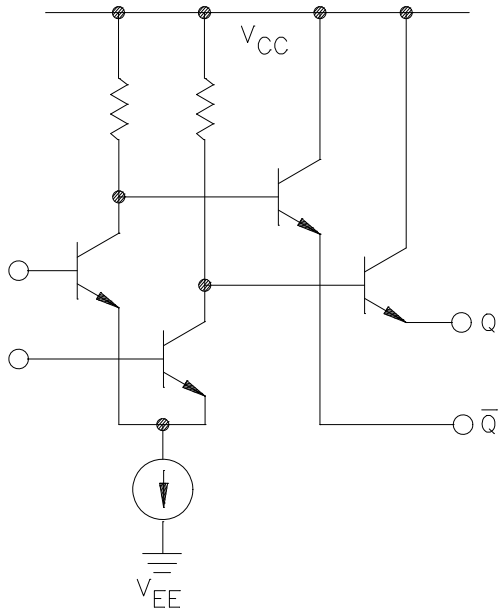


FIGURE 3. Simplified schematic diagram of the output stage.

6.8.3 Optimizing high speed performance. As with any high speed circuit, proper design and layout techniques are essential to obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and cause oscillation. Discontinuities along input and output transmission lines can also severely limit the specified jitter performance by reducing the effective input slew rate.
In a 50 Ω environment, input and output matching have a significant impact on performance. The buffer provides internal 50 Ω termination resistors for both D and $\overline{D}$ inputs. The return side should normally be connected to the reference pin provided. The termination potential should be carefully bypassed, using ceramic capacitors to prevent undesired aberrations on the input signal due to parasitic inductance in the termination return path. If the inputs are directly coupled to a source, care must be taken to ensure the pins are within the rated input differential and common-mode ranges. If the return is floated, the device exhibits 100 Ω cross termination, but the source must then control the common-mode voltage and supply the input bias currents. There are electrostatic discharge (ESD)/clamp diodes between the input pins to prevent the application of excessive offsets to the input transistors. ESD diodes are not optimized for best ac performance. When a clamp is desired, it is recommended that appropriate external diodes be used.

6.8.4 Buffer random jitter. The device is specifically designed to minimize added random jitter over a wide input slew rate range. Provided sufficient voltage swing is present, random jitter is affected most by the slew rate of the input signal. Whenever possible, excessively large input signals should be clamped with fast Schottky diodes because attenuators reduce the slew rate. Input signal runs of more than a few centimeters should be over low loss dielectrics or cables with good high frequency characteristics.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-09-27

Approved sources of supply for SMD 5962-13205 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1320501VXA	24355	ADCLK925AF/QMLR
5962L1320502VXA	24355	ADCLK925AF/QMLL

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Greensboro, NC 27409-9605

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.