Low Voltage 1.65 V to 3.6 V, Bidirectional Logic Level Translation, Bypass Switch

Data Sheet **ADG3233**

FEATURES

Operates from 1.65 V to 3.6 V supply rails
Bidirectional level translation, unidirectional signal path
8-lead SOT-23 and MSOP packages
Bypass or normal operation
Short circuit protection

APPLICATIONS

JTAG chain bypassing
Daisy-chain bypassing
Digital switching

FUNCTIONAL BLOCK DIAGRAM

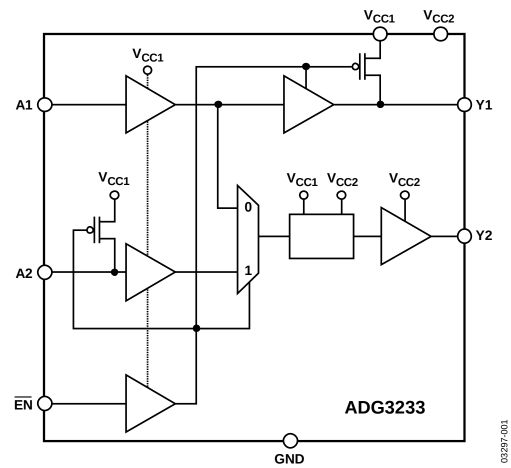

Figure 1.

GENERAL DESCRIPTION

The ADG3233[1] is a bypass switch designed on a submicron process that operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages, allowing bidirectional level translation, that is, it translates low voltages to higher voltages and vice versa. The signal path is unidirectional, meaning data may only flow from A → Y.

This type of device may be used in applications that require a bypassing function. It is ideally suited to bypassing devices in a JTAG chain or in a daisy-chain loop. One switch could be used for each device or a number of devices, thus allowing easy bypassing of one or more devices in a chain. This may be particularly useful in reducing the time overhead in testing devices in the JTAG chain or in daisy-chain applications where the user does not wish to change the settings of a particular device.

The bypass switch is packaged in two of the smallest footprints available for its required pin count. The 8-lead SOT-23 package requires only 2.9 mm × 2.8 mm board space, while the MSOP package occupies approximately 3 mm × 4.9 mm board area.

PRODUCT HIGHLIGHTS

1. Bidirectional level translation matches any voltage level from 1.65 V to 3.6 V.
2. The bypass switch offers high performance and is fully guaranteed across the supply range.
3. Short circuit protection.
4. Tiny 8-lead SOT-23 package and 8-lead MSOP.

Table 1. Truth Table

$\overline{EN}$	Signal Path	Function
L	A1 → Y2, Y1 → V_{CC1}	Enable bypass mode
H	A1 → Y1, A2 → Y2	Enable normal mode

[1] U.S. Patent Number: 7,369,385 B2.

Rev. B Document Feedback

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REVISION HISTORY

7/13—Rev. A to Rev. B

Changes to Table 1 ... 1

7/11—Rev. 0 to Rev. A

Changes to Patent Number, General Description Section, and Product Highlights Section ... 1
Changes to $V_{CC} = V_{CC1} = V_{CC2} = 2.5$ V ± 0.2 V, ENABLE Time $\overline{EN} \rightarrow$ Y1, Table 2 ... 4
Changes to Table 3 ... 6
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 16

5/03—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC1} = V_{CC2} = 1.65$ V to 3.6 V, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ[2]	Max	Unit
LOGIC INPUTS/OUTPUTS[3]		$V_{CC2} = 1.65$ V to 3.6 V, GND = 0 V				
Input High Voltage[4]	V_{IH}	$V_{CC1} = 3.0$ V to 3.6 V	1.35			V
		$V_{CC1} = 2.3$ V to 2.7 V	1.35			V
		$V_{CC1} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$			V
Input Low Voltage[4]	V_{IL}	$V_{CC1} = 3.0$ V to 3.6 V			0.8	V
		$V_{CC1} = 2.3$ V to 2.7 V			0.7	V
		$V_{CC1} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$	V
Output High Voltage (Y1)	V_{OH}	$I_{OH} = -100$ µA, $V_{CC1} = 3.0$ V to 3.6 V	2.4			V
		$I_{OH} = -100$ µA, $V_{CC1} = 2.3$ V to 2.7 V	2.0			V
		$I_{OH} = -100$ µA, $V_{CC1} = 1.65$ V to 1.95 V	$V_{CC} - 0.45$			V
		$I_{OH} = -4$ mA, $V_{CC1} = 2.3$ V to 2.7 V	2.0			V
		$I_{OH} = -4$ mA, $V_{CC1} = 1.65$ V to 1.95 V	$V_{CC} - 0.45$			V
		$I_{OH} = -8$ mA, $V_{CC1} = 3.0$ V to 3.6 V	2.4			V
Output Low Voltage (Y1)	V_{OL}	$I_{OL} = 100$ µA, $V_{CC1} = 3.0$ V to 3.6 V			0.40	V
		$I_{OL} = 100$ µA, $V_{CC1} = 2.3$ V to 2.7 V			0.40	V
		$I_{OL} = 100$ µA, $V_{CC1} = 1.65$ V to 1.95 V			0.45	V
		$I_{OL} = 4$ mA, $V_{CC1} = 2.3$ V to 2.7 V			0.40	V
		$I_{OL} = 4$ mA, $V_{CC1} = 1.65$ V to 1.95 V			0.45	V
		$I_{OL} = 8$ mA, $V_{CC1} = 3.0$ V to 3.6 V			0.40	V
LOGIC OUTPUTS[3]		$V_{CC1} = 1.65$ V to 3.6 V, GND = 0 V				
Output High Voltage (Y2)	V_{OH}	$I_{OH} = -100$ µA, $V_{CC2} = 3.0$ V to 3.6 V	2.4			V
		$I_{OH} = -100$ µA, $V_{CC2} = 2.3$ V to 2.7 V	2.0			V
		$I_{OH} = -100$ µA, $V_{CC2} = 1.65$ V to 1.95 V	$V_{CC} - 0.45$			V
		$I_{OH} = -4$ mA, $V_{CC2} = 2.3$ V to 2.7 V	2.0			V
		$I_{OH} = -4$ mA, $V_{CC2} = 1.65$ V to 1.95 V	$V_{CC} - 0.45$			V
		$I_{OH} = -8$ mA, $V_{CC2} = 3.0$ V to 3.6 V	2.4			V
Output Low Voltage (Y2)	V_{OL}	$I_{OL} = 100$ µA, $V_{CC2} = 3.0$ V to 3.6 V			0.40	V
		$I_{OL} = 100$ µA, $V_{CC2} = 2.3$ V to 2.7 V			0.40	V
		$I_{OL} = 100$ µA, $V_{CC2} = 1.65$ V to 1.95 V			0.45	V
		$I_{OL} = 4$ mA, $V_{CC2} = 2.3$ V to 2.7 V			0.40	V
		$I_{OL} = 4$ mA, $V_{CC2} = 1.65$ V to 1.95 V			0.45	V
		$I_{OL} = 8$ mA, $V_{CC2} = 3.0$ V to 3.6 V			0.40	V
SWITCHING CHARACTERISTICS[4, 5]						
$V_{CC} = V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 0.3$ V						
Propagation Delay, t_{PD}						
A1 → Y1 Normal Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		3.5	5.4	ns
A2 → Y2 Normal Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		3.5	5.4	ns
A1 → Y2 Bypass Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		4	6.5	ns
ENABLE Time $\overline{EN}$ → Y1	$t_{\overline{EN}}$	$C_L = 30$ pF, $V_T = V_{CC}/2$		4	6	ns
DISABLE Time $\overline{EN}$ → Y1	t_{DIS}	$C_L = 30$ pF, $V_T = V_{CC}/2$		2.8	4	ns
ENABLE Time $\overline{EN}$ → Y2	$t_{\overline{EN}}$	$C_L = 30$ pF, $V_T = V_{CC}/2$		4.5	6.5	ns
DISABLE Time $\overline{EN}$ → Y2	t_{DIS}	$C_L = 30$ pF, $V_T = V_{CC}/2$		4	6.5	ns

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ[2]	Max	Unit
$V_{CC} = V_{CC1} = V_{CC2} = 2.5\ V \pm 0.2\ V$						
Propagation Delay, t_{PD}						
A1 → Y1 Normal Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		4.5	6.2	ns
A2 → Y2 Normal Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		4.5	6.2	ns
A1 → Y2 Bypass Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		4.5	6.5	ns
ENABLE Time $\overline{EN}$ → Y1	$t_{\overline{EN}}$	$C_L = 30$ pF, $V_T = V_{CC}/2$		5	7.2	ns
DISABLE Time $\overline{EN}$ → Y1	t_{DIS}	$C_L = 30$ pF, $V_T = V_{CC}/2$		3.2	4.7	ns
ENABLE Time $\overline{EN}$ → Y2	$t_{\overline{EN}}$	$C_L = 30$ pF, $V_T = V_{CC}/2$		5	7.7	ns
DISABLE Time $\overline{EN}$ → Y2	t_{DIS}	$C_L = 30$ pF, $V_T = V_{CC}/2$		4.8	7.2	ns
$V_{CC} = V_{CC1} = V_{CC2} = 1.8\ V \pm 0.15\ V$						
Propagation Delay, t_{PD}						
A1 → Y1 Normal Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		6.7	10	ns
A2 → Y2 Normal Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		6.5	10	ns
A1 → Y2 Bypass Mode	t_{PHL}, t_{PLH}	$C_L = 30$ pF, $V_T = V_{CC}/2$		6.5	10.25	ns
ENABLE Time $\overline{EN}$ → Y1	$t_{\overline{EN}}$	$C_L = 30$ pF, $V_T = V_{CC}/2$		7	10.5	ns
DISABLE Time $\overline{EN}$ → Y1	t_{DIS}	$C_L = 30$ pF, $V_T = V_{CC}/2$		4.4	6.5	ns
ENABLE Time $\overline{EN}$ → Y2	$t_{\overline{EN}}$	$C_L = 30$ pF, $V_T = V_{CC}/2$		7	12	ns
DISABLE Time $\overline{EN}$ → Y2	t_{DIS}	$C_L = 30$ pF, $V_T = V_{CC}/2$		6.5	10.5	ns
Input Leakage Current	I_I	$0 \le V_{IN} \le 3.6$ V			±1	µA
Output Leakage Current	I_O	$0 \le V_{IN} \le 3.6$ V			±1	µA
POWER REQUIREMENTS						
Power Supply Voltages	V_{CC1}		1.65		3.6	V
	V_{CC2}		1.65		3.6	V
Quiescent Power Supply Current	I_{CC1}	Digital inputs = 0 V or V_{CC}			2	µA
	I_{CC2}	Digital inputs = 0 V or V_{CC}			2	µA
Increase in I_{CC} per Input	ΔI_{CC1}	$V_{CC} = 3.6$ V, one input at 3.0 V; others at V_{CC} or GND			0.75	µA

[1] Temperature range is as follows: B Version: −40°C to +85°C.
[2] All typical values are at $V_{CC} = V_{CC1} = V_{CC2}$, $T_A = 25$°C, unless otherwise stated.
[3] V_{IL} and V_{IH} levels are specified with respect to V_{CC1}, V_{OH}, and V_{OL} levels for Y1 are specified with respect to V_{CC1}, and V_{OH}, and V_{OL} levels are specified for Y2 with respect to V_{CC2}.
[4] Guaranteed by design, not subject to production test.
[5] See the Test Waveforms section.

TEST WAVEFORMS

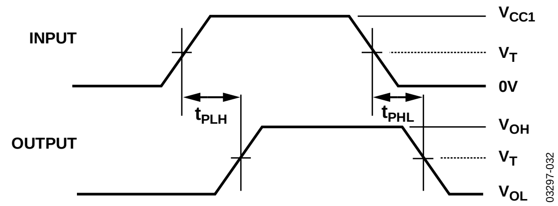

Figure 2. Propagation Delay

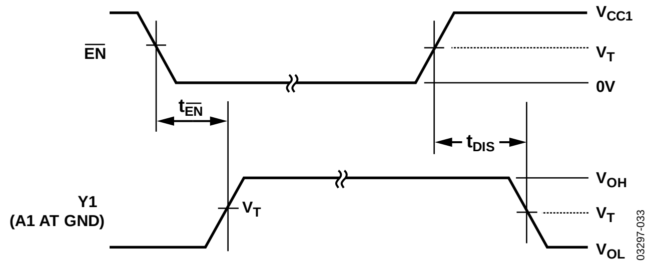

Figure 3. Y1 Enable and Disable Times

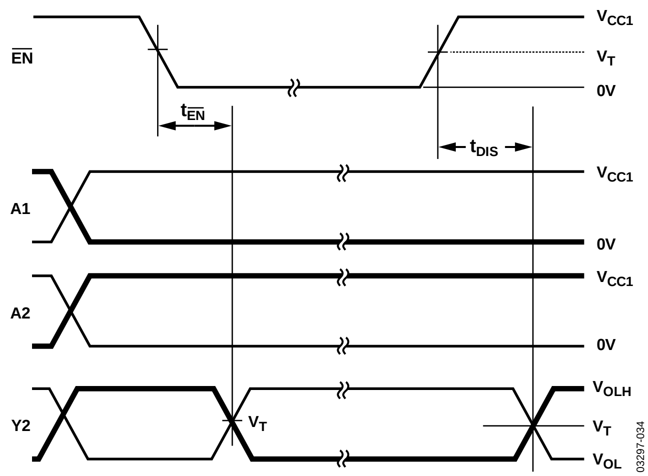

Figure 4. Y2 Enable and Disable Times

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.3 V to +4.6 V
Digital Inputs to GND	−0.3 V to +4.6 V
A1, $\overline{EN}$	−0.3 V to +4.6 V
A2	−0.3 V to V_{CC1} + 0.3 V
DC Output Current	25 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
8-Lead MSOP	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	43°C/W
8-Lead SOT-23	
θ_{JA} Thermal Impedance	211°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C
Soldering (Pb-Free)	
Reflow, Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

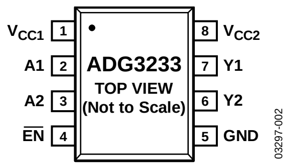

Figure 5. 8-Lead SOT-23 Package (RJ-8)

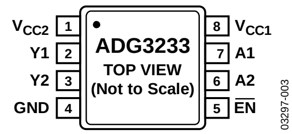

Figure 6. 8-Lead MSOP Package (RM-8)

Table 4. Pin Function Descriptions

Pin No.			
RJ-8	**RM-8**	**Mnemonic**	**Description**
1	8	V_{CC1}	Supply Voltage 1, can be any supply voltage from 1.65 V to 3.6 V.
8	1	V_{CC2}	Supply Voltage 2, can be any supply voltage from 1.65 V to 3.6 V.
2	7	A1	Input Referred to V_{CC1}.
3	6	A2	Input Referred to V_{CC2}.
7	2	Y1	Output Referred to V_{CC1}.
6	3	Y2	Output Referred to V_{CC2}. Voltage levels appearing at Y2 will be translated from a V_{CC1} voltage level to a V_{CC2} voltage level.
4	5	$\overline{EN}$	Active Low Device Enable. When low, bypass mode is enabled; when high, the device is in normal mode.
5	4	GND	Device Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

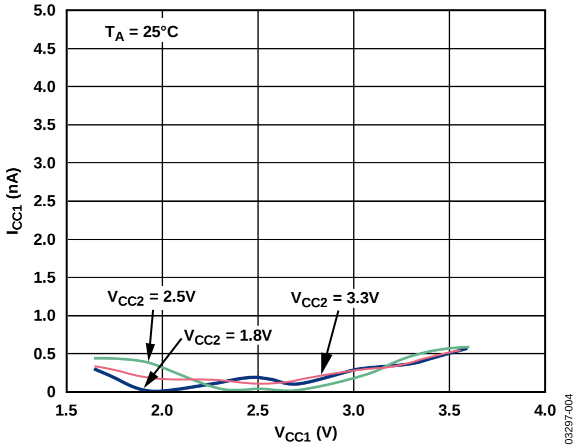

Figure 7. I_{CC1} vs. V_{CC1}

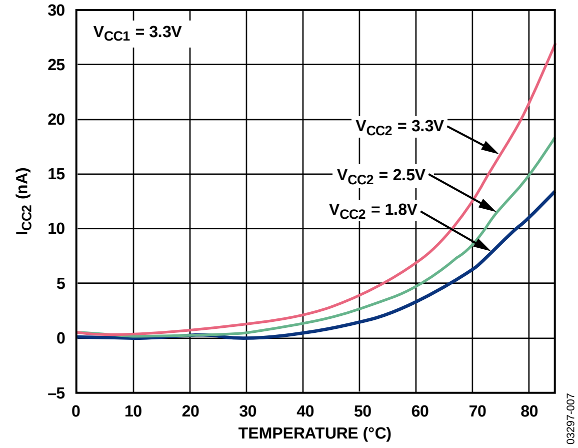

Figure 10. I_{CC2} vs. Temperature

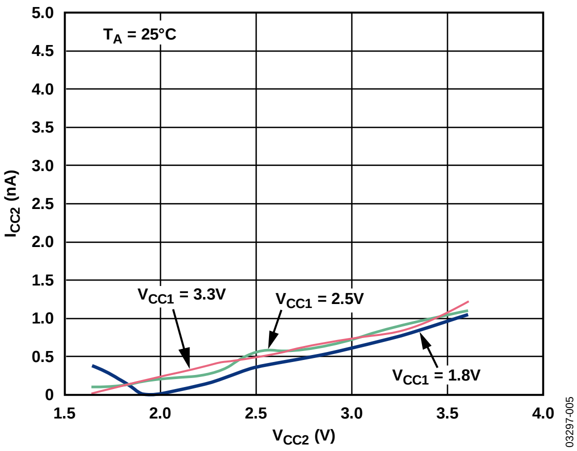

Figure 8. I_{CC2} vs. V_{CC2}

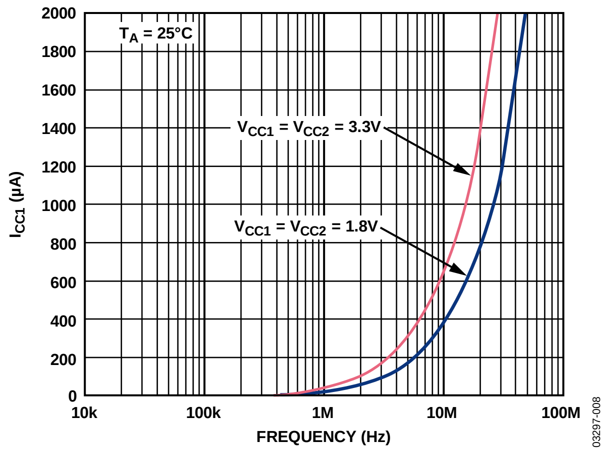

Figure 11. I_{CC1} vs. Frequency, Normal Mode

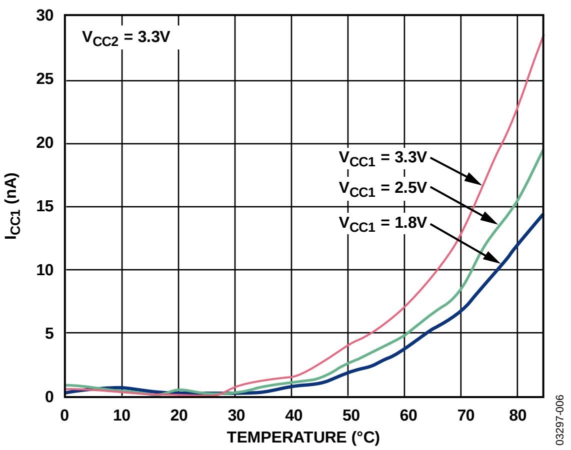

Figure 9. I_{CC1} vs. Temperature

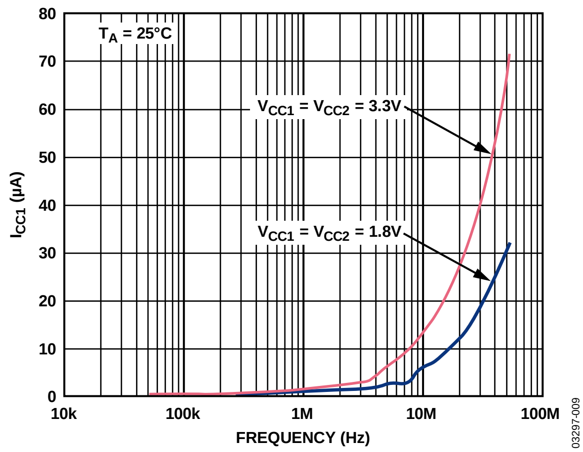

Figure 12. I_{CC1} vs. Frequency, Bypass Mode

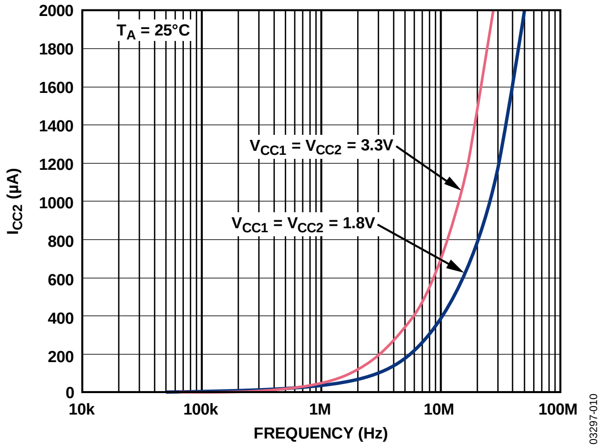

Figure 13. I_{CC2} vs. Frequency, Normal Mode

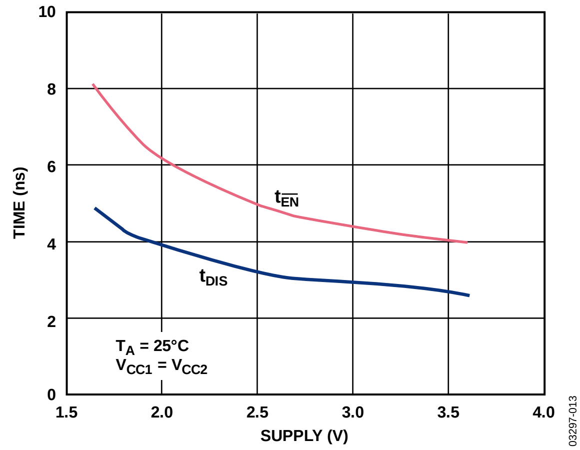

Figure 16. Y2 Enable, Disable Time vs. Supply

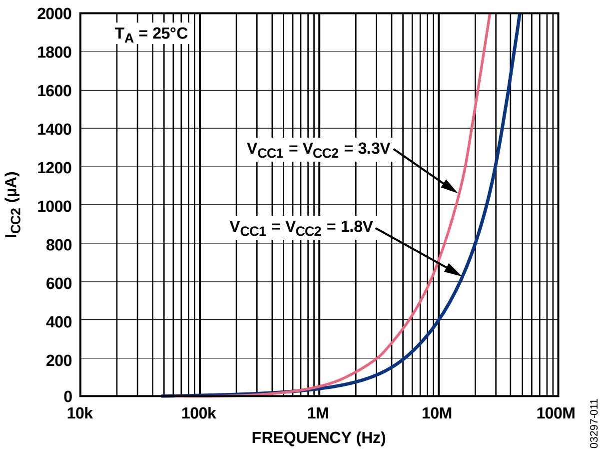

Figure 14. I_{CC2} vs. Frequency, Bypass Mode

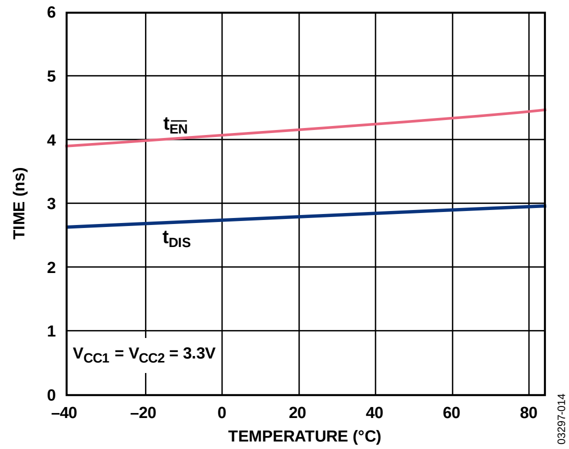

Figure 17. Y1 Enable, Disable Time vs. Temperature

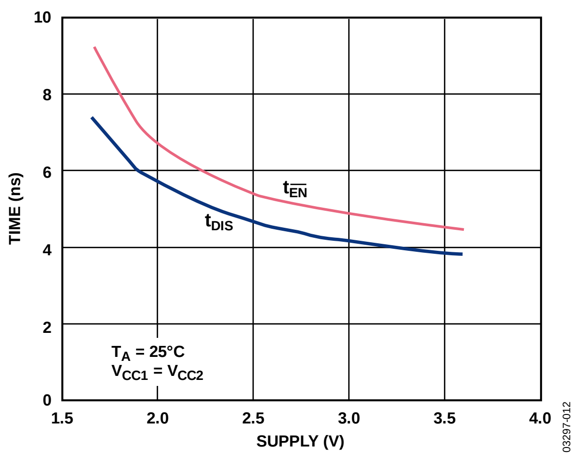

Figure 15. Y1 Enable, Disable Time vs. Supply

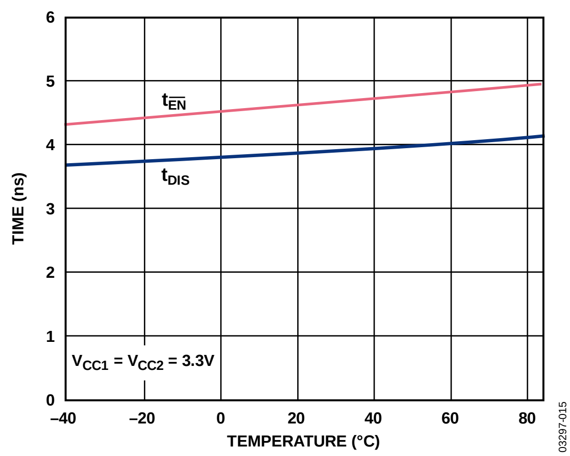

Figure 18. Y2 Enable, Disable Time vs. Temperature

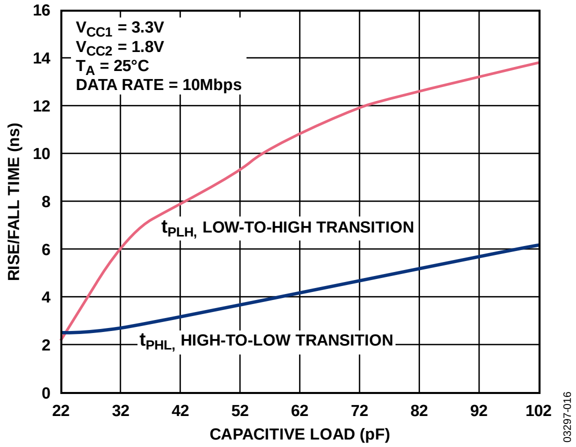

Figure 19. Rise/Fall Time vs. Capacitive Load, A1 → Y1, A2 → Y2

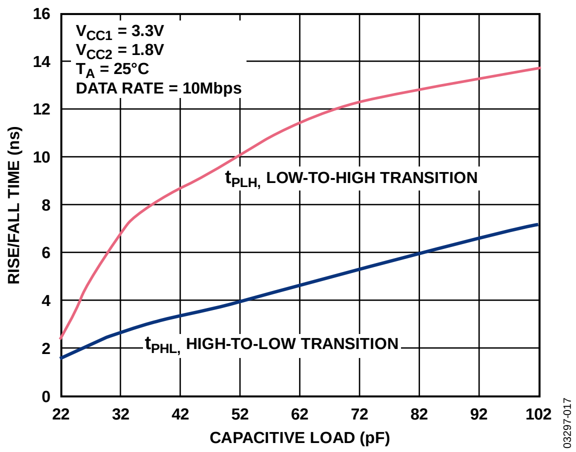

Figure 20. Rise/Fall Time vs. Capacitive Load, A1 → Y2, Bypass Mode

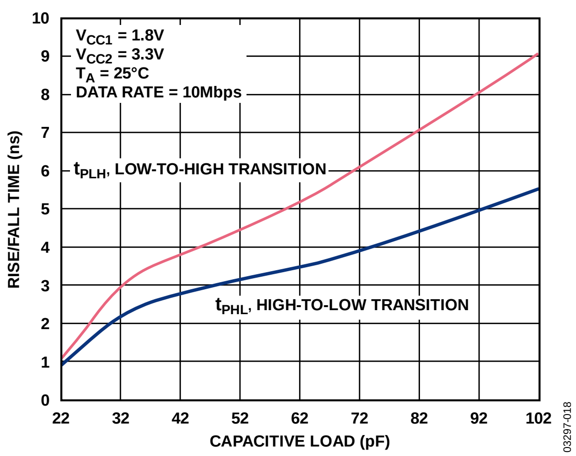

Figure 21. Rise/Fall Time vs. Capacitive Load, A1 → Y1, A2 → Y2

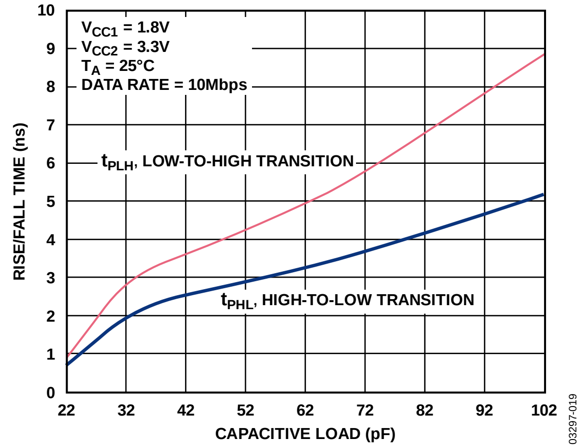

Figure 22. Rise/Fall Time vs. Capacitive Load, A1 → Y2, Bypass Mode

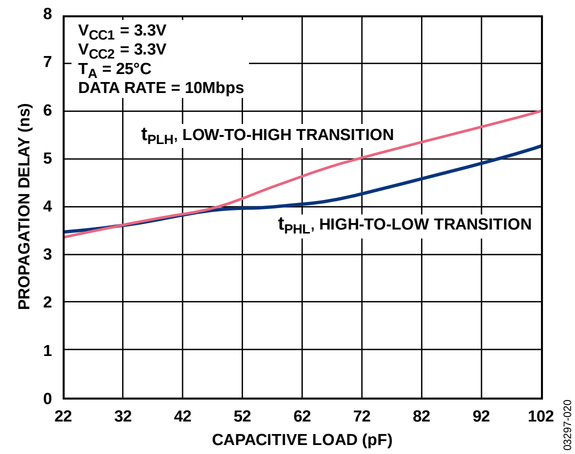

Figure 23. Propagation Delay vs. Capacitive Load A1 → Y1

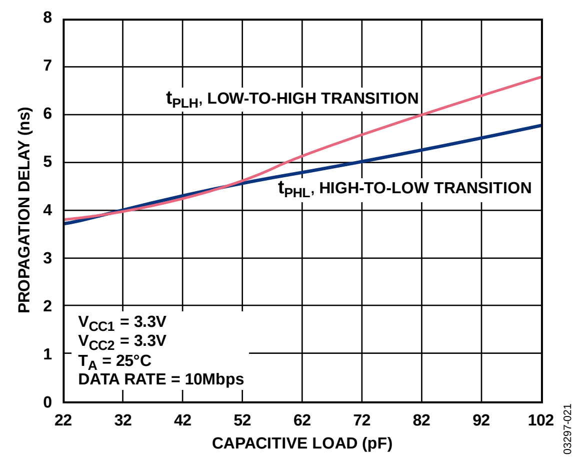

Figure 24. Propagation Delay vs. Capacitive Load A2 → Y2

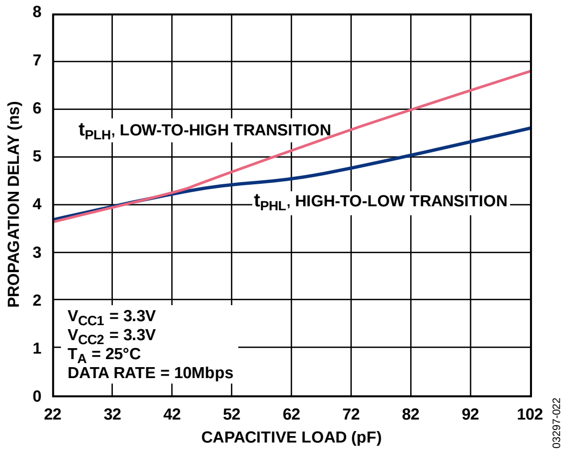

Figure 25. Propagation Delay vs. Capacitive Load A1 → Y2, Bypass Mode

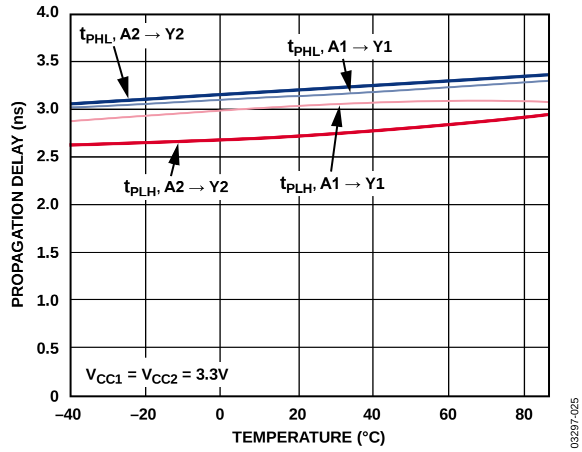

Figure 28. Propagation Delay vs. Temperature, Normal Mode

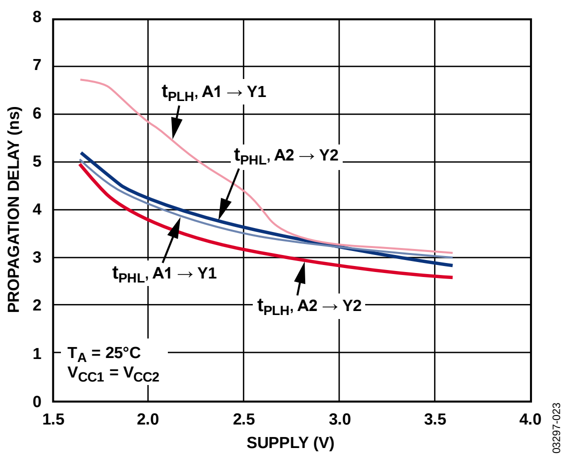

Figure 26. Propagation Delay vs. Supply, Normal Mode

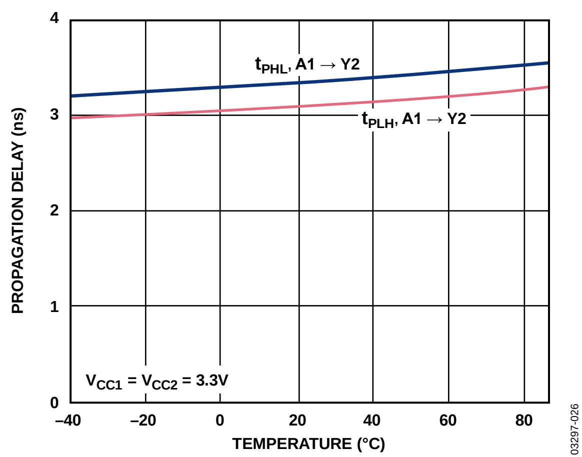

Figure 29. Propagation Delay vs. Temperature, Bypass Mode

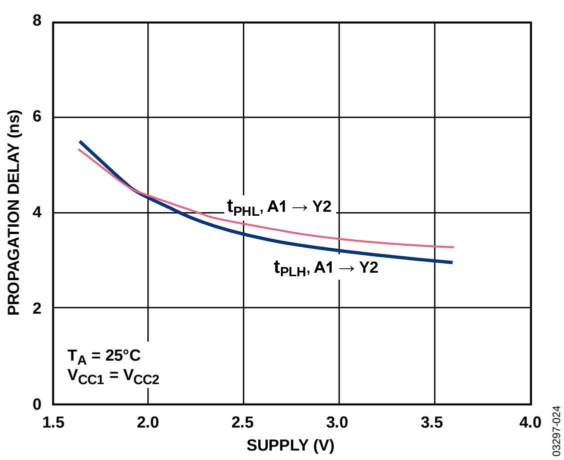

Figure 27. Propagation Delay vs. Supply, Bypass Mode

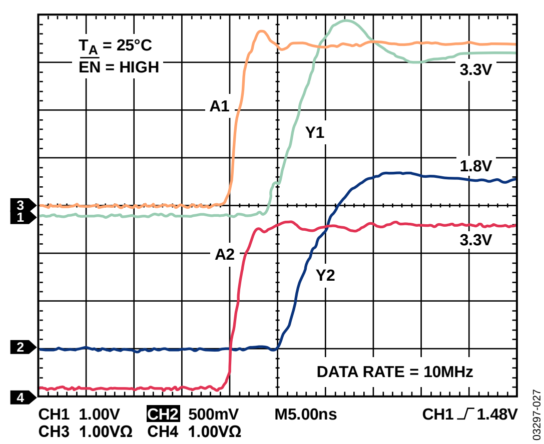

Figure 30. Normal Mode V_{CC1} = 3.3 V, V_{CC2} = 1.8 V

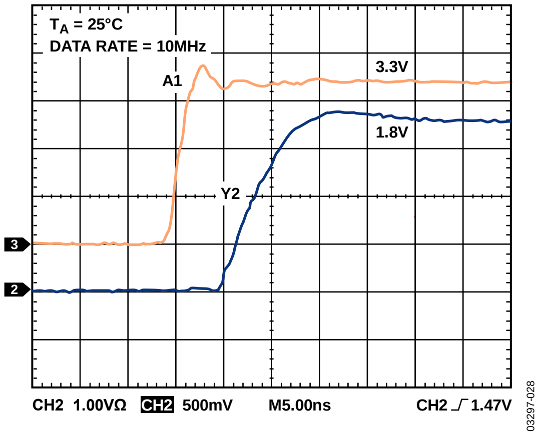

Figure 31. Bypass Mode, V_{CC1} = 3.3 V, V_{CC2} = 1.8 V

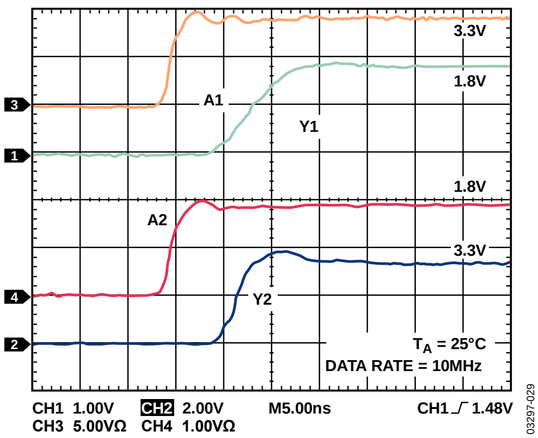

Figure 32. Normal Mode, V_{CC1} = 1.8 V, V_{CC2} = 3.3 V

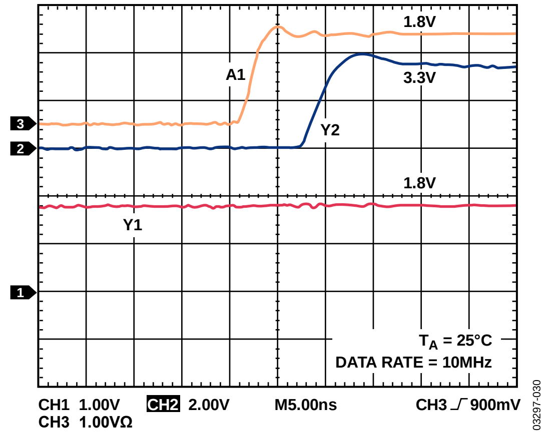

Figure 33. Bypass Mode, V_{CC1} = 1.8 V, V_{CC2} = 3.3 V

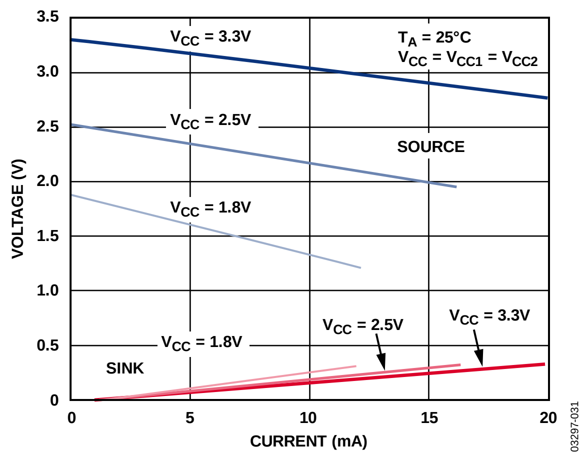

Figure 34. Y1 and Y2 Source and Sink Current

THEORY OF OPERATION

The ADG3233 is a bypass switch designed on a submicron process that operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages, allowing bidirectional level translation, that is, it translates low voltages to higher voltages and vice versa. The signal path is unidirectional, meaning data may only flow from A → Y.

A1 AND $\overline{EN}$ INPUT

The A1 and enable ($\overline{EN}$) inputs have V_{IL}/V_{IH} logic levels so that the part can accept logic levels of V_{OL}/V_{OH} from Device 0 or the controlling device independent of the value of the supply being used by the controlling device. These inputs (A1, $\overline{EN}$) are capable of accepting inputs outside the V_{CC1} supply range. For example, the V_{CC1} supply applied to the bypass switch could be 1.8 V while Device 0 could be operating from a 2.5 V or 3.3 V supply rail, there are no internal diodes to the supply rails, so the device can handle inputs above the supply but inside the absolute maximum ratings.

NORMAL OPERATION

Figure 35 shows the bypass switch being used in normal mode. In this mode, the signal paths are from A1 → Y1 and A2 → Y2. The device will level translate the signal applied to A1 to a V_{CC1} logic level (this level translation can be either to a higher or lower supply) and route the signal to the Y1 output, which will have standard V_{OL}/V_{OH} levels for V_{CC1} supplies. The signal is then passed through Device 1 and back to the A2 input pin of the bypass switch.

The logic level inputs of A2 are with respect to the V_{CC1} supply. The signal will be level translated from V_{CC1} to V_{CC2} and routed to the Y2 output pin of the bypass switch. Y2 output logic levels are with respect to the V_{CC2} supply.

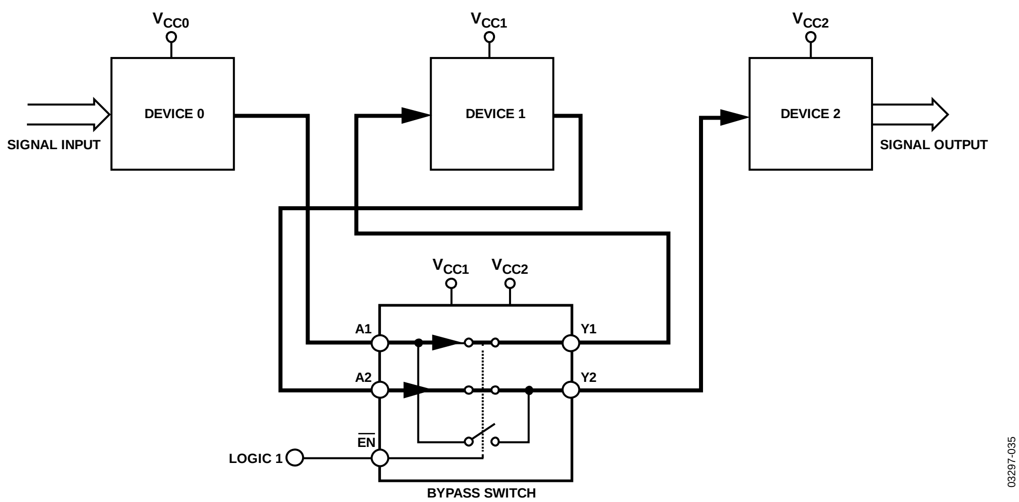

Figure 35. Bypass Switch in Normal Mode

BYPASS OPERATION

Figure 36 illustrates the device as used in bypass mode. The signal path is now from A1 directly to Y2, thus bypassing Device 1 completely. The signal will be level translated to a V_{CC2} logic level and available on Y2, where it may be applied directly to the input of Device 2. In bypass mode, Y1 is pulled up to V_{CC1}.

The three supplies in Figure 35 and Figure 36 may be any combination of supplies, that is., V_{CC0}, V_{CC1}, and V_{CC2} may be any combination of supplies, for example, 1.8 V, 2.5 V, and 3.3 V.

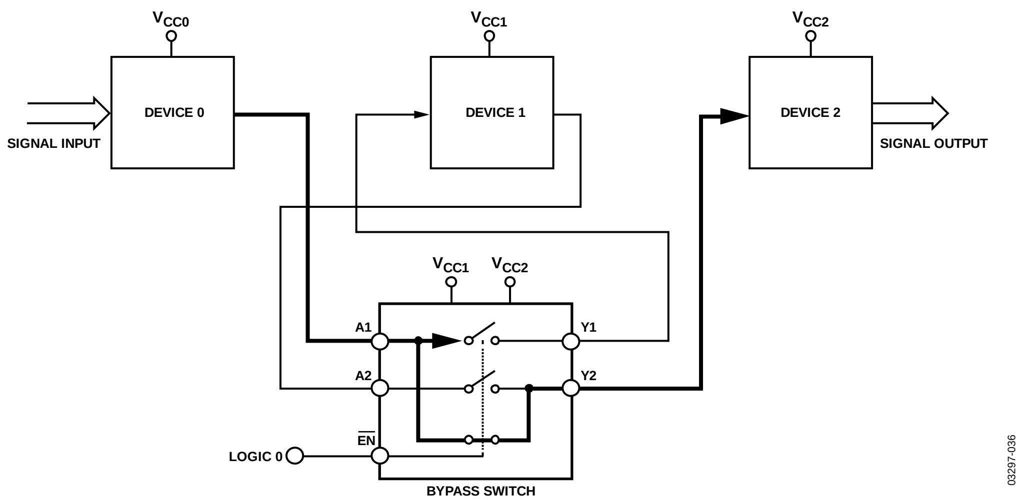

Figure 36. Bypass Switch in Bypass Mode

OUTLINE DIMENSIONS

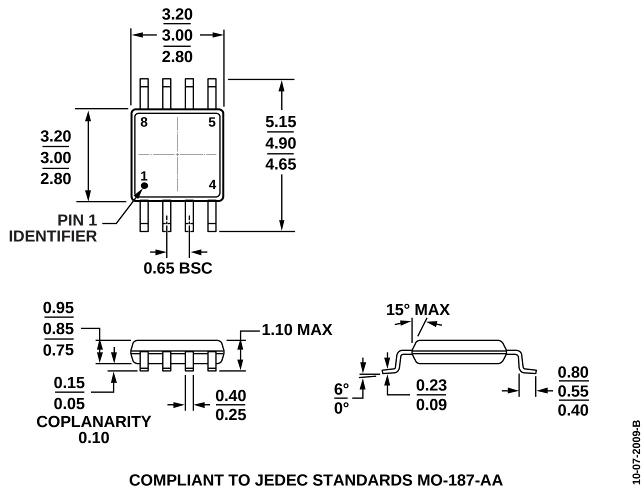

Figure 37. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

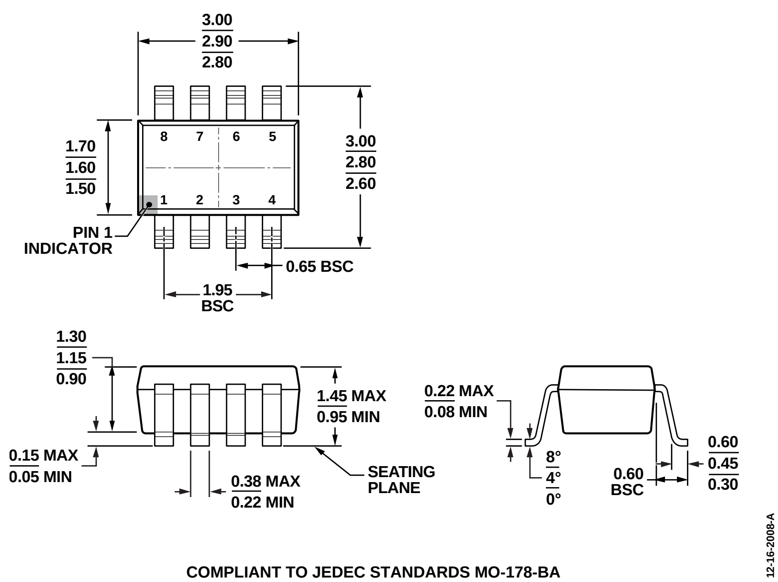

Figure 38. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Branding	Package Option
ADG3233BRJ-REEL	−40°C to +85°C	8-Lead SOT-23	W1B	RJ-8
ADG3233BRJ-REEL7	−40°C to +85°C	8-Lead SOT-23	W1B	RJ-8
ADG3233BRJZ-REEL7	−40°C to +85°C	8-Lead SOT-23	S1S	RJ-8
ADG3233BRM	−40°C to +85°C	8-Lead MSOP	W1B	RM-8
ADG3233BRM-REEL	−40°C to +85°C	8-Lead MSOP	W1B	RM-8
ADG3233BRM-REEL7	−40°C to +85°C	8-Lead MSOP	W1B	RM-8
ADG3233BRMZ	−40°C to +85°C	8-Lead MSOP	S1S	RM-8
ADG3233BRMZ-REEL7	−40°C to +85°C	8-Lead MSOP	S1S	RM-8

[1] Z = RoHS Compliant Part.

D03297-0-7/13(B)

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