

# Small Highly-Integrated Highly-Efficient Non-Isolated PoE Powered Device

## DESCRIPTION

Demonstration circuit 2125 is a small, highly-integrated, non-isolated PoE Powered Device (PD) solution. It features a PD Interface Controller (LT<sup>®</sup>4275), which interfaces with a PoE Power Sourcing Equipment (PSE), an ideal diode bridge controller (LT4321), which minimizes bridge losses, and a DC/DC  $\mu$ Module<sup>®</sup> regulator (LTM<sup>®</sup>8027).

The DC2125 is initially configured as a 38.7W LTPoE++<sup>™</sup> PD that is capable of providing 12V and 3A at the output. Users can configure the PD circuit to be an IEEE802.3

compliant Type 2 (25.5W, “at”) or Type 1 (13W, “af”) PD by changing the RCLASS and RCLASS++ resistors. See the LT4275 data sheet for further information. The output voltage of the LTM8027 can be easily configured for different output voltages as shown in the LTM8027 data sheet.

**Gerber files for this circuit board are available. Call the LTC factory.**

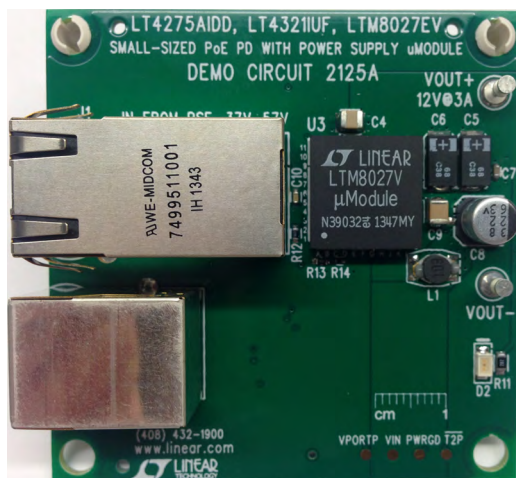
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## PERFORMANCE SUMMARY

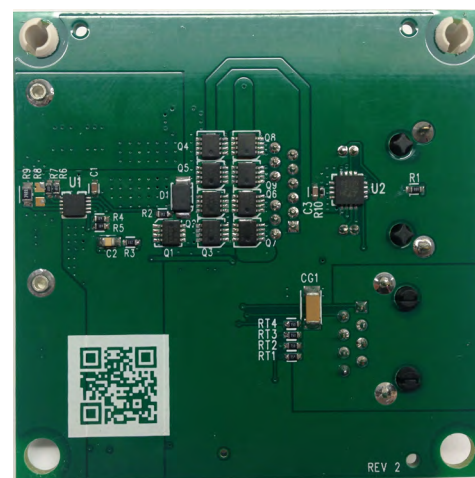
Specifications are at  $T_A = 25^\circ\text{C}$

SYMBOL	CONDITIONS	UNITS
$V_{\text{PORT}}$	RJ-45 Port Voltage Range	37V to 57V
$I_{\text{OUT(MAX)}}$	Maximum Current from $V_{\text{OUT}^+}$ to $V_{\text{OUT}^-}$	3A
$V_{\text{OUT}}$	Output Voltage	12V (typ)
$\Delta V_{\text{OUT(ripple)}}$	Output Voltage Ripple at $V_{\text{PORT}} = 50\text{V}$ , $I_{\text{OUT}} = 3\text{A}$	58mVpp (typ)
$\Delta V_{\text{OUT(REG)}}$	Output Voltage Regulation, $I_{\text{OUT}} = 0\text{A}$ to $3\text{A}$ , $V_{\text{PORT}}$	$\pm 0.031\%$ (typ)
Efficiency	Maximum Efficiency, $V_{\text{PORT}} = 41\text{V}$ , $I_{\text{OUT}} = 3\text{A}$	90% (typ)
$f_{\text{SW}}$	Switching Frequency	300kHz (typ)

## BOARD PHOTOS

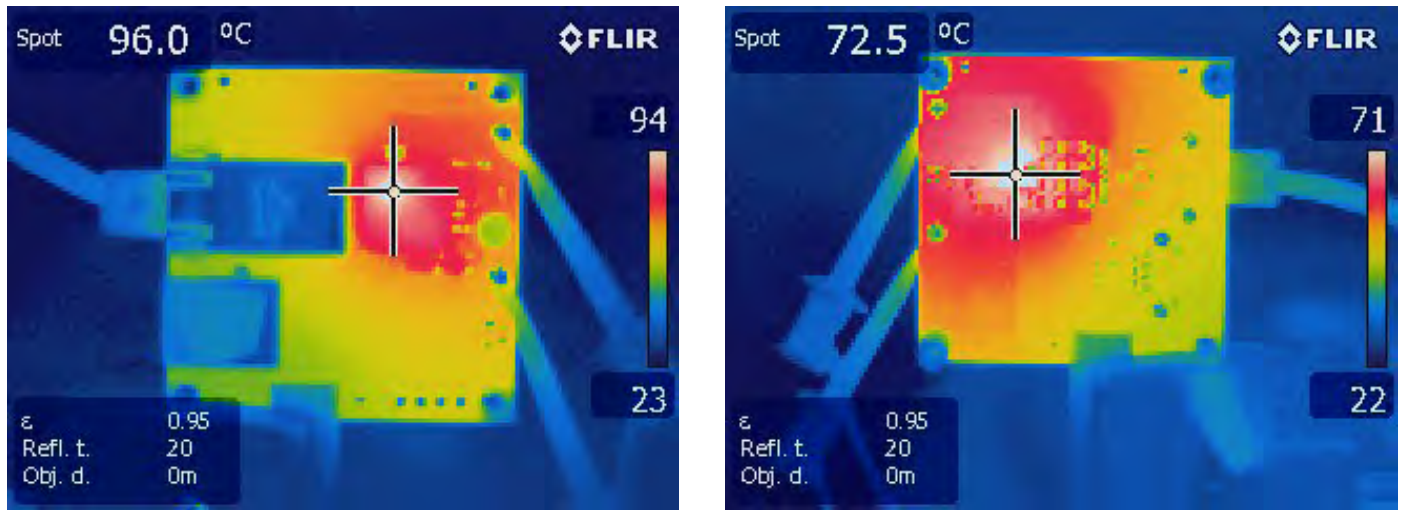


Top Side



Bottom Side

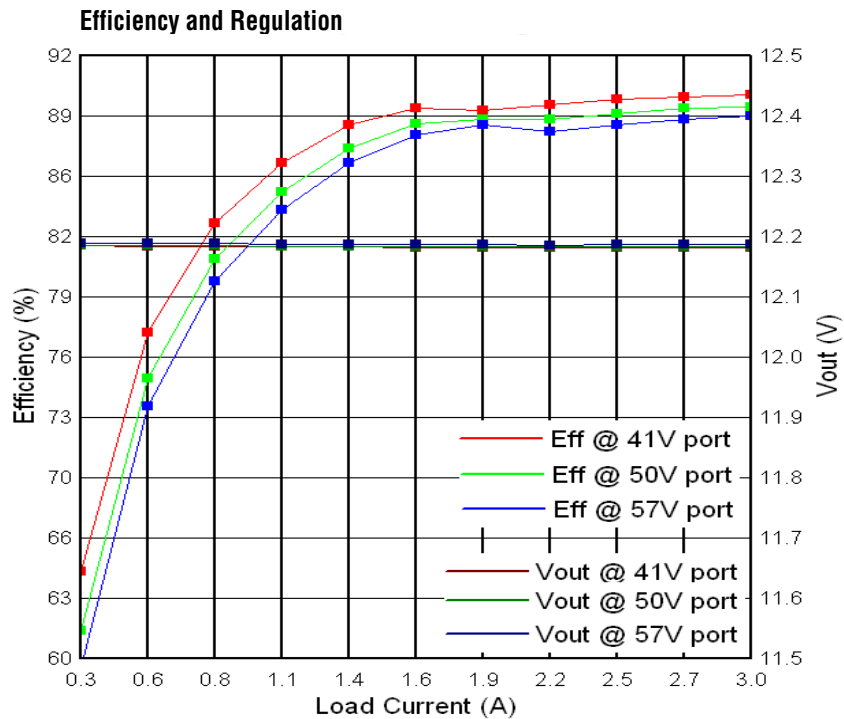
## TYPICAL PERFORMANCE CHARACTERISTICS



Top Side

Bottom Side

Figure 1. Thermal Pictures –  $V_{PORT} = 50V$ ,  $I_{OUT} = 3A$



## QUICK START PROCEDURE

NOTE: Handle the DC2125 printed circuit board by the edges.

1. Refer to Figure 2 below to evaluate the DC2125 while powering a 12V Load such as power resistors or an electronic load.
2. Connect the positive terminal of the 12V Load to the  $V_{OUT+}$  turret, E1. Connect the negative terminal of the 12V Load to the  $V_{OUT-}$  turret, E2. If using an electronic load, power it on and turn the load current down to 0A.
3. Check the power delivery capability of the LTPoE++ PSE to ensure it can power the PD and the 12V Load. Power-up the LTPoE++ PSE. NOTE: The DC1814A-A
4. Connect the output of the PSE to the input RJ45 connector, J1, of the DC2125 with a CAT5e or CAT6 Ethernet cable  $\leq 100$  meters in length.
5. After connection has been established, verify that the LED (D2) is lit. This indicates the PSE has successfully detected and powered the PD.
6. The 12V Load can now be adjusted to exercise the DC2125 over its full operating load range.

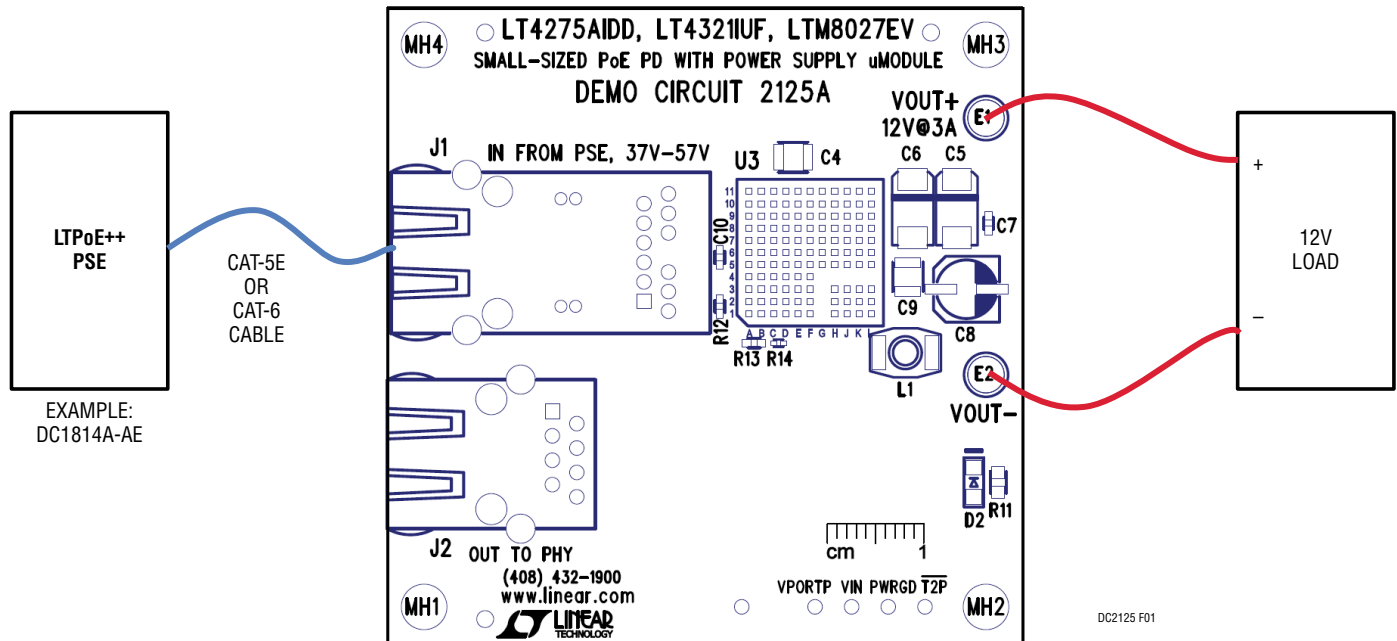


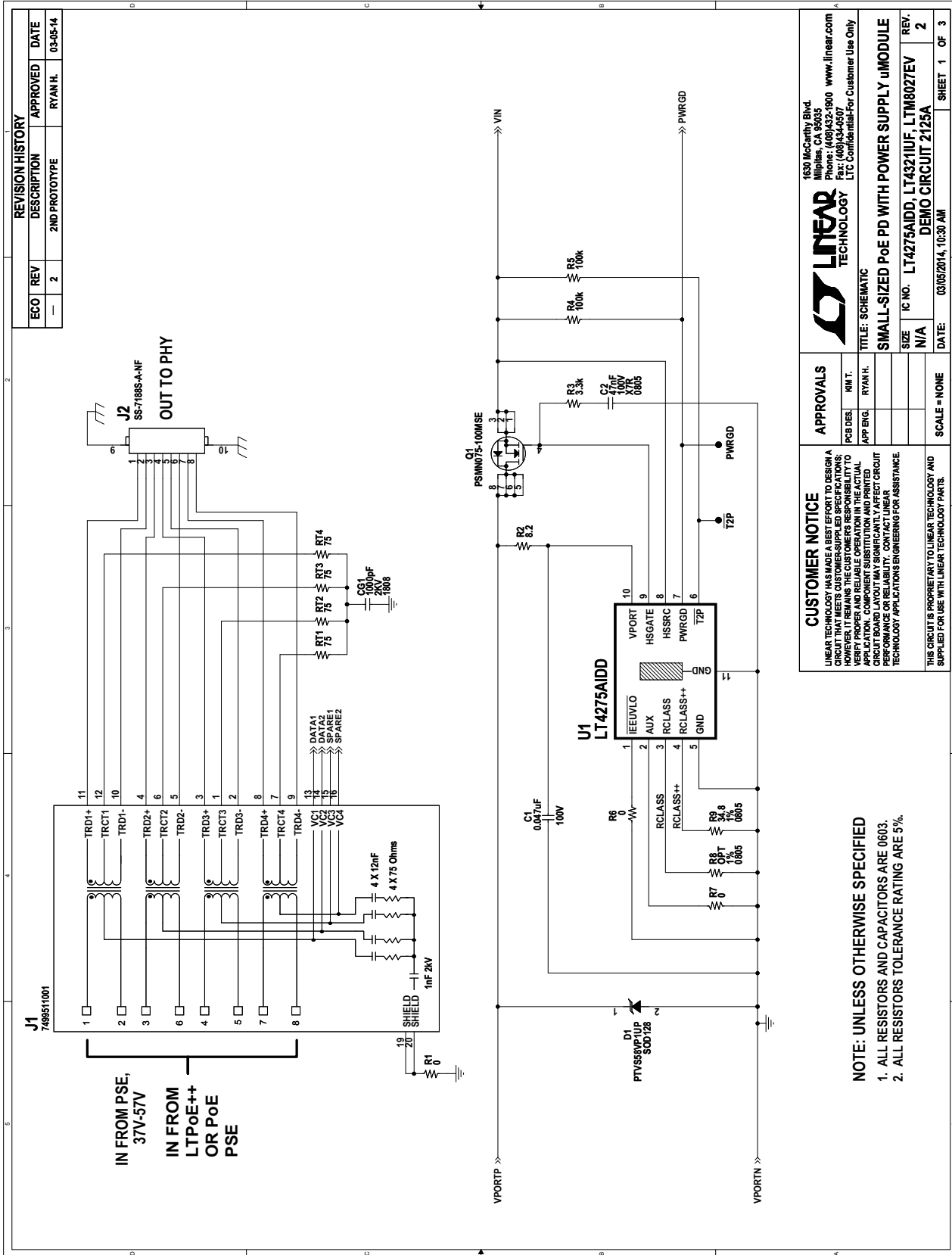
Figure 2. Setup Diagram for the DC2125 Using an LTPoE++ PSE and a Load

# DEMO MANUAL DC2125

## PARTS LIST

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
<b>Required Circuit Components</b>			
2	C1, C3	CAP., X7S, 0.047µF 100V, 10%, 0603	TDK, C1608X7S2A473K
1	C2	CAP., X7R, 47nF 100V, 10%, 0805	AVX, 08051C473KAT2A
1	C4	CAP., X7R, 22µF 16V, 20%, 1210	AVX, 1210YC226MAT2A
2	C5, C6	CAP., TQC, 68µF 16V, 7343	PANASONIC, 16TQC68MYF
1	C7	CAP., X7R, 0.1µF 50V, 10%, 0603	MURATA, GRM188R71H104KA93D
1	C8	CAP., ALUMINUM, 22µF 63V,C-CE-BS-6.3X7.7	SUN ELECT., 63CE22BS
1	C9	CAP., X7R, 2.2µF 100V, 1210	AVX, 12101C225KAT2A
1	C10	CAP., X7R, 1500pF 100V, 5%, 0603	AVX, 06031C152JAT2A
1	D1	DIODE, 600W TRANSIENT VOLTAGE SUPPRESSOR, SOD128	NXP, PTVS58VP1UP
1	J1	CONN., MAGJACK 1PORT 1000BASE-T	WE, 7499511001
1	L1	IND, 10µH, DO1608C	COILCRAFT, DO1608C-103MLB
9	Q1-Q9	MOSFET, N-CH, LFPK33	NXP, PSMN075-100MSE
1	R2	RES., CHIP, 8.2Ω, 5%, 0603	VISHAY, CRCW06038R20JNEA
1	R3	RES., CHIP, 3.3k, 5%, 0603	VISHAY, CRCW06033K30JNEA
2	R4, R5	RES., CHIP, 100k, 5%, 0603	VISHAY, CRCW0603100KJNEA
1	R9	RES., CHIP, 34.8Ω, 1%, 0805	VISHAY, CRCW080534R8FKEA
1	R12	RES., CHIP, 56.2k, 1%, 0603	VISHAY, CRCW060356K2FKEA
1	R13	RES., CHIP, 49.9k, 1%, 0603	VISHAY, CRCW060349K9FKEA
1	U1	IC, LT4275AIDD#PBF, DFN10DD-3X3	LINEAR TECHNOLOGY CORPORATION, LT4275AIDD#PBF
1	U2	IC, LT4321IUF#PBF, QFN16UF-4X4	LINEAR TECHNOLOGY CORPORATION, LT4321IUF#PBF
1	U3	IC, µModule REGULATOR, LGA113-15X15X4.32	LINEAR TECHNOLOGY CORPORATION, LTM8027EV#PBF
<b>Optional Circuit Components</b>			
1	CG1	CAP., X7R, 1000pF, 2KV, 10% 1808	TDK, C4520X7R3D102K
1	D2	LED, GREEN	ROHM, SML-010FTT86L
1	J2	CONN., SS-7188S-A-NF	STEWART CONNECTOR, SS-7188S-A-NF
4	RT1-RT4	RES., CHIP, 75Ω, 5%, 0603	VISHAY, CRCW060375R0JNEA
3	R1, R6, R7	RES., CHIP, 0Ω, 5%, 0603	VISHAY, CRCW06030000Z0EA
0	R8	RES., 0805	OPT
1	R11	RES., CHIP, 2k, 5%, 0805	VISHAY, CRCW08052K00JNEA
2	R10, R14	RES., CHIP, 0Ω, 5%, 0402	VISHAY, CRCW04020000Z0ED
<b>Hardware: For Demo Board Only</b>			
2	E1, E2	TP, TURRET, 0.094"	MILL-MAX 2501-2-00-80-00-00-07-0
4	MH1-MH4	STANDOFF, NYLON, 0.5, 1/2"	KEYSTONE, 8833 (SNAP ON)

**SCHEMATIC DIAGRAM**



**LINEAR TECHNOLOGY**

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**APPROVALS**

PCB DES.	KIM T.
APP ENG.	RYAN.H.

**TITLE: SCHEMATIC**

**SMALL-SIZED PoE PD WITH POWER SUPPLY uMODULE**

SIZE	N/A
IC NO.	LT4275AIDD, LT4321UF, LTM8027EV
REV.	2

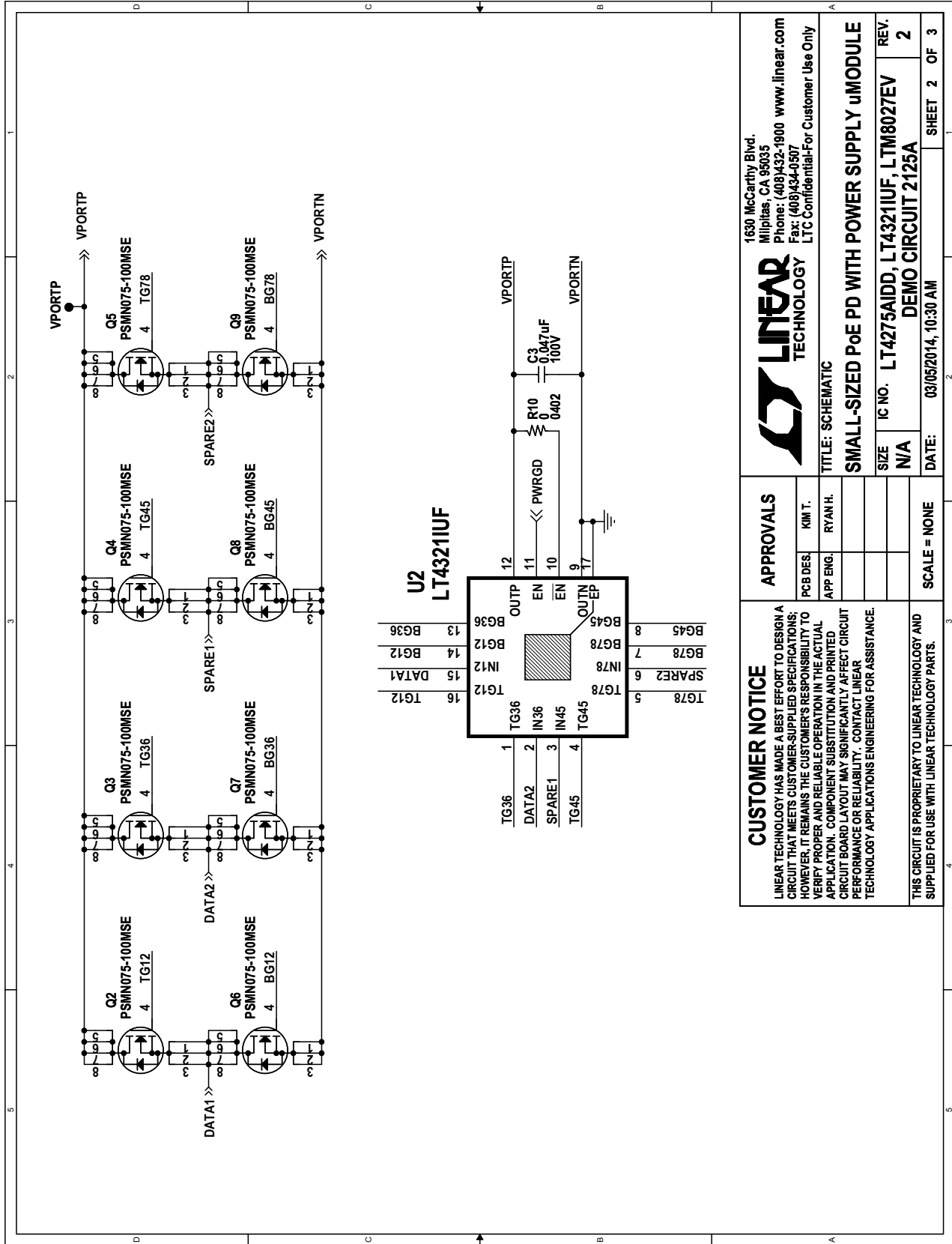
DATE: 03/05/2014, 10:30 AM

SCALE = NONE

SHEET 1 OF 3

Figure 3. DC2125 Demo Circuit Schematic, Sheet 1

## SCHEMATIC DIAGRAM



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**APPROVALS**

PCB DES.	KIM T.
APP ENG.	RYAN H.
SCALE	NONE

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**TITLE: SCHEMATIC**

**SMALL-SIZED PoE PD WITH POWER SUPPLY UMODULE**

SIZE	N/A	REV.	2
IC NO.	LT4275AIDD, LT4321UFD, LTM8027EV	DEMO CIRCUIT	2125A
DATE:	03/05/2014, 10:30 AM	SHEET	2 OF 3

Figure 4. DC2125 Demo Circuit Schematic, Sheet 2

**SCHEMATIC DIAGRAM**

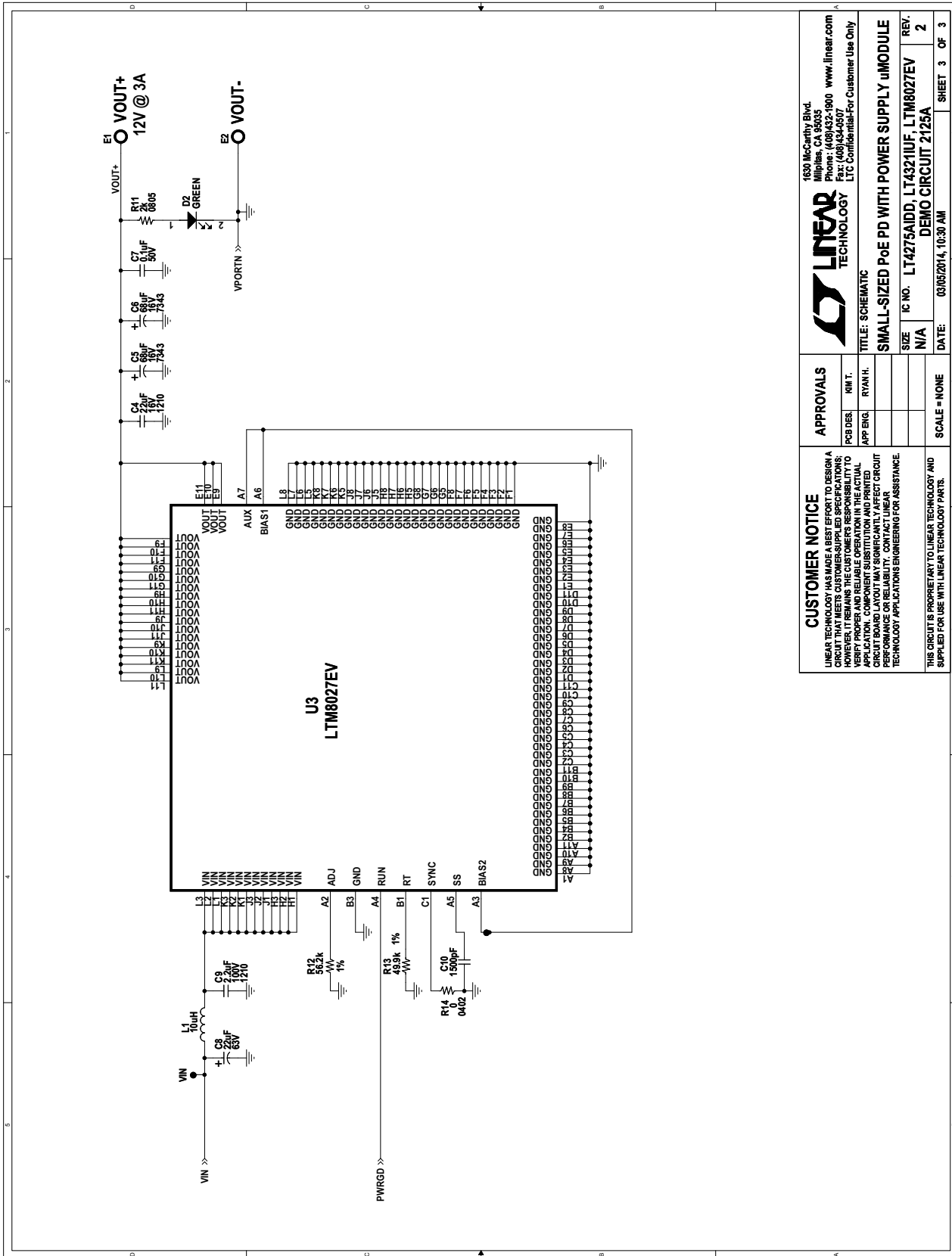


Figure 5. DC2125 Demo Circuit Schematic, Sheet 3

# DEMO MANUAL DC2125

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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