

# LT1763 500mA Low Noise Micropower LDO Regulator

## DESCRIPTION

Demonstration circuit DC368A is a low noise micropower voltage regulator using the LT<sup>®</sup>1763 in the 8-lead SO package. These circuits are used primarily in voltage controlled oscillators, RF power supplies and, in larger systems, as local regulators. The ability to tolerate a wide variety of

output capacitors makes them ideal in space- and cost-sensitive systems.

**Design files for this circuit board are available at <http://www.linear.com/demo/DC368A>**

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## PERFORMANCE SUMMARY

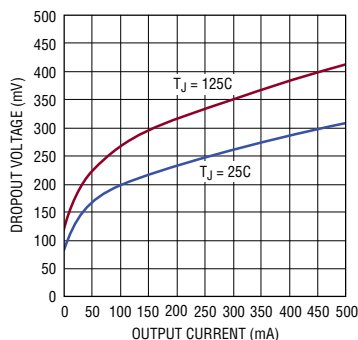
$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 2.3\text{V}$ ,  $V_{SHDN} = 5\text{V}$ ,  $I_{LOAD} = 1\text{mA}$ ,  $V_{OUT} = 1.22\text{V}$  (JP2 set on Pins 1-2), unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.3		20	V
Output Voltage (Note 1)		1.208	1.220	1.232	V
Output Voltage (Note 1)	$V_{IN} = 1.5\text{V}$ , JP2 on Pins 5-6	1.478	1.497	1.519	V
Output Voltage (Note 1)	$V_{IN} = 1.8\text{V}$ , JP2 on Pins 7-8	1.775	1.802	1.834	V
Output Voltage (Note 1)	$V_{IN} = 2.5\text{V}$ , JP2 on Pins 9-10	2.462	2.506	2.563	V
Output Voltage (Note 1)	$V_{IN} = 3\text{V}$ , JP2 on Pins 11-12	2.961	3.019	3.093	V
Output Voltage (Note 1)	$V_{IN} = 3.3\text{V}$ , JP2 on Pins 13-14	3.235	3.300	3.384	V
Output Voltage (Note 1)	$V_{IN} = 5\text{V}$ , JP2 on Pins 15-16	4.897	5.006	5.148	V
Line Regulation	$\Delta V_{IN} = 2.3\text{V}$ to 20V		1	5	mV
Quiescent Current	$\Delta I_{LOAD} = 0\text{mA}$		30	50	$\mu\text{A}$
Load Regulation	$\Delta I_{LOAD} = 1\text{mA}$ to 500mA		0.2	1	%
SHDN Pin Threshold	On-to-Off	0.45	0.65		V
	Off-to-On, $I_{LOAD} = 1\text{mA}$		0.8	1.8	V
Output Voltage Noise	$I_{LOAD} = 500\text{mA}$ , BW = 10Hz to 100kHz		20		$\mu\text{V}_{\text{RMS}}$

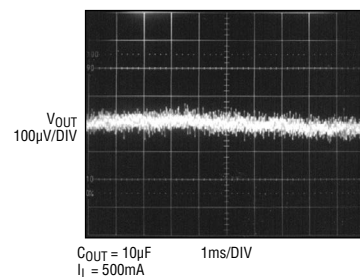
**Note 1:** Output voltage variations include  $\pm 1\%$  tolerance of feedback divider network. For tighter voltage range, use lower tolerance resistors or use fixed voltage output devices.

## TYPICAL PERFORMANCE CHARACTERISTICS

Typical Dropout Voltage



LT1763 (5V Output)  
10Hz to 100kHz Output Noise



## PACKAGE AND SCHEMATIC DIAGRAMS

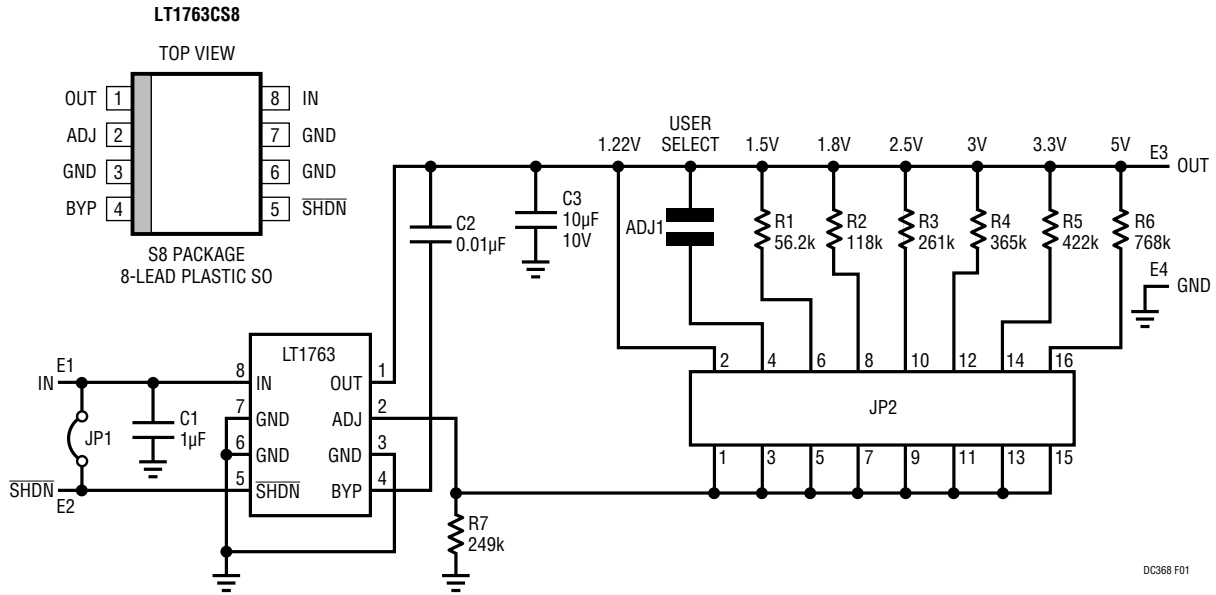


Figure 1. LT1763 500mA Low Noise Micropower LDO Regulator

DC368 F01

## PARTS LIST

ITEM	QUANTITY	REFERENCE	PART DESCRIPTION	MANUFACTURE/PART #
1	0	ADJ1	OPT, 0402	
2	1	C1	CAP., X5R 1 $\mu$ F 25V 10%, 0603	AVX 06033D105KAT2A
3	1	C2	CAP., X7R 0.01 $\mu$ F 16V 5%, 0402	AVX 0402YC103JAT1A
4	1	C3	CAP CER X7R 10 $\mu$ F 10V, 1210	TAIYO YUDEN LMK325BJ106MN
5	4	E1 to E4	TP, TERMINAL TURRET, 1 PIN, 0.064 HOLE	Mill-Max 2308-2
6	1	JP1	JMP, 2 PINS 1 ROW .079CC	COMM-CON 2802S-02-G1
7	1	JP2	CONN, SMT2X8, 0.39" GAP	COMM-CON 6351-16P1
8	1	SHUNTS FOR JP1	SHUNTS, .079" CENTER	COMM-CON CCIJ2MM-138G
9	1	SHUNTS FOR JP2	SHUNTS 0.39CC	COMM-CON CTAIJ1MM-G
10	1	R1	RES., CHIP 56.2k 1/16W 1% 0402	AAC CR05-5622FM
11	1	R2	RES., CHIP 118k 1/16W 1% 0402	AAC CR05-1183FM
12	1	R3	RES., CHIP 261k 1/16W 1% 0402	AAC CR05-2613FM
13	1	R4	RES., CHIP 365k 1/16W 1% 0402	AAC CR05-3653FM
14	1	R5	RES., CHIP 422k 1/16W 1% 0402	AAC CR05-4223FM
15	1	R6	RES., CHIP 768k 1/16W 1% 0402	AAC CR05-7683FM
16	1	R7	RES., CHIP 249k 1/16W 1% 0402	AAC CR05-2493FM
17	1	U1	IC, LT1763CS8, SO8	LINEAR TECH. LT1763CS8

## OPERATION

### HOOK-UP

Solid turret terminals are provided for easy connection to supplies and test equipment. Connect a 0V to 20V, 0.6A power supply across the IN and GND terminals and the load across the OUT and GND terminals. The  $\overline{\text{SHDN}}$  pin can be disconnected from IN via JP1 to allow for separate shutdown control via a secondary control line. JP2 can be used to select any of a number of common fixed output voltages, or used in conjunction with ADJ1 to create a custom output voltage using the formula:

$$\text{ADJ1} = (V_{\text{OUT}} - 1.22\text{V})/4.93\mu\text{A}$$

### Thermal Characteristics

Demonstration Circuit DC368A has been laid out to illustrate and achieve maximum power handling capabilities. Although a simple two-layer board might have been sufficient for electrical operation of the LT1763, the four-layer board with vias to internal ground planes offers excellent thermal characteristics. A two-layer board of the same size with no thermal vias will exhibit a thermal resistance of 60°C/W, whereas DC368A exhibits a thermal resistance of 50°C/W.

### OUTPUT CAPACITOR SELECTION

The output capacitor C3 is a 10μF X7R ceramic chip capacitor. Should a different output capacitor be desired, care must be exercised with the selection. Many ceramic capacitor dielectrics exhibit strong temperature and voltage characteristics that reduce their effective capacitance to as low as 10% to 20% of nominal over the full temperature range. For further information, see Linear Technology Application Note 83, "Performance Verification of Low Noise, Low Dropout Regulators," Appendix B, "Capacitor Selection Considerations," reprinted below.

### CAPACITOR SELECTION CONSIDERATIONS

#### Bypass Capacitance and Low Noise Performance

Adding a capacitor between the regulator's  $V_{\text{OUT}}$  and BYP pins lowers output noise. A good quality, low leakage capacitor is recommended. This capacitor bypasses the regulator's reference, providing a low frequency noise

pole. A 0.01μF capacitor lowers the output voltage noise to 20μV<sub>RMS</sub>. Using a bypass capacitor also improves transient response. With no bypassing and a 10μF output capacitor, a 10mA to 500mA load step settles to within 1% of final value in under 100μs. With a 0.01μF bypass capacitor, the output settles to within 1% for the same load step in under 10μs; total output deviation is inside 2.5%. Regulator start-up time is inversely proportional to bypass capacitor size, slowing to 15ms with a 0.01μF bypass capacitor and 10μF at the output.

### Output Capacitance and Transient Response

The regulators are designed to be stable with a wide range of output capacitors. Output capacitor ESR affects stability, most notably with small capacitors. A 3.3μF minimum output value with ESR of 3Ω or less is recommended to prevent oscillation. Transient response is a function of output capacitance. Larger values of output capacitance decrease peak deviations, providing improved transient response for large load current changes. Bypass capacitors, used to decouple individual components powered by the regulator, increase the effective output capacitor value. Larger values of reference bypass capacitance dictate larger output capacitors. For 100pF of bypass capacitance, 4.7μF of output capacitor is recommended. With 1000pF or more of bypass capacitance, a 6.8μF output capacitor is required.

The shaded region of Figure B1 defines the regulator's stability range. The minimum ESR needed is set by the amount of bypass capacitance used, while maximum ESR is 3Ω.

### Ceramic Capacitors

Ceramic capacitors require extra consideration. They are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high capacitance in a small package, but exhibit strong voltage and temperature coefficients, as shown in Figures B2 and B3. Used with a 5V regulator, a 10μF Y5V capacitor shows values as low as 1μF to 2μF over the operating temperature range. The X5R and X7R dielectrics have

## OPERATION

more stable characteristics and are more suitable for output capacitor use. The X7R type has better stability over temperature, while the X5R is less expensive and available in higher values.

Voltage and temperature coefficients are not the only problem sources. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way

a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced Figure B4's trace in response to light tapping from a pencil. Similar vibration-induced behavior can masquerade as increased output voltage noise.

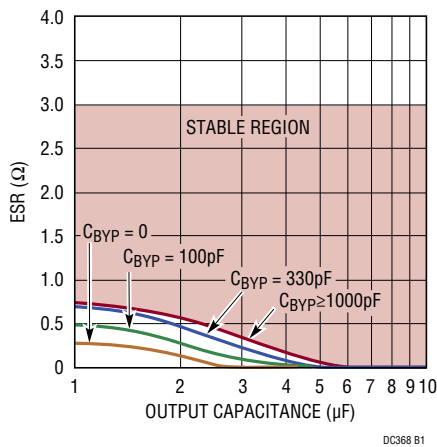


Figure B1. LT1763 Regulator Stability for Various Output and Bypass (C<sub>BYP</sub>) Capacitor Characteristics

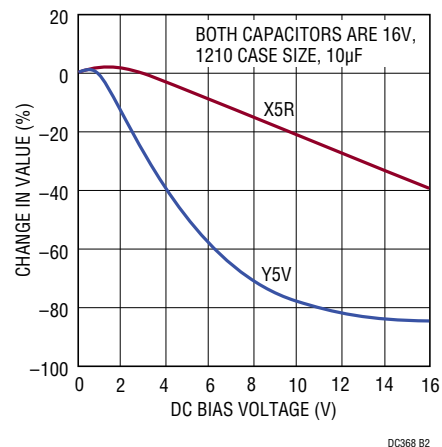


Figure B2. Ceramic Capacitor DC Bias Characteristics Indicate Pronounced Voltage Dependence. Device Must Provide Desired Capacitance Value at Operating Voltage

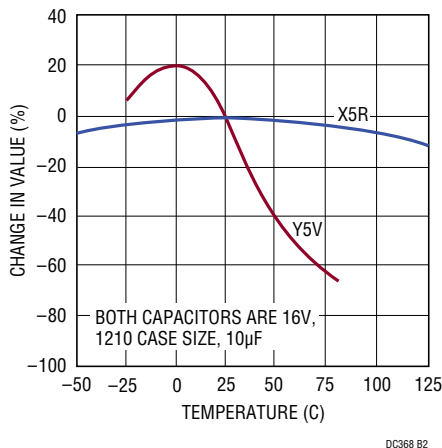


Figure B3. Ceramic Capacitor Temperature Characteristics Show Large Capacitance Shift. Effect Should Be Considered When Determining Circuit Error Budget

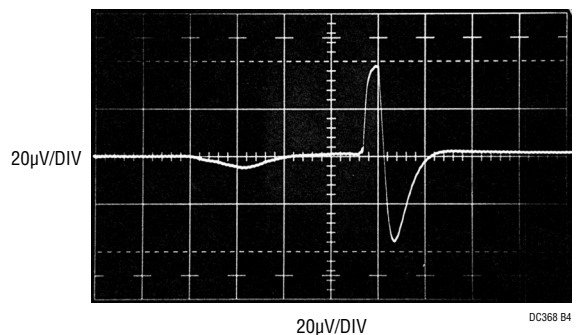


Figure B4. A Ceramic Capacitor Responds to Light Pencil Tapping. Piezoelectric Based Response Approaches 80μV<sub>p-p</sub>

## OPERATION

### OUTPUT VOLTAGE NOISE

Measuring output voltage noise can be a tricky process, further complicated by the low levels of noise inherent in a circuit such as this. Consideration must be given to regulator operating conditions, as well as the noise bandwidth of interest. Linear Technology has invested an enormous amount of time to provide accurate, relevant data to customers regarding noise performance. For further information on measuring output voltage noise, see Linear Technology Application Note 83, "Performance Verification of Low Noise, Low Dropout Regulators."

### Noise Testing Considerations

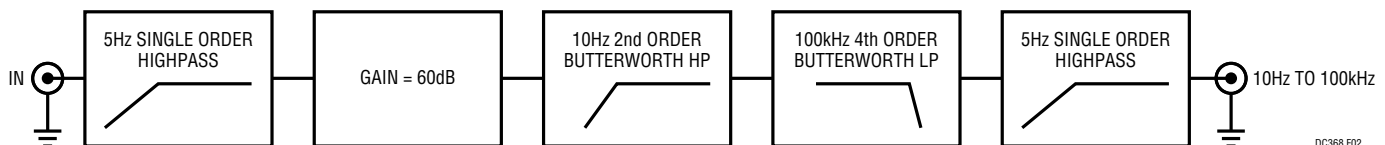
What noise bandwidth is of interest and why is it interesting? In most systems, the range of 10Hz to 100kHz is the information signal processing area of concern. Additionally, linear regulators produce little noise energy outside this region.<sup>1</sup> These considerations suggest a measurement bandpass of 10Hz to 100kHz, with steep slopes at the band limits. Figure 2 shows a conceptual filter for LDO noise testing. The Butterworth sections are the key to

step slopes and flatness in the passband. The small input level requires 60dB of low noise gain to provide adequate signal for the Butterworth filters. Figure 3 details the filter scheme. The regulator under test is at the diagram's center.<sup>2</sup> A1–A3 make up a 60dB gain highpass section. A1 and A2, extremely low noise devices ( $<1\text{nV}/\sqrt{\text{Hz}}$ ), comprise a 60dB gain stage with a 5Hz highpass input. A3 provides a 10Hz, 2nd order Butterworth highpass characteristic. The LTC<sup>®</sup>1562 filter block is arranged as a 4th order Butterworth lowpass. Its output is delivered via the 330 $\mu\text{F}$ -100 $\Omega$  highpass network. The circuit's output drives a thermally responding RMS voltmeter.<sup>3</sup> Note that all circuit power is furnished by batteries, precluding ground loops from corrupting the measurement.

**Note 1:** Switching regulators are an entirely different proposition, requiring very broadband noise measurement.

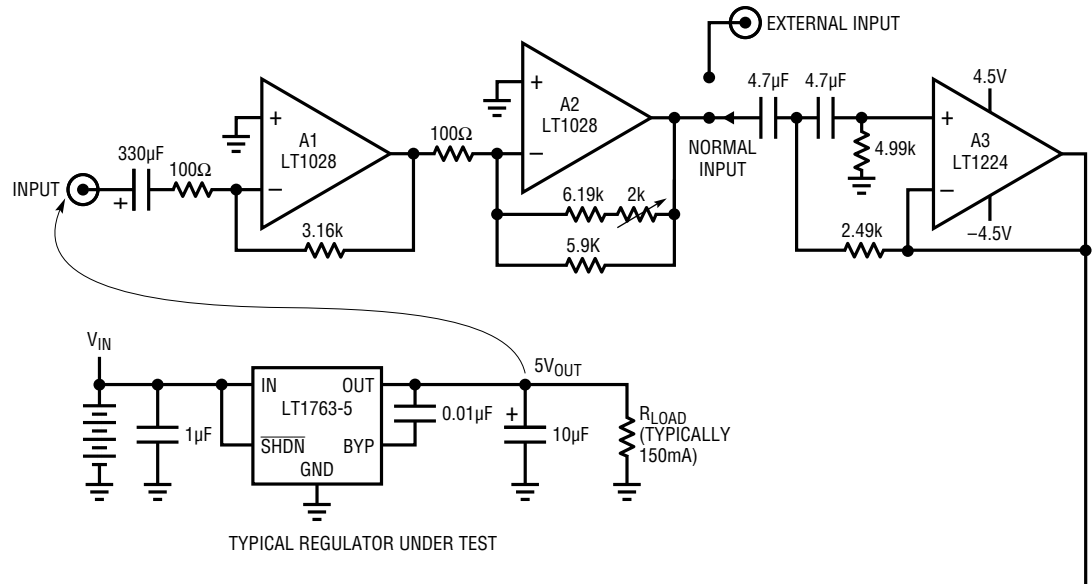
**Note 2:** Component choice for the regulator, more critical than might be supposed, is discussed in "Capacitor Selection Considerations."

**Note 3:** The choice of the RMS voltmeter is absolutely crucial to obtaining meaningful measurements. See Appendix C, Application Note 83 "Understanding and Selecting RMS Voltmeters."



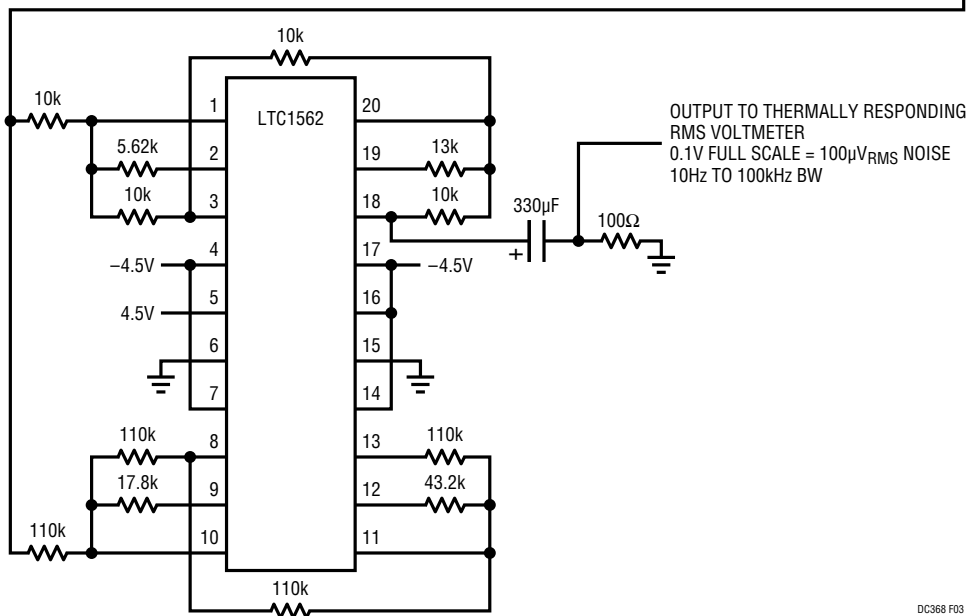
**Figure 2. Filter Structure for Noise Testing LDOs. Butterworth Sections Provide Appropriate Response in Desired Frequency Range**

OPERATION



TYPICAL REGULATOR UNDER TEST

ALL RESISTORS 1% METAL FILM  
 4.7µF CAPACITORS = MYLAR, WIMA MKS-2  
 330µF CAPACITORS = SANYO OSCON  
 ±4.5V DERIVED FROM 6AA CELLS  
 POWER REGULATOR FROM APPROPRIATE  
 NUMBER OF D SIZE BATTERIES



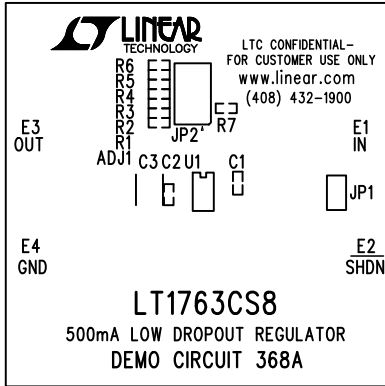
OUTPUT TO THERMALLY RESPONDING  
 RMS VOLTMETER  
 0.1V FULL SCALE = 100µV<sub>RMS</sub> NOISE  
 10Hz TO 100kHz BW

DC368 F03

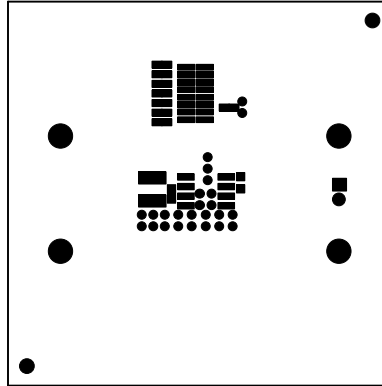
Figure 3. Implementation of Figure 2. Low Noise Amplifiers Provide Gain and Initial Highpass Shaping. LTC1562 Filter Supplies 4th Order Butterworth Lowpass Characteristic

# DEMO MANUAL DC368A

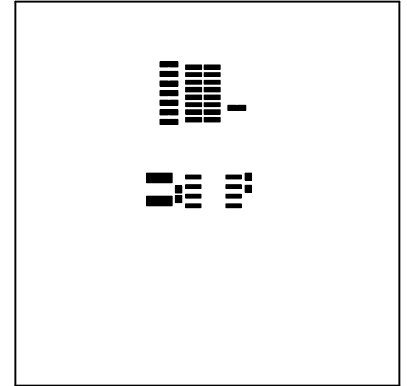
## PCB LAYOUT AND FILM



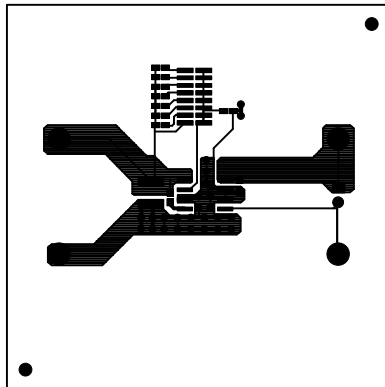
Silkscreen Top



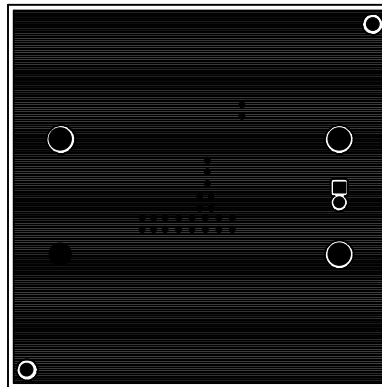
Solder Mask Top



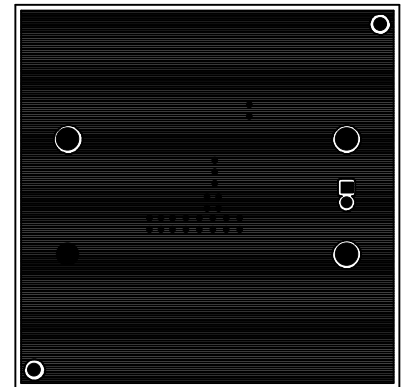
Paste Mask Top



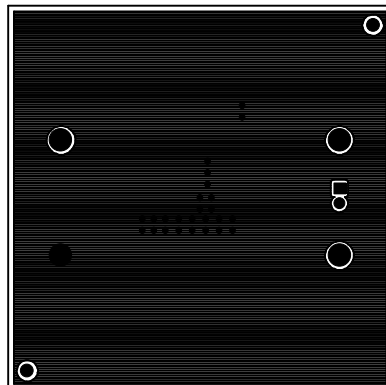
Layer 1, Component Side\*



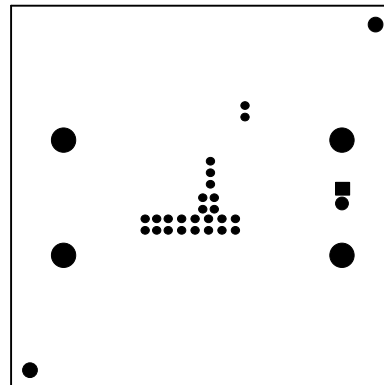
Layer 2, GND Plane\*



Layer 3, GND Plane\*



Layer 4, Solder Side\*

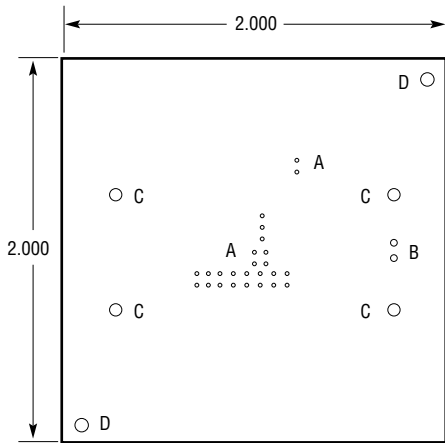


Solder Mask Bottom

\* These layers are shorted to L1 with Vias and function as heat dispersants.

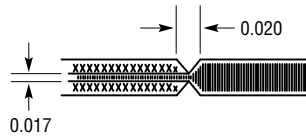


PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: FR4 OR EQUIVALENT EPOXY, 2 OZ. COPPER CLAD THICKNESS 0.062 0.006 TOTAL OF 4 LAYERS.
2. FINISH: ALL PLATED HOLES 0.001 MIN./0.005 MAX. COPPER PLATE ELECTRODEPOSITED TIN-LEAD COMPOSITION BEFORE REFLOW. SOLDER MASK OVER BARE COPPER (SMOBC).
3. SOLDER MASK: BOTH SIDES USING LPI OR EQUIVALENT.
4. SILKSCREEN: USING WHITE EPOXY NON-CONDUCTIVE INK.
5. UNUSED SMD COMPONENTS SHOULD BE FREE OF SOLDER.
6. FILL UP ALL VIAS WITH SOLDER.
7. SCORING:



SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	0.02	25	YES
B	0.035	2	YES
C	0.064	4	YES
D	0.07	2	NO
TOTAL HOLES		33	

# DEMO MANUAL DC368A

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