36V_{IN}, 5A, 2-Quadrant CVCC Step-Down µModule Regulator

FEATURES

- **Complete Step-Down Switch Mode Power Supply**
- **CVCC: Constant-Voltage Constant-Current**
- **2-Quadrant: Sources and Sinks Output Current**
- **Adjustable Output Current**
- **Wide Input Voltage Range: 6V to 36V**
- **1.2V to 24V Output Voltage**
- Forced Continuous Operation
- Selectable Switching Frequency: 100kHz to 1MHz
- (e4) RoHS Compliant Package with Gold Pad Finish
- Programmable Soft-Start
- Compact (11.25mm × 15mm × 2.82mm) Surface Mount LGA and (11.25mm × 15mm × 3.42mm) BGA Packages

APPLICATIONS

- Constant-Frequency Voltage Regulation Even at No Load
- Peltier Driver
- Battery Tester
- Battery/Supercap Charging and Cell Balancing
- Motor Drive Power Regulator
- High Power LED Drive

DESCRIPTION

The LTM®8052/LTM8052A is a 36V_{IN}, 5A, 2-quadrant constant-voltage, constant-current (CVCC) step-down µModule® regulator. Included in the package are the switching controller, power switches, inductor and support components. Operating over an input voltage range of 6V to 36V, the LTM8052/LTM8052A supports an output voltage range of 1.2V to 24V. The LTM8052/LTM8052A is able to sink or source current to maintain voltage regulation up to the positive and negative current limits. This output current limit can be set by a control voltage, a single resistor or a thermistor. LTM8052 features a 125% output overvoltage protection, while LTM8052A does not, allowing operation when the output is above the target regulation point.

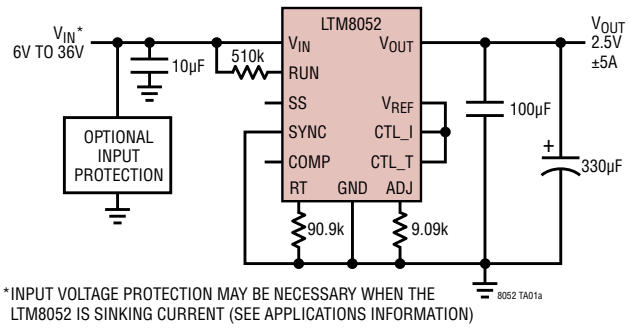
The LTM8052/LTM8052A is packaged in a compact (11.25mm × 15mm × 2.82mm) overmolded land grid array (LGA) and ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8052/LTM8052A are available with SnPb (BGA) or RoHS compliant terminal finish.

PART NUMBER	BEST FOR
LTM8052	Sinking and sourcing output current for voltage regulation primarily.
LTM8052A	Sinking and sourcing output current for current regulation primarily.
LTM8026	Sourcing more than 3A of output current. (Less than 3A maximum consider LTM8025.)

Click to view associated TechClip Videos.

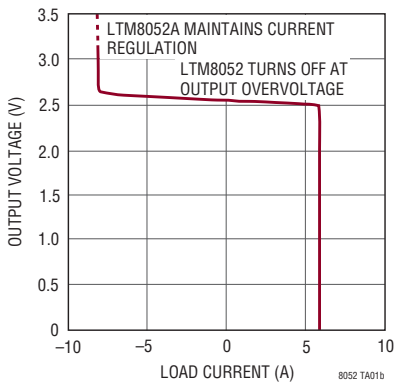
TYPICAL APPLICATION

±5A, 2.5V (2-Quadrant) µModule Voltage Regulator



*INPUT VOLTAGE PROTECTION MAY BE NECESSARY WHEN THE LTM8052 IS SINKING CURRENT (SEE APPLICATIONS INFORMATION)

Output Voltage vs Output Current



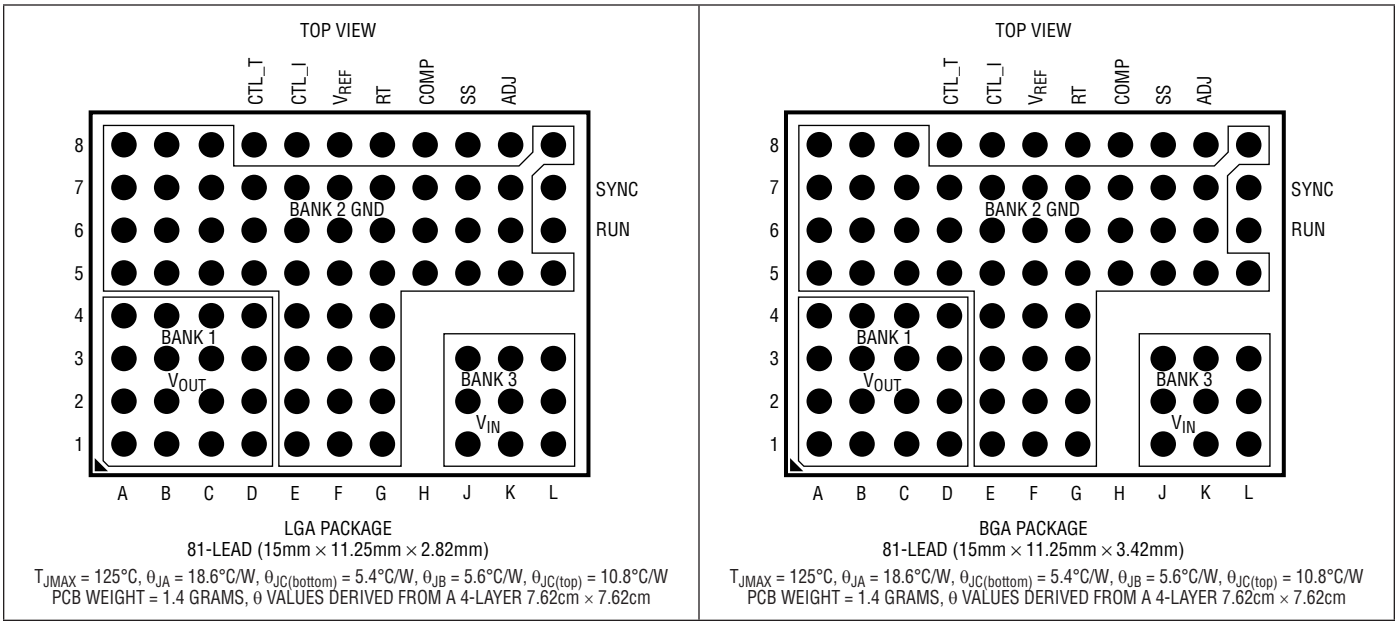
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 40V
ADJ, RT, COMP, CTL_I, CTL_T, V_{REF}.....3V
V_{OUT}.....25V
RUN, SYNC, SS.....6V

Current Into RUN Pin 100µA
Internal Operating Temperature Range .. –40°C to 125°C
Peak Solder Reflow Body Temperature ..... 245°C
Storage Temperature..... –55°C to 125°C

PIN CONFIGURATION



LGA PACKAGE
81-LEAD (15mm × 11.25mm × 2.82mm)

T_{JMAX} = 125°C, θ_{JA} = 18.6°C/W, $\theta_{JC(bottom)}$ = 5.4°C/W, θ_{JB} = 5.6°C/W, $\theta_{JC(top)}$ = 10.8°C/W
PCB WEIGHT = 1.4 GRAMS, θ VALUES DERIVED FROM A 4-LAYER 7.62cm × 7.62cm

BGA PACKAGE
81-LEAD (15mm × 11.25mm × 3.42mm)

T_{JMAX} = 125°C, θ_{JA} = 18.6°C/W, $\theta_{JC(bottom)}$ = 5.4°C/W, θ_{JB} = 5.6°C/W, $\theta_{JC(top)}$ = 10.8°C/W
PCB WEIGHT = 1.4 GRAMS, θ VALUES DERIVED FROM A 4-LAYER 7.62cm × 7.62cm

ORDER INFORMATION

http://www.linear.com/product/LTM8052#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 3)
		DEVICE	FINISH CODE			
LTM8052EV#PBF	Au (RoHS)	LTM8052V	e4	LGA	3	–40°C to 125°C
LTM8052IV#PBF	Au (RoHS)	LTM8052V	e4	LGA	3	–40°C to 125°C
LTM8052MPV#PBF	Au (RoHS)	LTM8052V	e4	LGA	3	–55°C to 125°C
LTM8052AEV#PBF	Au (RoHS)	LTM8052AV	e4	LGA	3	–40°C to 125°C
LTM8052AIV#PBF	Au (RoHS)	LTM8052AV	e4	LGA	3	–40°C to 125°C
LTM8052AMPV#PBF	Au (RoHS)	LTM8052AV	e4	LGA	3	–55°C to 125°C
LTM8052EY#PBF	SAC305 (RoHS)	LTM8052Y	e1	BGA	3	–40°C to 125°C
LTM8052IY#PBF	SAC305 (RoHS)	LTM8052Y	e1	BGA	3	–40°C to 125°C
LTM8052MPY#PBF	SAC305 (RoHS)	LTM8052Y	e1	BGA	3	–55°C to 125°C
LTM8052AEY#PBF	SAC305 (RoHS)	LTM8052AY	e1	BGA	3	–40°C to 125°C
LTM8052AIY#PBF	SAC305 (RoHS)	LTM8052AY	e1	BGA	3	–40°C to 125°C
LTM8052AMPY#PBF	SAC305 (RoHS)	LTM8052AY	e1	BGA	3	–55°C to 125°C
LTM8052IY	SnPb (63/67)	LTM8052Y	e0	BGA	3	–40°C to 125°C
LTM8052MPY	SnPb (63/67)	LTM8052Y	e0	BGA	3	–55°C to 125°C
LTM8052AIY	SnPb (63/67)	LTM8052AY	e0	BGA	3	–40°C to 125°C
LTM8052AMPY	SnPb (63/67)	LTM8052AY	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C. RUN = 3V, unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●			6	V
Output DC Voltage	I_{OUT} = 1A, R_{ADJ} Open I_{OUT} = 1A, R_{ADJ} = 499Ω			1.2 24		V V
Output DC Current	CTL_T, CTL_I = 1.5V		–6		5	A
Quiescent Current Into V_{IN}	V_{IN} = 12V, RUN = 0V V_{IN} = 12V, No Load			0.1 17	3 30	µA mA
Line Regulation	6V < V_{IN} < 36V, I_{OUT} = 1A			0.1		%
Load Regulation	V_{IN} = 12V, 0A < I_{OUT} < 5A			0.7		%
Output RMS Voltage Ripple	V_{IN} = 12V, I_{OUT} = 4.5A			10		mV
Switching Frequency	R_T = 40.2k R_T = 453k			1000 100		kHz kHz
Voltage at ADJ Pin		●	1.16	1.19	1.22	V
Current Out of ADJ Pin	ADJ = 0V, V_{OUT} = 1V			100		µA
RUN Pin Current	RUN = 1.45V			5.5		µA
RUN Threshold Voltage (Falling)			1.49	1.55	1.61	V
RUN Input Hysteresis				160		mV
CTL_I Control Range			0		1.5	V
CTL_I Pin Current					1.5	µA
CTL_I Positive Current Limit	CTL_I = 1.5V CTL_I = 0.75V		5.1 2.24	5.6 2.8	6.1 3.36	A A
CTL_I Negative Current Limit	CTL_I = 1.5V CTL_I = 0.75V		–8.5 –5.7	–7.7 –5.1	–6.9 –4.5	A A
CTL_T Control Range			0		1.5	V
CTL_T Pin Current					1.5	µA
CTL_T Positive Current Limit	CTL_T = 1.5V CTL_T = 0.75V		5.1 2.24	5.6 2.8	6.1 3.36	A A
CTL_T Negative Current Limit	CTL_T = 1.5V CTL_T = 0.75V		–8.5 –5.5	–7.7 –4.9	–6.9 –4.3	A A
V_{REF} Voltage	0.5mA Load		1.93	2	2.04	V
SS Pin Current				11		µA
SYNC Input Low Threshold	f_{SYNC} = 400kHz				0.6	V
SYNC Input High Threshold	f_{SYNC} = 400kHz		1.2			V
SYNC Bias Current	SYNC = 0V				1	µA

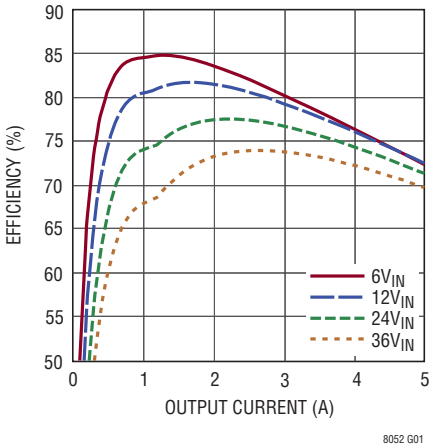
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This µModule regulator includes overtemperature protection that is intended to protect the device during momentary overload conditions. Internal temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum internal operating junction temperature may impair device reliability.

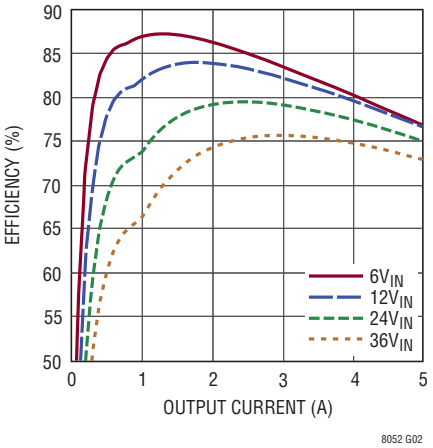
Note 3: The LTM8052E/LTM8052AE is guaranteed to meet performance specifications from 0°C to 125°C internal operating temperature. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8052I/LTM8052AI is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8052MP/LTM8052AMP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

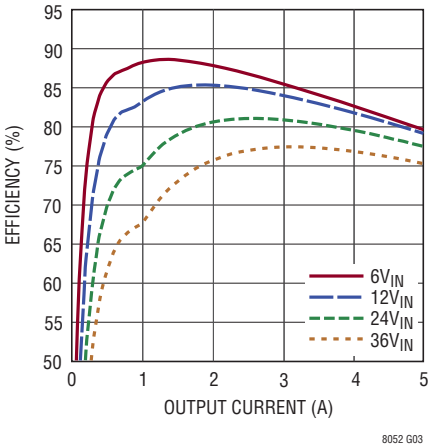
1.2V_{OUT} Efficiency



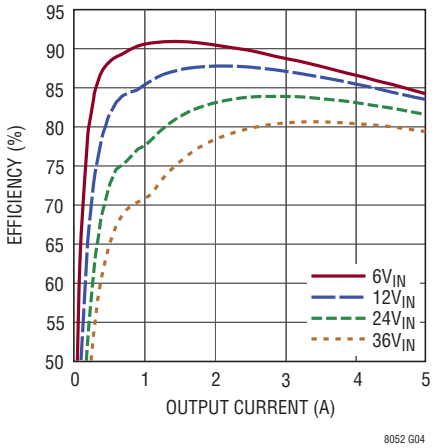
1.5V_{OUT} Efficiency



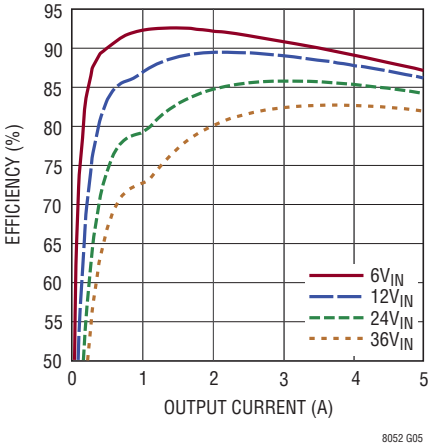
1.8V_{OUT} Efficiency



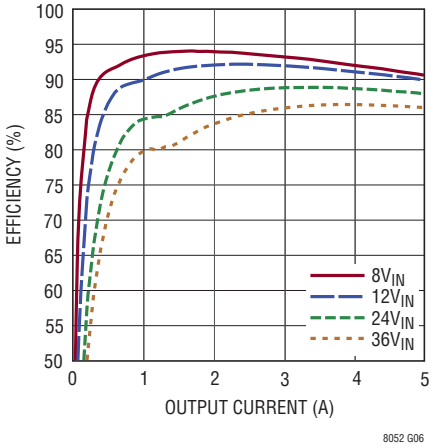
2.5V_{OUT} Efficiency



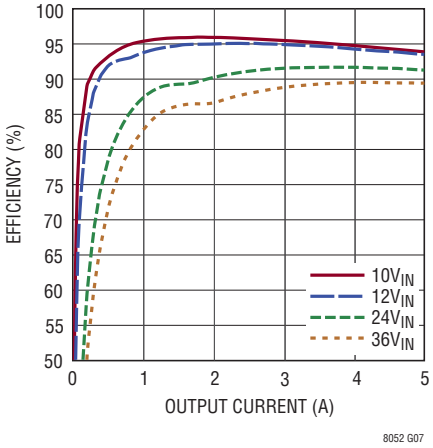
3.3V_{OUT} Efficiency



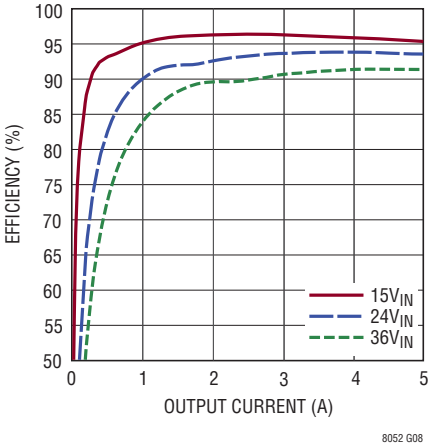
5V_{OUT} Efficiency



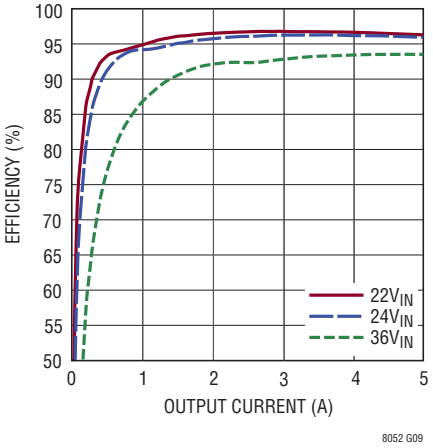
8V_{OUT} Efficiency



12V_{OUT} Efficiency

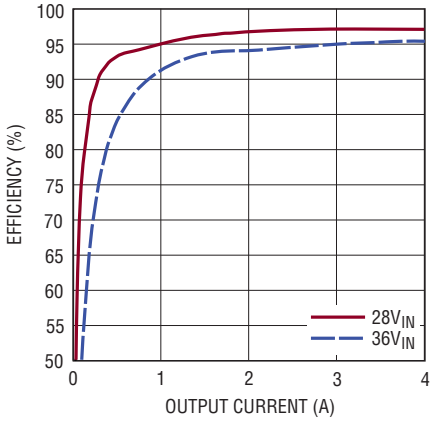


18V_{OUT} Efficiency

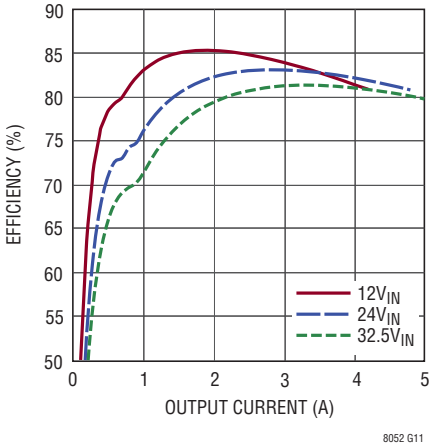


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

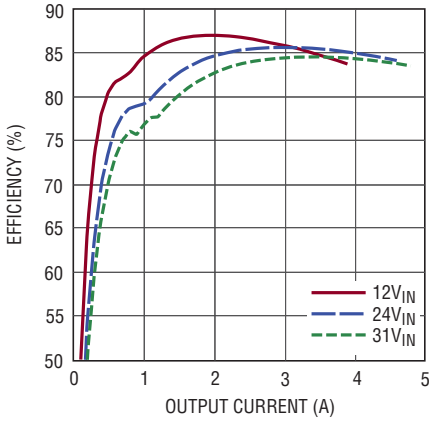
24V_{OUT} Efficiency



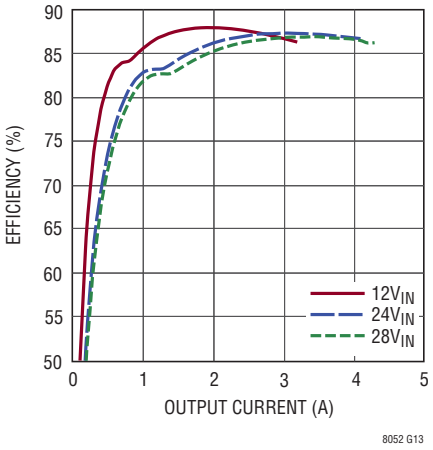
–3.3V_{OUT} Efficiency



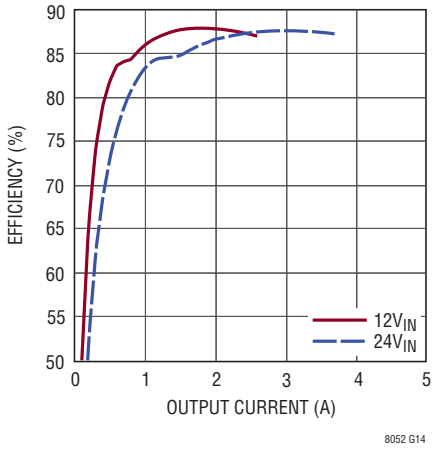
–5V_{OUT} Efficiency



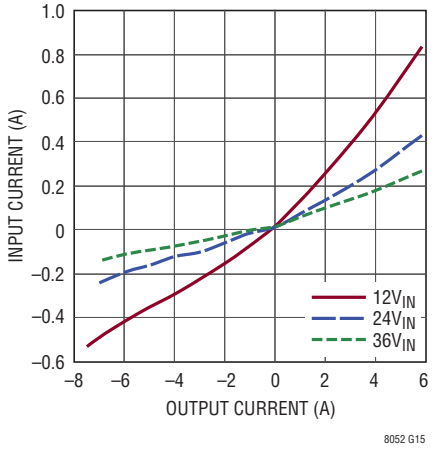
–8V_{OUT} Efficiency



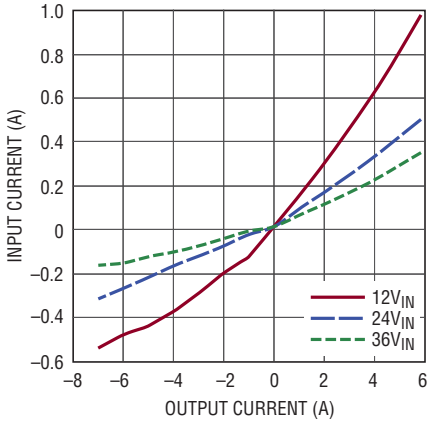
–12V_{OUT} Efficiency



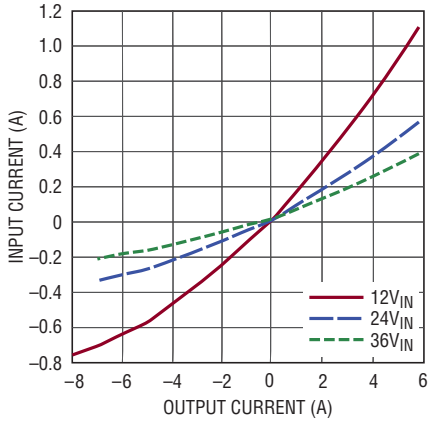
Input Current vs Output Current 1.2V_{OUT}



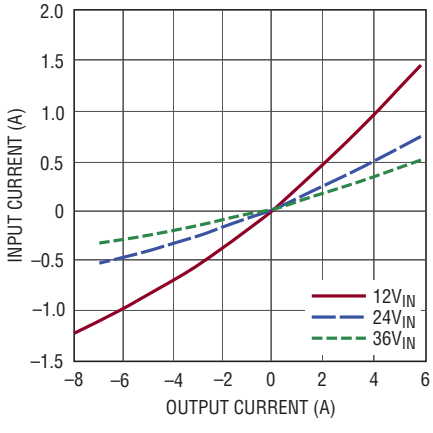
Input Current vs Output Current 1.5V_{OUT}



Input Current vs Output Current 1.8V_{OUT}

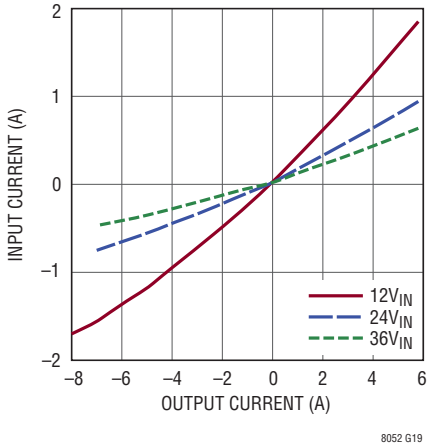


Input Current vs Output Current 2.5V_{OUT}

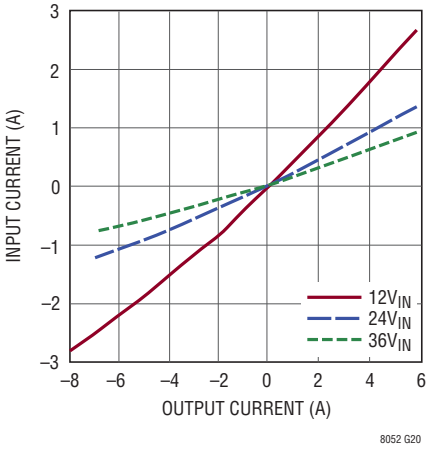


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

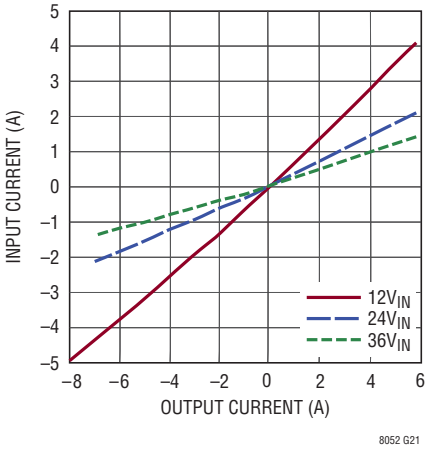
Input Current vs Output Current 3.3V_{OUT}



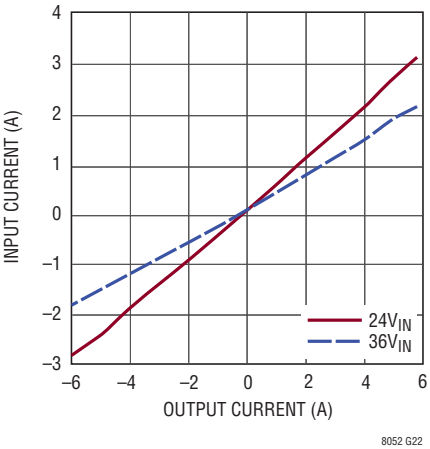
Input Current vs Output Current 5V_{OUT}



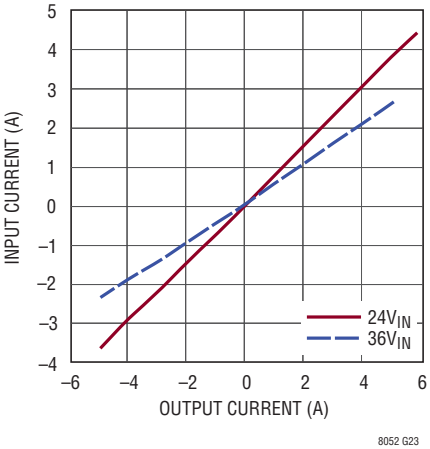
Input Current vs Output Current 8V_{OUT}



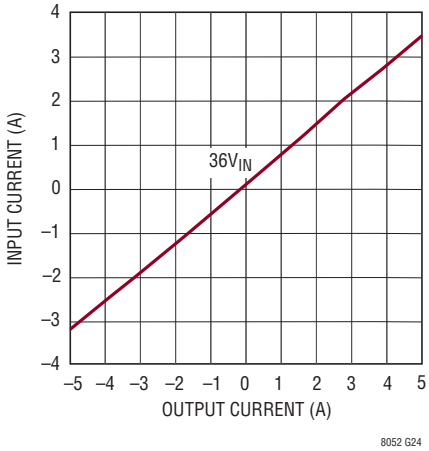
Input Current vs Output Current 12V_{OUT}



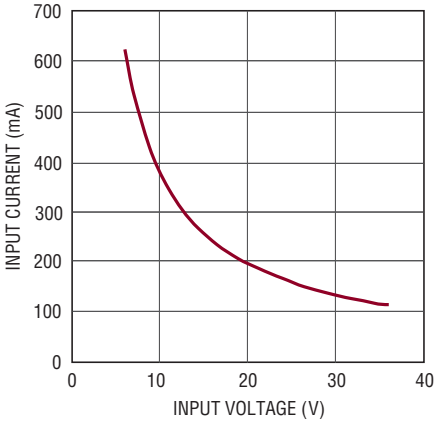
Input Current vs Output Current 18V_{OUT}



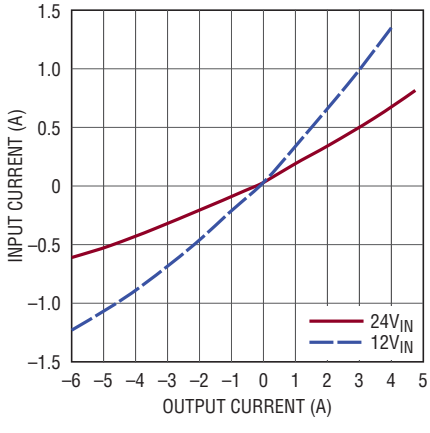
Input Current vs Output Current 24V_{OUT}



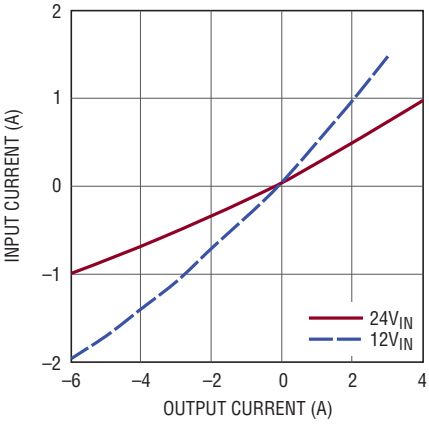
Input Current vs Input Voltage (Output Shorted)



Input Current vs Output Current −3.3V_{OUT}

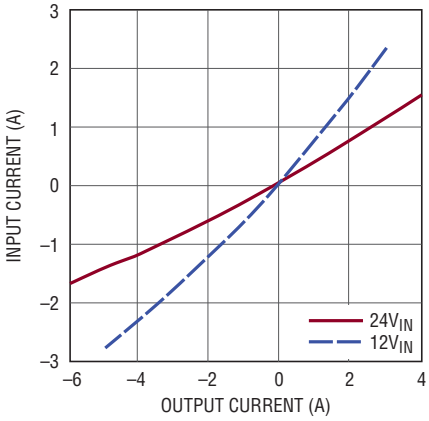


Input Current vs Output Current −5V_{OUT}

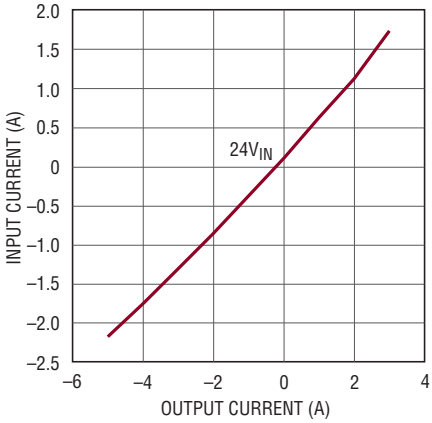


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

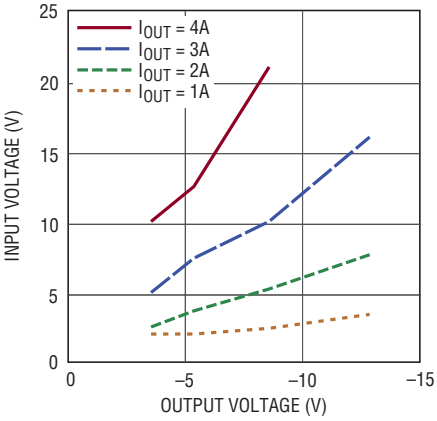
Input Current vs Output Current –8V_{OUT}



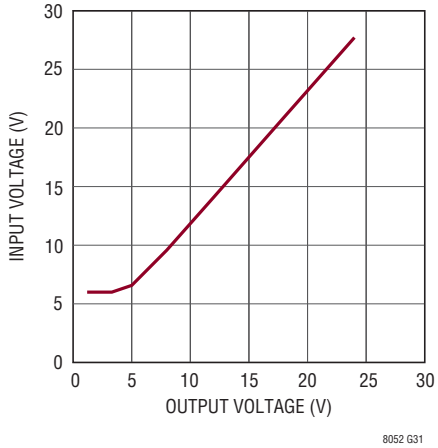
Input Current vs Output Current –12V_{OUT}



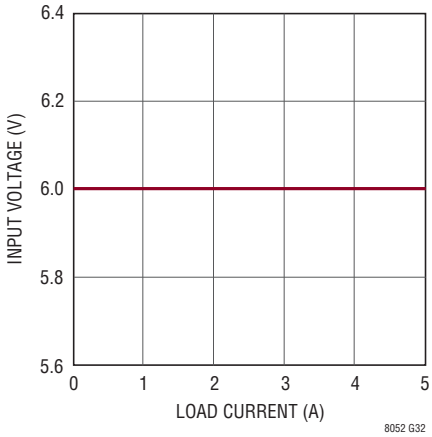
Minimum Required Input Running Voltage vs Negative Output Voltage



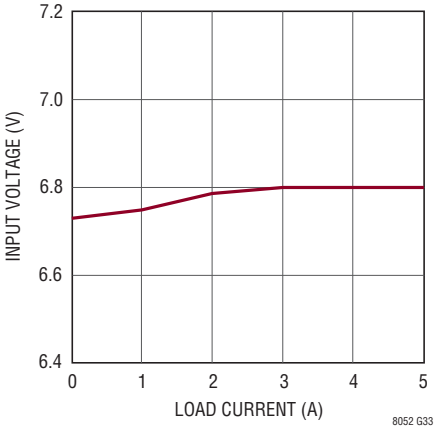
Minimum Required Input Running Voltage vs Output Voltage, I_{OUT} = 5A



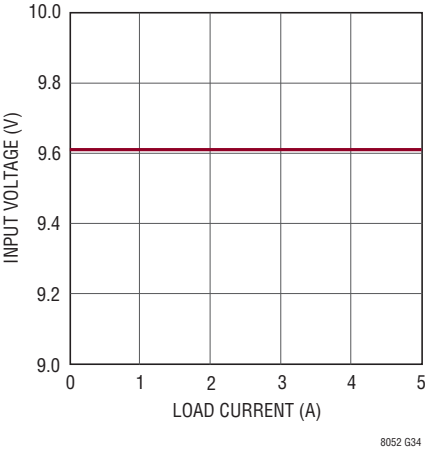
Minimum Required Input Voltage vs Load 3.3V_{OUT} and Below



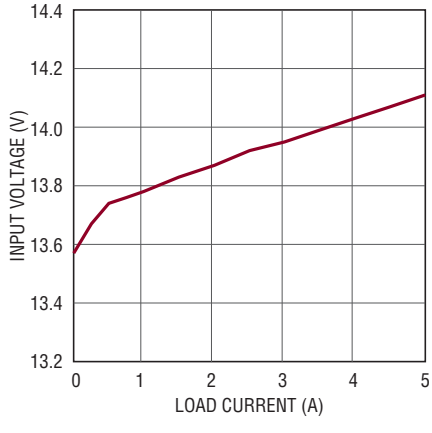
Minimum Required Input Voltage vs Load 5V_{OUT}



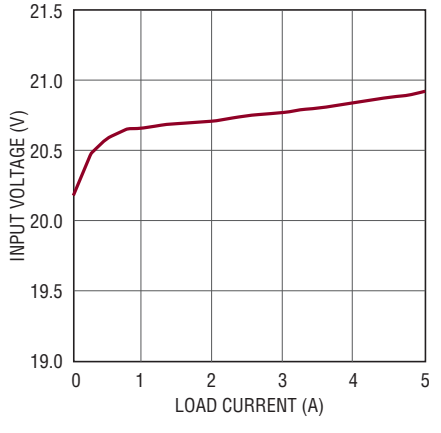
Minimum Required Input Voltage vs Load 8V_{OUT}



Minimum Required Input Voltage vs Load 12V_{OUT}

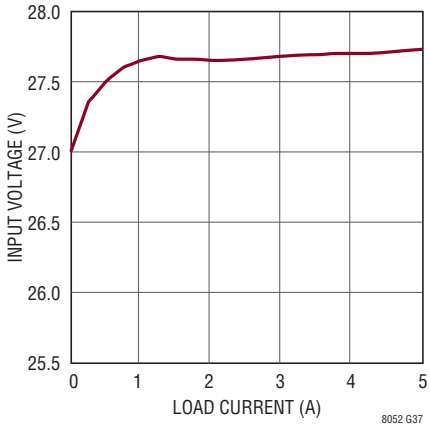


Minimum Required Input Voltage vs Load 18V_{OUT}

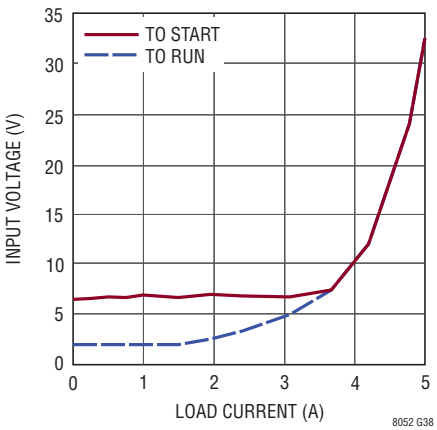


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

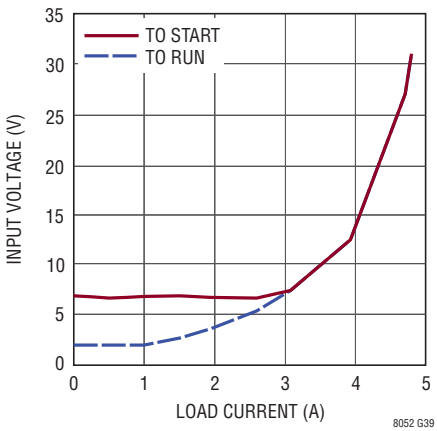
Minimum Required Input Voltage vs Load 24V_{OUT}



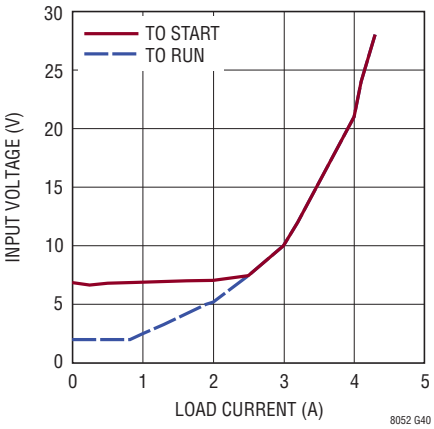
Minimum Required Input Voltage vs Load –3.3V_{OUT}



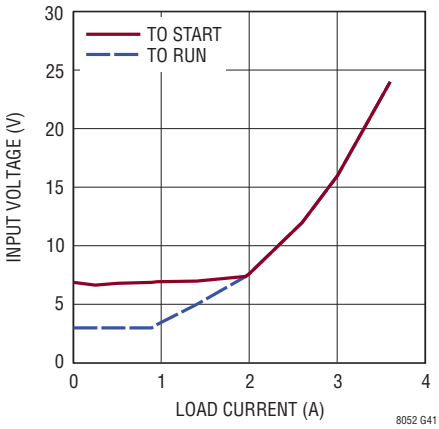
Minimum Required Input Voltage vs Load –5V_{OUT}



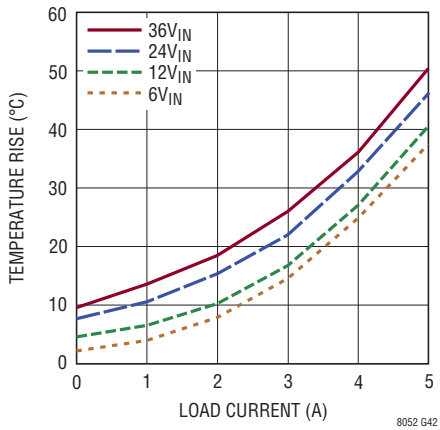
Minimum Required Input Voltage vs Load –8V_{OUT}



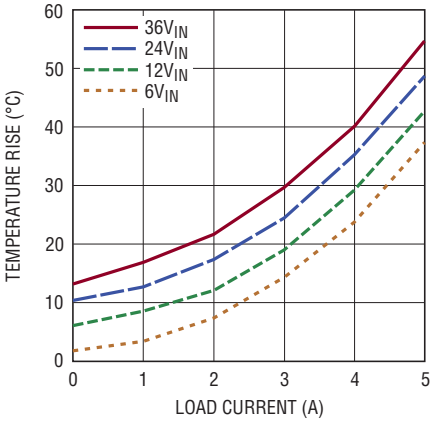
Minimum Required Input Voltage vs Load –12V_{OUT}



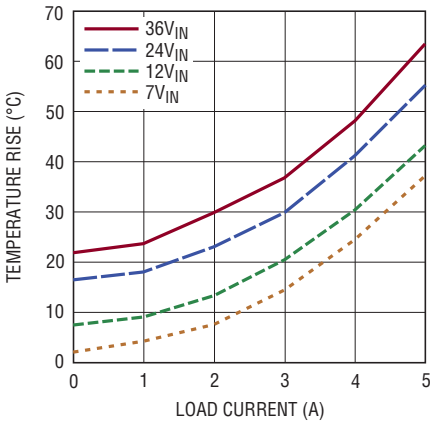
Temperature Rise vs Load Current 2.5V_{OUT}



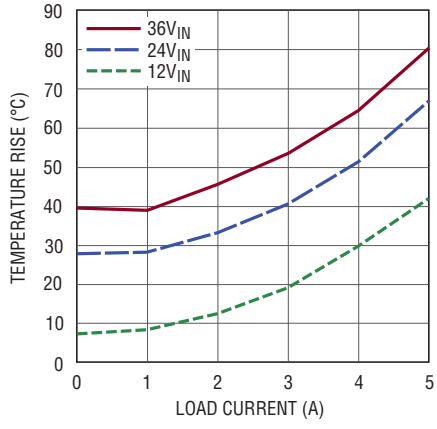
Temperature Rise vs Load Current 3.3V_{OUT}



Temperature Rise vs Load Current 5V_{OUT}

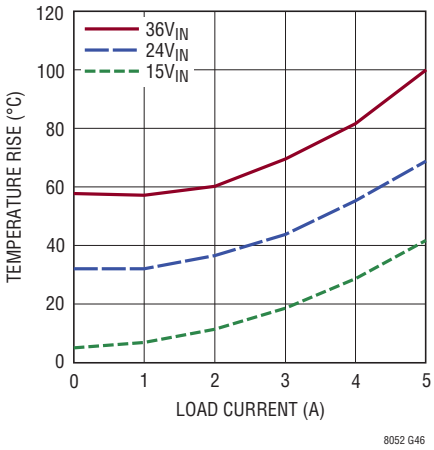


Temperature Rise vs Load Current 8V_{OUT}

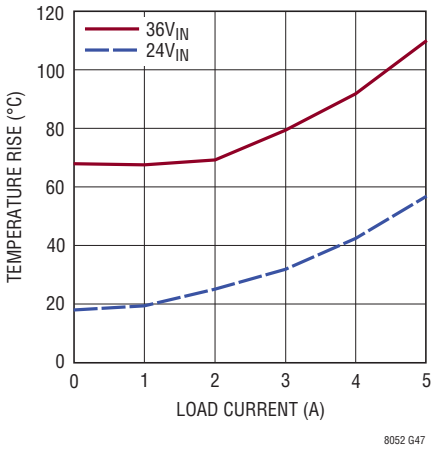


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

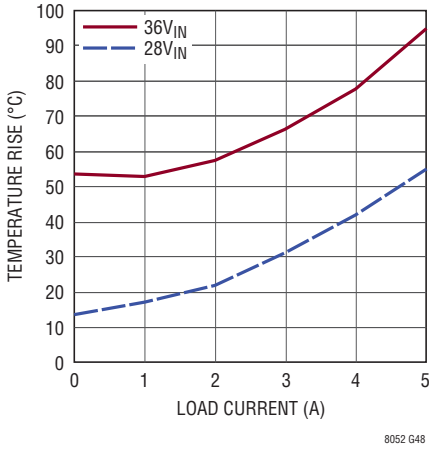
Temperature Rise vs Load Current 12V_{OUT}



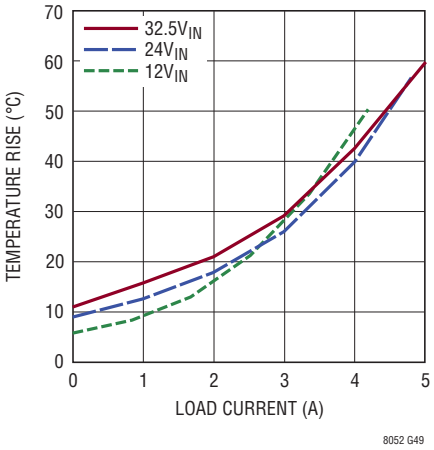
Temperature Rise vs Load Current 18V_{OUT}



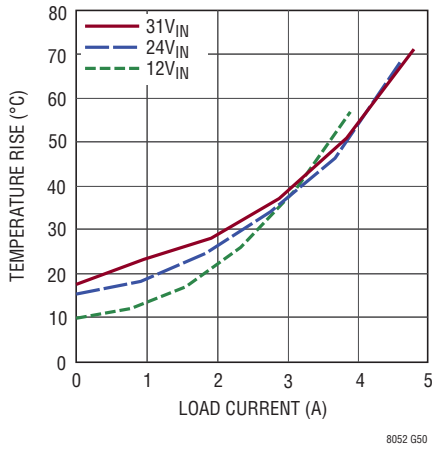
Temperature Rise vs Load Current 24V_{OUT}



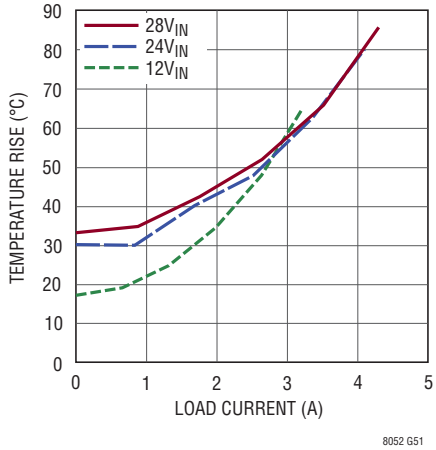
Temperature Rise vs Load Current –3.3V_{OUT}



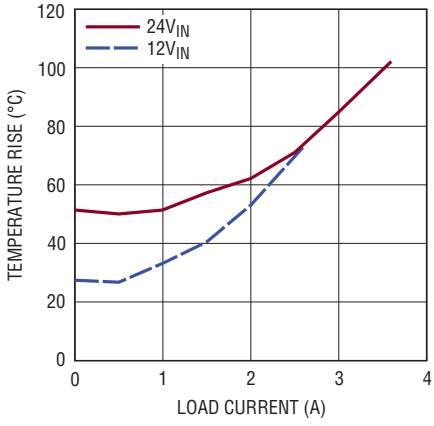
Temperature Rise vs Load Current –5V_{OUT}



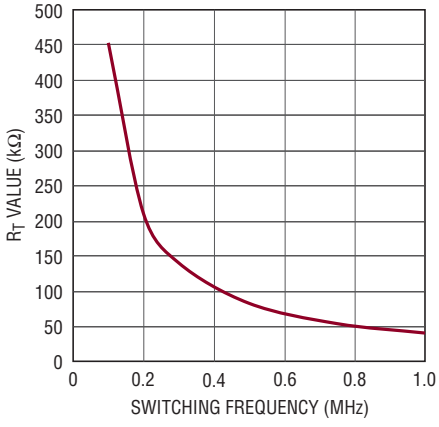
Temperature Rise vs Load Current –8V_{OUT}



Temperature Rise vs Load Current –12V_{OUT}

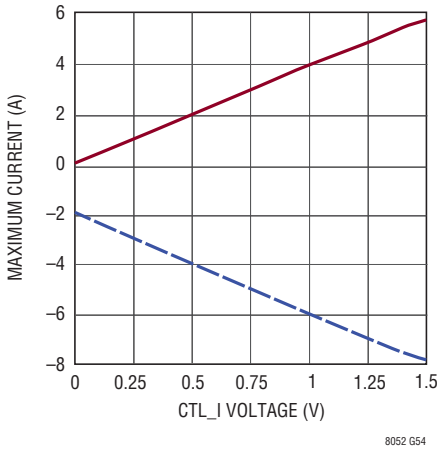


Switching Frequency vs R_T Value

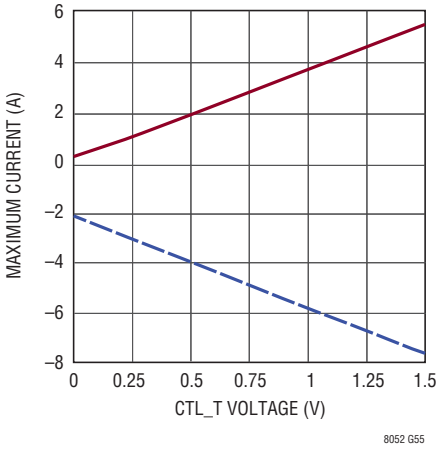


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

CTL_I Voltage vs Maximum Output Current, CTL_T = 2V



CTL_T Voltage vs Maximum Output Current, CTL_I = 2V



PIN FUNCTIONS

V_{OUT} (Bank 1): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins. When reverse current is being driven into the LTM8052/LTM8052A's output by the load, the energy is delivered back through the LTM8052/LTM8052A and out to the V_{IN} pins. Care must be taken to prevent excessive voltage if other devices on the V_{IN} bus cannot absorb this energy. See Input Precautions in the Applications Information section for more details and circuit suggestions.

GND (Bank 2): Tie these GND pins to a local ground plane below the LTM8052/LTM8052A and the circuit components. In most applications, the bulk of the heat flow out of the LTM8052/LTM8052A is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (R_{ADJ}) to this net.

V_{IN} (Bank 3): The V_{IN} pins supply current to the LTM8052/LTM8052A's internal regulator and to the internal power switches. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

CTL_T (Pin D8): Connect a resistor/NTC thermistor network to the CTL_T pin to reduce the maximum regulated output current of the LTM8052/LTM8052A in response to temperature. The maximum control voltage is 1.5V. If this function is not used, tie this pin to V_{REF}.

CTL_I (Pin E8): The CTL_I pin reduces the maximum regulated output current of the LTM8052/LTM8052A. The maximum control voltage is 1.5V. If this function is not used, tie this pin to V_{REF}.

V_{REF} (Pin F8): Buffered 2V Reference Capable of 0.5mA Drive. It is valid when V_{IN} > 6V and RUN is active high.

RT (Pin G8): The RT pin is used to program the switching frequency of the LTM8052/LTM8052A by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. When using the SYNC function, apply a resistor value equivalent to 20% lower than the clock frequency applied to the SYNC pin. Do not leave this pin open.

COMP (Pin H8): Compensation Pin. This pin is generally not used. The LTM8052/LTM8052A is internally compensated, but some rare situations may arise that require a modification to the control loop. This pin connects directly to the input PWM comparator of the LTM8052/LTM8052A. In most cases, no adjustment is necessary. If this function is not used, leave this pin open.

PIN FUNCTIONS

SS (Pin J8): Soft-Start Pin. Place an external capacitor to ground to ramp the output voltage during start-up conditions. The soft-start pin has an 11µA charging current.

ADJ (Pin K8): The LTM8052/LTM8052A regulates its ADJ pin to 1.19V. Connect the adjust resistor from this pin to ground. The value of R_{ADJ} is given by the equation:

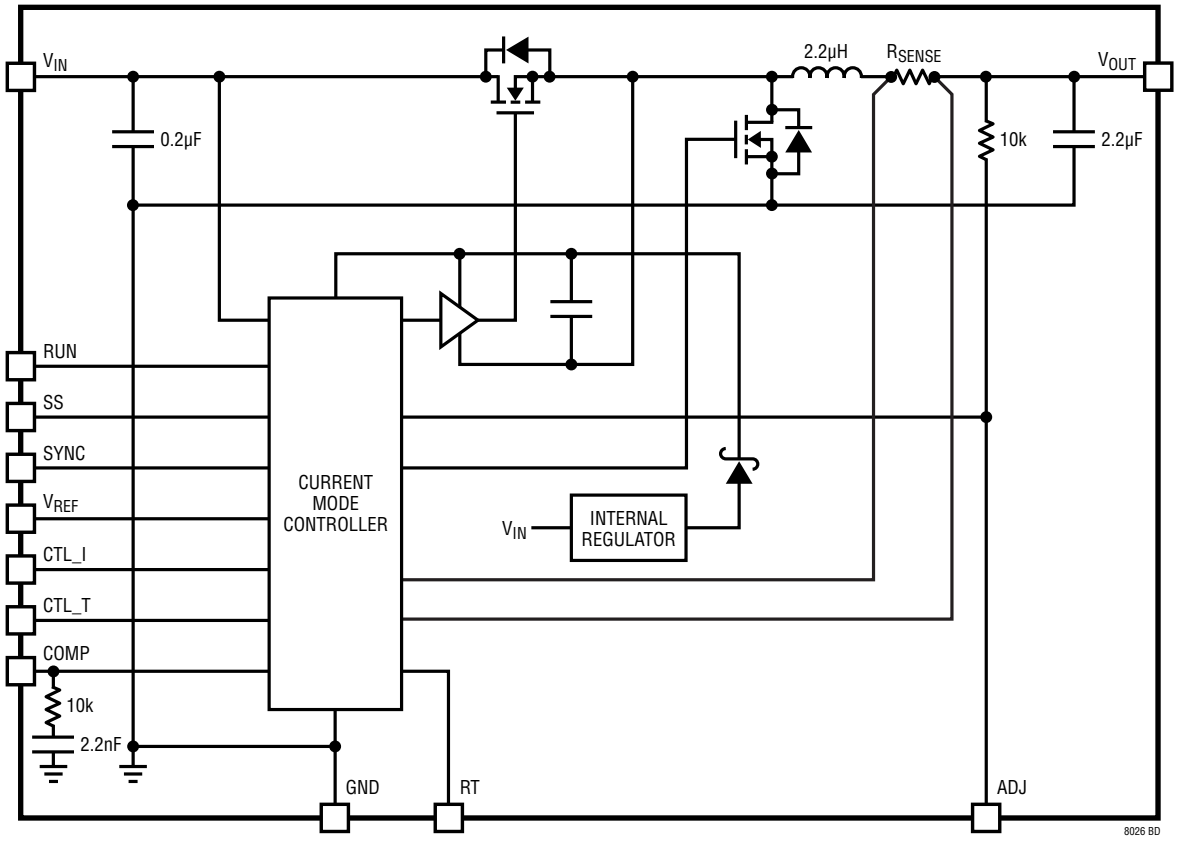
$$R_{ADJ} = \frac{11.9}{V_{OUT} - 1.19}$$

where R_{ADJ} is in kΩ.

RUN (Pin L6): The RUN pin acts as an enable pin and turns on the internal circuitry. It may also be used to implement a precision UVLO. See the Applications Information section for details. The RUN pin is internally clamped, so it may be pulled up to a voltage source that is higher than the absolute maximum voltage of 6V through a resistor, provided the pin current does not exceed 100µA. Do not leave this pin open.

SYNC (Pin L7): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The R_T resistor should be chosen to operate the internal clock at 20% lower than the SYNC pulse frequency. This pin should be grounded when not in use. Do not leave this pin floating. When laying out the board, avoid noise coupling to or from the SYNC trace. See the Synchronization section in Applications Information.

BLOCK DIAGRAM



OPERATION

The LTM8052/LTM8052A is a standalone nonisolated constant-voltage, constant-current step-down switching DC/DC power supply that can deliver up to 5A of positive or 6A of negative output current. This µModule regulator provides a precisely regulated output voltage programmable via one external resistor from 1.2V to 24V. The input voltage range is 6V to 36V. Given that the LTM8052/LTM8052A is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current.

The LTM8052/LTM8052A is a 2-quadrant device, meaning that it can both source and sink current in order to regulate its output voltage. Most traditional voltage regulators are one quadrant; that is, they only source current. If the load, for whatever reason, forces current into a traditional regulator, the output voltage will typically rise. In a similar situation, the LTM8052/LTM8052A will sink current to keep the output voltage in regulation.

It should be clear that the above situation is only possible if the load is providing energy to the LTM8052/LTM8052A output. The LTM8052/LTM8052A will be able to maintain the output voltage at the target regulation point as long as the current from the load does not exceed its negative current limit. If the current does exceed the negative current limit, the LTM8052/LTM8052A output will start to rise. If the output continues to rise, the LTM8052/LTM8052A's output overvoltage protection circuitry will turn off the internal power switches, and the output will be free to rise. The LTM8052A does not respond to an output overvoltage. If the output voltage of either the LTM8052 or the LTM8052A rises above the input, current will flow through an internal power diode. The output will be clamped to a diode drop above the input, and current regulation will be lost.

When the LTM8052/LTM8052A is sinking current, it maintains its output voltage regulation by power conversion, not power dissipation. This means that the energy provided to the LTM8052/LTM8052A is in turn delivered to its input power bus. There must be something on this power bus to accept or use the energy, or the LTM8052/LTM8052A's input voltage will rise. Left unchecked, the energy can raise the input voltage above the absolute maximum voltage and damage the LTM8052/LTM8052A. Please see the Input Precautions section for further details. For applications where only sourcing current (one quadrant operation) is desired, use LTM8026.

The LTM8052/LTM8052A operates in forced continuous mode. This means that the part will not skip cycles when the load approaches zero amps. This may be particularly useful in applications where the synchronization function is used, or any time discontinuous switching is undesirable. The LTM8052/LTM8052A will not operate in forced continuous mode when an input UVLO, output OVLO or minimum duty cycle violation occurs.

As shown in the Block Diagram, the LTM8052/LTM8052A contains a current mode controller, power switches, power inductor, and a modest amount of input and output capacitance.

The LTM8052/LTM8052A utilizes fixed frequency, average current mode control to accurately regulate the inductor current, independent from the output voltage. This is an ideal solution for applications requiring a regulated current source. The control loop will regulate the current in the internal inductor. Once the output has reached the regulation voltage determined by the resistor from the ADJ pin to ground, the inductor current will be reduced by the voltage regulation loop.

The output current loop has two control inputs, determined by the voltage at the analog control pins, CTL_I and CTL_T. CTL_I is typically used to set the maximum allowable current output of the LTM8052/LTM8052A, while CTL_T is typically used with a NTC thermistor to reduce the output current in response to temperature. The lower of the two analog voltages on CTL_I and CTL_T determines the regulated output current. The analog control range of both the CTL_I and CTL_T pin is from 0V to 1.5V. As shown in the Typical Performance Characteristics section, the positive and negative currents are not symmetric. The negative current limit is offset by approximately 2A.

The RUN pin functions as a precision shutdown pin. When the voltage at the RUN pin is lower than 1.55V, switching is terminated. Below the turn-on threshold, the RUN pin sinks 5.5µA. This current can be used with a resistor between RUN and V_{IN} to set a hysteresis. During start-up, the SS pin is held low until the part is enabled, after

OPERATION

which the capacitor at the soft-start pin is charged with an 11µA current source.

The LTM8052/LTM8052A is equipped with a thermal shutdown to protect the device during momentary overload conditions. It is set above the 125°C absolute maximum internal temperature rating to avoid interfering with normal specified operation, so internal device temperatures will exceed the absolute maximum rating when the overtemperature protection is active. So, continuous or repeated activation of the thermal shutdown may impair device reliability. During thermal shutdown, all switching is terminated and the SS pin is driven low.

The switching frequency is determined by a resistor at the RT pin. The LTM8052/LTM8052A may also be synchronized to an external clock through the use of the SYNC pin.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{ADJ} and R_T values.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8052/LTM8052A should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature, applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Many of the output capacitances given in Table 1 specify an electrolytic capacitor. Ceramic capacitors may also be used in the application, but it may be necessary to use more of them. Many high value ceramic capacitors have a large voltage coefficient, so the actual capacitance of the component at the desired operating voltage may be only a fraction of the specified value. Also, the very low ESR of ceramic capacitors may necessitate additional capacitors for acceptable stability margin.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8052/LTM8052A. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8052/LTM8052A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot Plugging Safely section.

APPLICATIONS INFORMATION

Table 1. Recommended Component Values and Configuration.
(T_A = 25°C. See Typical Performance Characteristics for Load Conditions)

V_{IN}	V_{OUT}	C_{IN}	C_{OUT} CERAMIC	C_{OUT} ELECTROLYTIC	R_{ADJ}	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$	f_{MAX}	$R_{T(MIN)}$
6V to 36V	1.2	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	Open	200kHz	210k	250kHz	169k
6V to 36V	1.5	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	38.3k	300kHz	140k	350kHz	118k
6V to 36V	1.8	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	19.6k	350kHz	118k	400kHz	102k
6V to 36V	2.5	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	9.09k	450kHz	90.9k	525kHz	78.7k
6V to 36V	3.3	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	5.62k	550kHz	75.0k	625kHz	64.9k
7V to 36V	5	10µF, 50V, 1210	100µF, 6.3V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	3.09k	600kHz	68.1k	700kHz	57.6k
10V to 36V	8	10µF, 50V, 1210	100µF, 10V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.74k	625kHz	64.9k	750kHz	53.6k
15V to 36V	12	10µF, 50V, 1210	47µF, 16V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.10k	650kHz	61.9k	800kHz	49.9k
22V to 36V	18	10µF, 50V, 1210	22µF, 25V, 1210	47µF, 20V, 45mΩ, OS-CON, 20SVPS47M	604	675kHz	59.0k	900kHz	44.2k
28V to 36V	24	4.7µF, 50V, 1210	10µF, 50V, 1206	47µF, 35V, 30mΩ, OS-CON, 35SVPC47M	523	700kHz	57.6k	1MHz	39.2k
9V to 15V	1.2	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	Open	200kHz	210k	525kHz	78.7k
9V to 15V	1.5	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	38.3k	300kHz	140k	650kHz	61.9k
9V to 15V	1.8	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	19.6k	350kHz	118k	800kHz	49.9k
9V to 15V	2.5	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	9.09k	450kHz	90.9k	1MHz	39.2k
9V to 15V	3.3	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	5.62k	550kHz	75.0k	1MHz	39.2k
9V to 15V	5	10µF, 50V, 1210	100µF, 6.3V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	3.09k	600kHz	68.1k	1MHz	39.2k
10V to 15V	8	10µF, 50V, 1210	100µF, 10V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.74k	625kHz	64.9k	1MHz	39.2k
18V to 36V	1.2	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	Open	200kHz	210k	250kHz	169k
18V to 36V	1.5	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	38.3k	300kHz	140k	350kHz	118k
18V to 36V	1.8	10µF, 50V, 1210	100µF, 6.3V, 1210	470µF, 6.3V, 9mΩ, Chemi-Con, APXF6R3ARA471MH80G	19.6k	350kHz	118k	400kHz	102k
18V to 36V	2.5	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	9.09k	450kHz	90.9k	525kHz	78.7k
18V to 36V	3.3	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	5.62k	550kHz	75.0k	625kHz	64.9k
18V to 36V	5	10µF, 50V, 1210	100µF, 6.3V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	3.09k	600kHz	68.1k	700kHz	57.6k
18V to 36V	8	10µF, 50V, 1210	100µF, 10V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.74k	625kHz	64.9k	750kHz	53.6k
18V to 36V	12	10µF, 50V, 1210	47µF, 16V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.10k	650kHz	61.9k	800kHz	49.9k
2.7V to 32.5V*	–3.3	10µF, 50V, 1210	100µF, 6.3V, 1210	330µF, 4V, 27mΩ, OS-CON, 4SVPC330M	5.62k	550kHz	75.0k	625kHz	64.9k
2V to 31V*	–5	10µF, 50V, 1210	100µF, 6.3V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	3.09k	600kHz	68.1k	700kHz	57.6k
2V to 28V*	–8	10µF, 50V, 1210	100µF, 10V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.74k	625kHz	64.9k	750kHz	53.6k
3V to 24V*	–12	10µF, 50V, 1210	47µF, 16V, 1210	120µF, 16V, 27mΩ, OS-CON, 16SVPC120M	1.10k	650kHz	61.9k	800kHz	49.9k

*Running voltage. See the Typical Performance Characteristics section for starting requirements.
Note: An input bulk capacitor is required.

APPLICATIONS INFORMATION

Programming Switching Frequency

The LTM8052/LTM8052A has an operational switching frequency range between 100kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any circumstance. See Table 2 for resistor values and the corresponding switching frequencies.

Table 2. R_T Resistor Values and Their Resultant Switching Frequencies

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
1	39.2
0.75	53.6
0.5	82.5
0.3	140
0.2	210
0.1	453

In addition, the Typical Performance Characteristics section contains a graph that shows the switching frequency versus R_T value.

Switching Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8052/LTM8052A is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8052/LTM8052A in some fault conditions. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Switching Frequency Synchronization

The nominal switching frequency of the LTM8052/LTM8052A is determined by the resistor from the RT pin to GND and may be set from 100kHz to 1MHz. The internal oscillator may also be synchronized to an external clock through the SYNC pin. The external clock applied to the SYNC pin must have a logic low below 0.6V, a logic high greater than 1.2V and frequency between 100kHz and 1MHz. The input frequency must be 20% higher than the frequency determined by the resistor at the RT pin. Input signals outside of these specified parameters may cause erratic switching behavior and subharmonic oscillations. The SYNC pin must be tied to GND if synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor at the RT pin.

Switching Mode

The LTM8052/LTM8052A operates in forced continuous mode. This means that the part will not skip cycles when the load approaches zero amps. This may be particularly useful in applications where the synchronization function is used, or any time discontinuous switching is undesirable. The LTM8052/LTM8052A will not operate in forced continuous mode when an input UVLO, output OVLO or minimum duty cycle violation occurs.

Soft-Start

The soft-start function controls the slew rate of the power supply output voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing. A capacitor connected from the SS pin to GND programs the slew rate. The capacitor is charged from an internal 11µA current source to produce a ramped output voltage.

APPLICATIONS INFORMATION

Maximum Output Current Adjust

To adjust the regulated load current, an analog voltage is applied to the CTL_I pin or CTL_T pins. Varying the voltage between 0V and 1.5V adjusts the maximum current between the minimum and the maximum current, typically 5.6A positive and 7.7A negative. Graphs of the output current vs CTL_I and CTL_T voltages are given in the Typical Performance Characteristics section. The LTM8052/LTM8052A provides a 2V reference voltage for conveniently applying resistive dividers to set the current limit. The current limit can be set as shown in Figure 1 with the following equation:

$$I_{MAX} = \frac{7.467 \bullet R2}{R1+R2} \text{ Amps (Positive Current)}$$

$$I_{MAX} = -\left[\frac{7.467 \bullet R2}{R1+R2} + 2.1\right] \text{ Amps (Negative Current)}$$

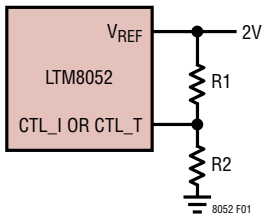


Figure 1. Setting the Output Current Limit

Load Current Derating Using the CTL_T Pin

In high current applications, derating the maximum current based on operating temperature may prevent damage to the load. In addition, many applications have thermal limitations that will require the regulated current to be reduced based on the load and/or board temperature. To achieve this, the LTM8052/LTM8052A uses the CTL_T pin to reduce the effective regulated current in the load. While CTL_I programs the regulated current in the load, CTL_T can be configured to reduce this regulated current based on the analog voltage at the CTL_T pin. The load/board temperature derating is programmed using a resistor network with a temperature dependant resistance (Figure 2). When the board/load temperature rises, the CTL_T voltage will decrease. To reduce the regulated current, the CTL_T voltage must be lower than the voltage at the CTL_I pin. V_{CTL_T} may be higher than V_{CTL_I}, but then it will have no effect.

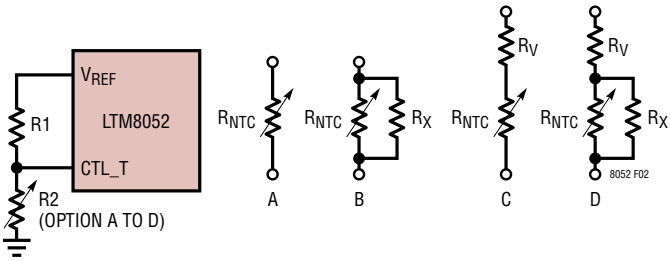


Figure 2. Load Current Derating vs Temperature Using NTC Resistor

Voltage Regulation and Output Overvoltage Protection

The LTM8052/LTM8052A uses the ADJ pin to regulate the output voltage and to provide a high speed overvoltage lockout to avoid high voltage conditions. If the output voltage exceeds 125% of the regulated voltage level (1.5V at the ADJ pin), the LTM8052 terminates switching and shuts down switching for a brief time before restarting. The LTM8052A does not. The regulated output voltage must be greater than 1.19V and is set by the equation:

$$V_{OUT} = 1.19V\left(1+\frac{10k}{R_{ADJ}}\right)$$

where R_{ADJ} is shown in Figure 3.

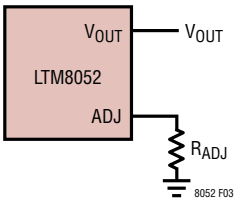


Figure 3. Voltage Regulation and Overvoltage Protection Feedback Connections

APPLICATIONS INFORMATION

In situations where the output of the LTM8052/LTM8052A is required to sink current (that is, the load is driving current into the LTM8052/LTM8052A output), the µModule regulator will maintain voltage regulation as long as the negative current limit is not exceeded. If the current limit is exceeded, the output voltage may begin to rise. If the output voltage rises more than 125% of the target regulation voltage, the output overvoltage protection will engage, and the LTM8052 will stop switching. In this situation, the load will be free to pull up the LTM8052 output. The LTM8052A does not have the output overvoltage protection, making it ideal for applications where the current must remain in regulation even if the output rises above the voltage regulation target. For example, in a thermo-electric cooling (TEC) application, the voltage is not particularly important and an output overvoltage cut-off function could be more of a nuisance than a benefit, so the LTM8052A is a good choice. In a voltage regulation application, output OVP is a nice feature to have to protect the load. In a LED drive, even though it is primarily a current regulation application, choose the LTM8052 in order to use the OVP as an open LED protection.

If the output voltage of either the LTM8052 or the LTM8052A rises above the input, current will flow through an internal power diode. The output will be clamped to a diode drop above the input, and current regulation will be lost.

Thermal Shutdown

If the part is too hot, the LTM8052/LTM8052A engages its thermal shutdown, terminates switching and discharges the soft-start capacitor. When the part has cooled, the part automatically restarts. This thermal shutdown is set to engage at temperatures above the 125°C absolute maximum internal operating rating to ensure that it does not interfere with functionality in the specified operating range. This means that internal temperatures will exceed the 125°C absolute maximum rating when the overtemperature protection is active, possibly impairing the device's reliability.

UVLO and Shutdown

The LTM8052/LTM8052A has an internal UVLO that terminates switching, resets all logic, and discharges the soft-start capacitor when the input voltage is below 6V. The LTM8052/LTM8052A also has a precision RUN function that enables switching when the voltage at the RUN pin rises to 1.68V and shuts down the LTM8052/LTM8052A when the RUN pin voltage falls to 1.55V. There is also an internal current source that provides 5.5µA of pull-down current to program additional UVLO hysteresis. For RUN rising, the current source is sinking 5.5µA until RUN = 1.68V, after which the current source turns off. For RUN falling, the current source is off until the RUN = 1.55V, after which it sinks 5.5µA. The following equations determine the voltage divider resistors for programming the falling UVLO voltage and rising enable voltage (V_{ENA}) as configured in Figure 4.

$$R1 = \frac{1.55V \bullet R2}{UVLO - 1.55V}$$

$$R2 = \frac{V_{ENA} - 1.084 \bullet UVLO}{5.5\mu A}$$

The RUN pin has an absolute maximum voltage of 6V. To accommodate the largest range of applications, there is an internal Zener diode that clamps this pin, so that it can be pulled up to a voltage higher than 6V through a resistor that limits the current to less than 100µA. For applications where the supply range is greater than 4:1, size R2 greater than 375k.

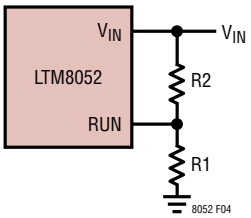


Figure 4. UVLO Configuration

APPLICATIONS INFORMATION

Input Precautions

When the LTM8052/LTM8052A is sinking current, it maintains its output voltage regulation by power conversion, not power dissipation. This means that the energy provided to the LTM8052/LTM8052A is in turn delivered to its input power bus. There must be something on this power bus to accept or use the energy, or the LTM8052/LTM8052A's input voltage will rise. Left unchecked, the energy can raise the input voltage above the absolute maximum voltage rating and damage the LTM8052/LTM8052A.

In many cases, the system load on the LTM8052/LTM8052A input bus will be sufficient to absorb the energy delivered by the µModule regulator. The power required by other devices will consume more than enough to make up for what the LTM8052/LTM8052A delivers. In cases where the LTM8052/LTM8052A is the largest or only power converter, this may not be true and some means may need to be devised to prevent the LTM8052/LTM8052A's input from rising too high. Figure 5a shows a passive crowbar circuit that will dissipate energy during momentary input overvoltage conditions. The breakdown voltage of the zener diode is chosen in conjunction with the resistor R to set the circuit's trip point. The trip point is typically set well above the maximum V_{IN} voltage under normal operating conditions. This circuit does not have a precision threshold, and is subject to both part-to-part and temperature variations, so it is not suitable for applications where high accuracy is required or large voltage margins are not available.

The circuit in Figure 5b also dissipates energy during momentary overvoltage conditions, but is more precise than that in Figure 5a. It uses an inexpensive comparator and the V_{REF} output of the LTM8052/LTM8052A to establish a reference voltage. The optional hysteresis resistor in the comparator circuit avoids MOSFET chatter. Figure 5c shows a circuit that latches on and crowbars the input in an overvoltage event. The SCR latches when the input voltage threshold is exceeded, so this circuit should be used with a fuse, as shown, or employ some other method to interrupt current from the load.

As mentioned, the LTM8052/LTM8052A sinks current by energy conversion and not dissipation. Thus, no matter what protection circuit that is used, the amount of power that the protection circuit must absorb depends upon the amount of power at the input. For example, if the output voltage is 2.5V and can sink 5A, the input protection circuit should be designed to absorb at least 7.5W. In Figures 5a and 5b, let us say that the protection activation threshold is 30V. Then the circuit must be designed to be able to dissipate 7.5W and accept 7.5W/30V = 250mA.

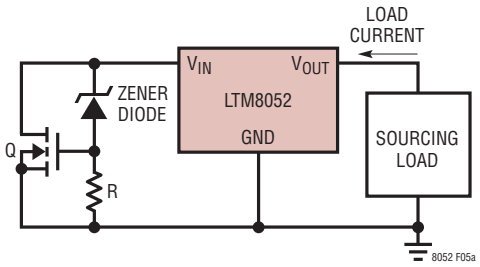


Figure 5a. The MOSFET Q Dissipates Momentary Energy to GND. The Zener Diode and Resistor Are Chosen to Ensure That the MOSFET Turns On Above the Maximum V_{IN} Voltage Under Normal Operation

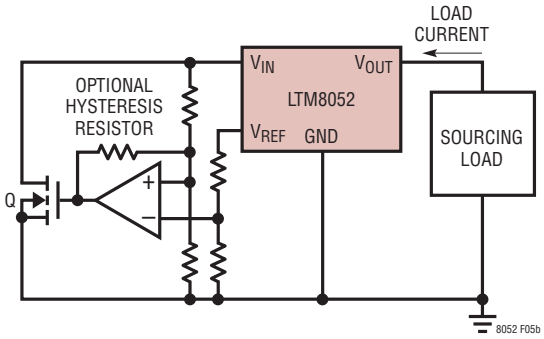


Figure 5b. The Comparator in This Circuit Activates the Q MOSFET at a More Precise Voltage Than the One Shown in Figure 5a. The Reference for the Comparator is Derived from the V_{REF} Pin of the LTM8052/LTM8052A

APPLICATIONS INFORMATION

Figures 5a through 5c are crowbar circuits, which attempt to prevent the input voltage from rising above some level by clamping the input to GND through a power device. In some cases, it is possible to simply turn off the LTM8052/LTM8052A when the input voltage exceeds some threshold. This is possible when the voltage power source that drives current into V_{OUT} never exceeds V_{IN}. An example of this circuit is shown in Figure 5d. When the power source on the output drives V_{IN} above a predetermined threshold, the comparator pulls down on the RUN pin and stops switching in the LTM8052/LTM8052A. When this happens, the input capacitance needs to absorb the energy stored within the LTM8052/LTM8052A's internal inductor, resulting in an additional voltage rise. As shown in the Block Diagram, the internal inductor value is 2.2µH. If the LTM8052/LTM8052A negative current limit is set to 5A, for example, the energy that the input capacitance must absorb is $1/2\,LI^2 = 27.5\mu J$. Suppose the comparator circuit in Figure 5d is set to pull the RUN pin down when $V_{TRIP} = 15V$. The input voltage will rise according to the capacitor energy equation:

$$\frac{1}{2}C\left(V_{IN}^{\,2} - V_{TRIP}^{\,2}\right) = 27.5\mu J$$

If the total input capacitance is 10µF, the input voltage will rise to:

$$27.5\mu J = \frac{1}{2}10\mu F\left(V_{IN}^{\,2} - 15V^{2}\right)$$

$$V_{IN} = 15.2V$$

For applications where only sourcing current (one quadrant operation) is desired, use LTM8026.

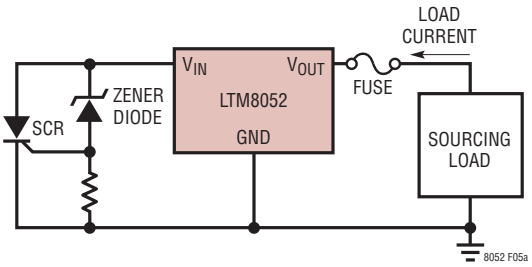


Figure 5c. The SCR Latches On When the Activation Threshold is Reached, So a Fuse or Some Other Method of Disconnecting the Load Should be Used

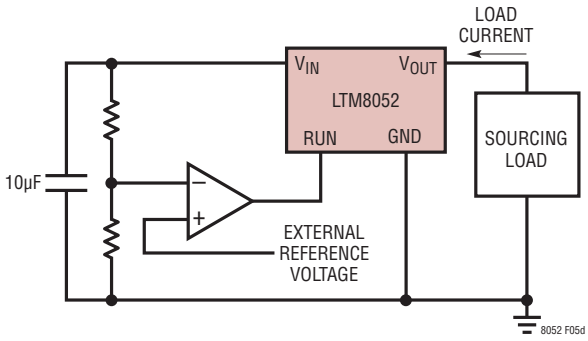


Figure 5d. This Comparator Circuit Turns Off the LTM8052/LTM8052A if the Input Rises Above a Predetermined Threshold. When the LTM8052/LTM8052A Turns Off, the Energy Stored in the Internal Inductor Will Raise V_{IN} a Small Amount Above the Threshold.

APPLICATIONS INFORMATION

No Output Current Sharing

The LTM8052/LTM8052A is a two quadrant device, able to both sink and source current to maintain voltage regulation. It is therefore not suitable for current sharing.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8052/LTM8052A. The LTM8052/LTM8052A is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 6 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{ADJ} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8052/LTM8052A.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8052/LTM8052A.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground currents flow directly adjacent or underneath the LTM8052/LTM8052A.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8052/LTM8052A.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 6. The LTM8052/LTM8052A can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

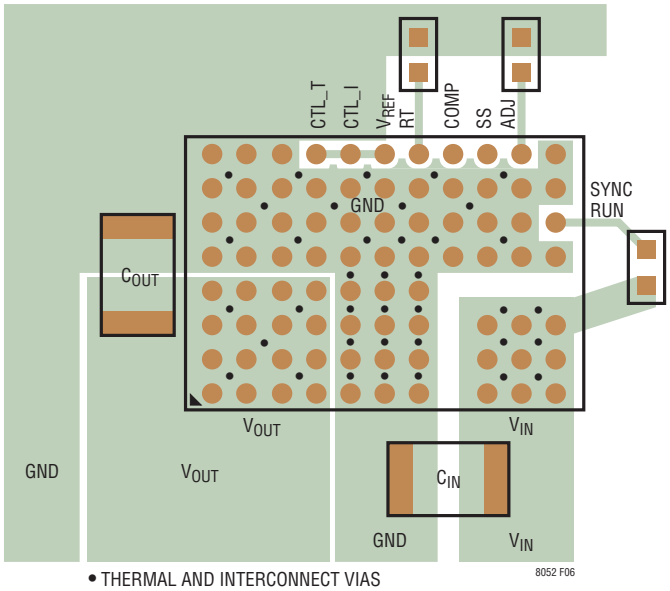


Figure 6. Layout Showing Suggested External Components, GND Plane and Thermal Vias

APPLICATIONS INFORMATION

Hot Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8052/LTM8052A. However, these capacitors can cause problems if the LTM8052/LTM8052A is plugged into a live input supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8052/LTM8052A can ring to more than twice the nominal input voltage, possibly exceeding the LTM8052/LTM8052A's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8052/LTM8052A into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is physically large.

Thermal Considerations

The LTM8052/LTM8052A output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8052/LTM8052A mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use finite element analysis (FEA) to predict thermal performance. To that end, Page 2 of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient

$\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case

θ_{JCtop} – Thermal resistance from junction to top of the product case

θ_{JB} – Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

APPLICATIONS INFORMATION

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a 2-sided, 2-layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 7.

The blue resistances are contained within the µModule device, and the green are outside.

The die temperature of the LTM8052/LTM8052A must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8052/LTM8052A. The bulk of the heat flow out of the LTM8052/LTM8052A is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

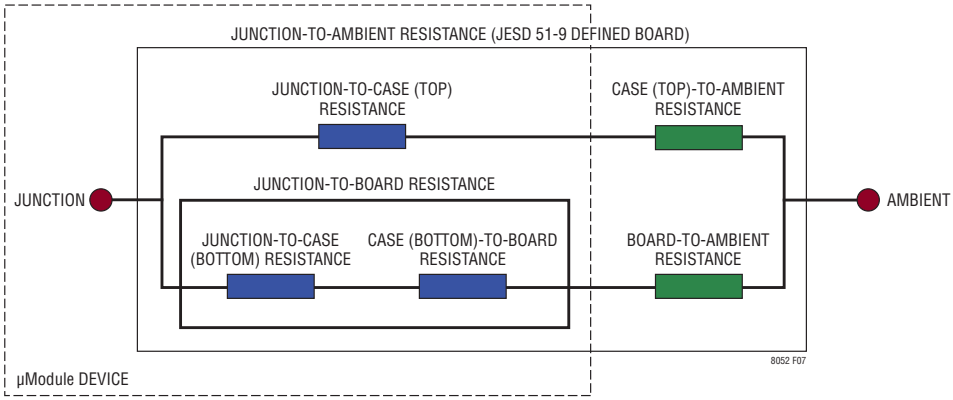
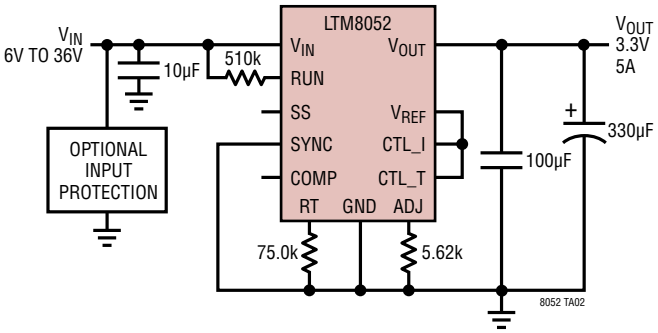


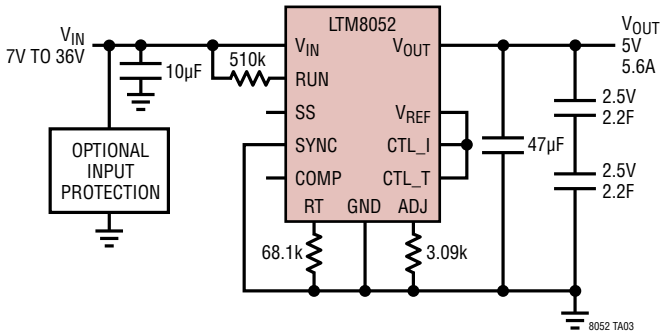
Figure 7. Thermal Resistances Among µModule Device, Printed Circuit Board and Environment

TYPICAL APPLICATIONS

36V_{IN}, 3.3V_{OUT} Step-Down CVCC Converter

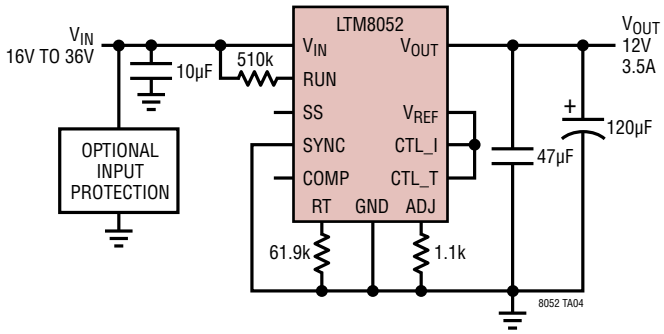


36V_{IN}, LTM8052 Charges Two 2.5V Series Supercapacitors at 5.6A

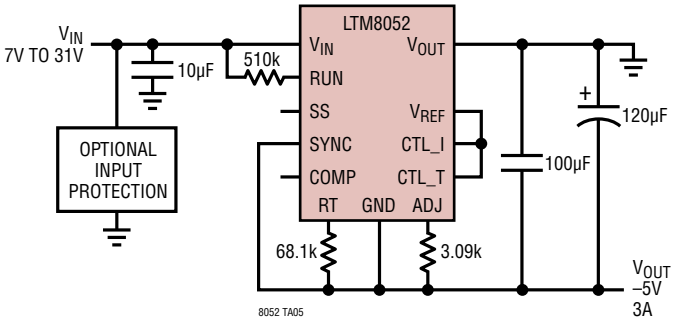


TYPICAL APPLICATIONS

36V_{IN}, 12V_{OUT} Step-Down CVCC Converter

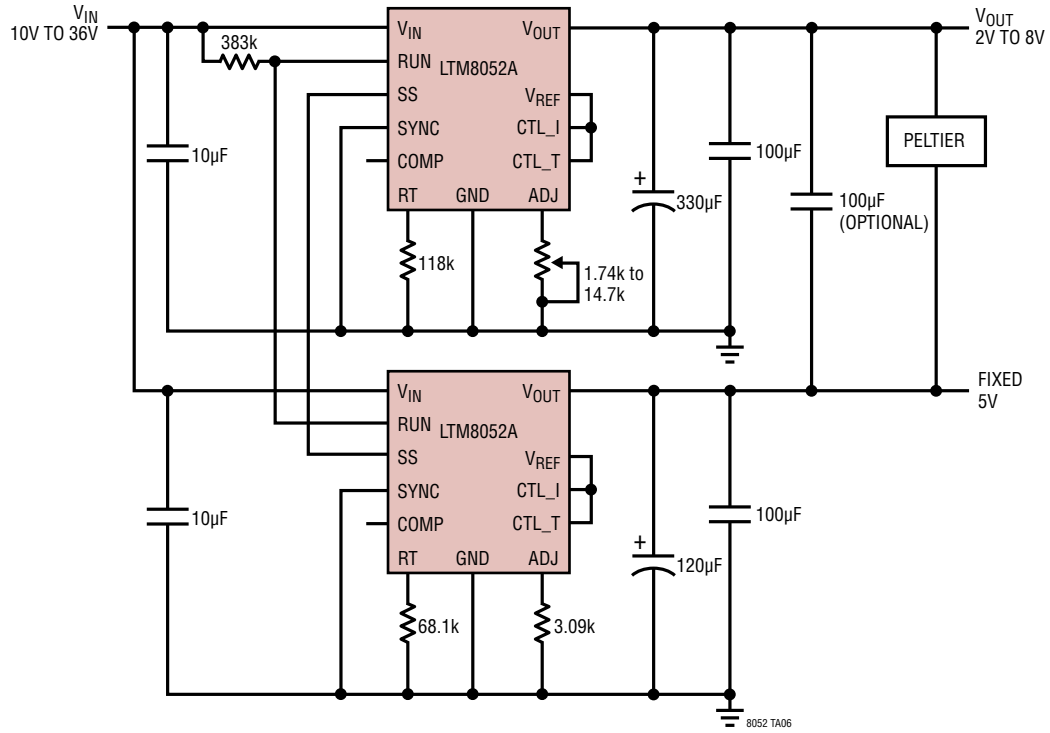


31V_{IN}, –5V_{OUT} Negative Converter

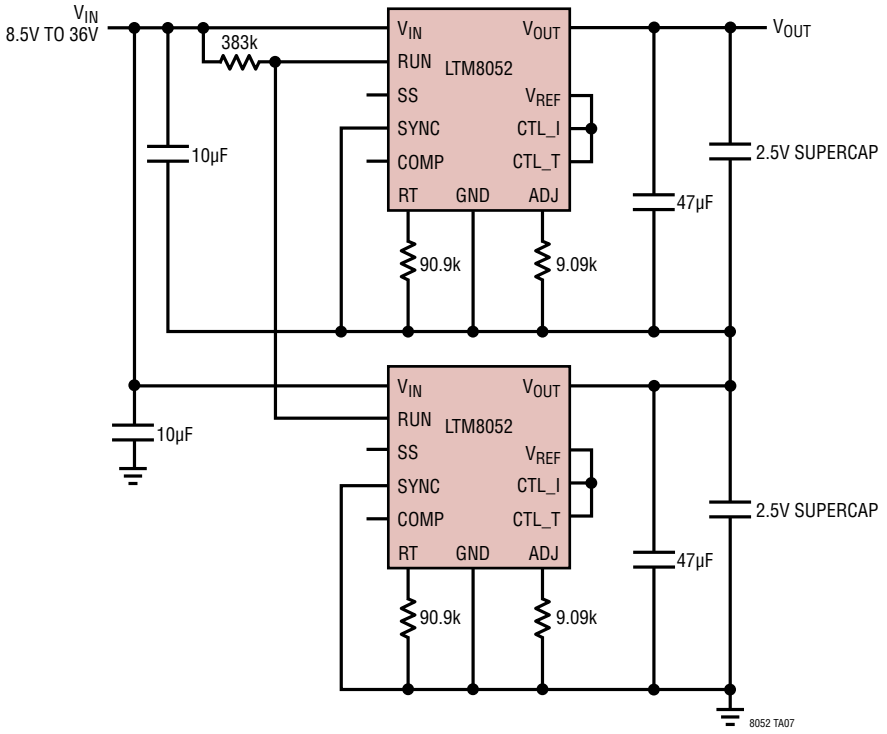


TYPICAL APPLICATIONS

Two LTM8052As Used to Regulate Positive or Negative Voltage (and Current) Across a Peltier Device

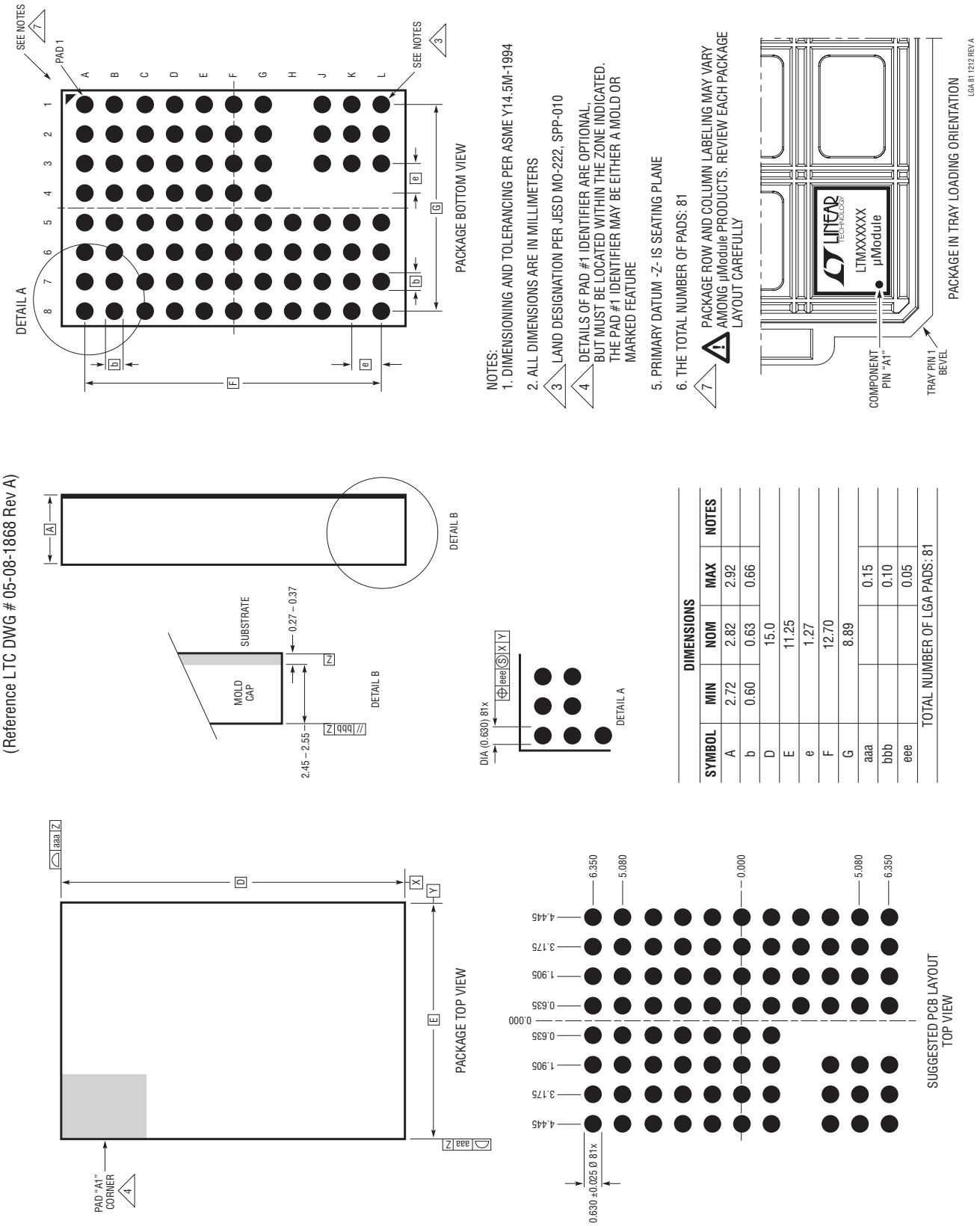


Stack Two LTM8052s to Charge and Actively Balance Supercapacitors (or Batteries)



PACKAGE DESCRIPTION

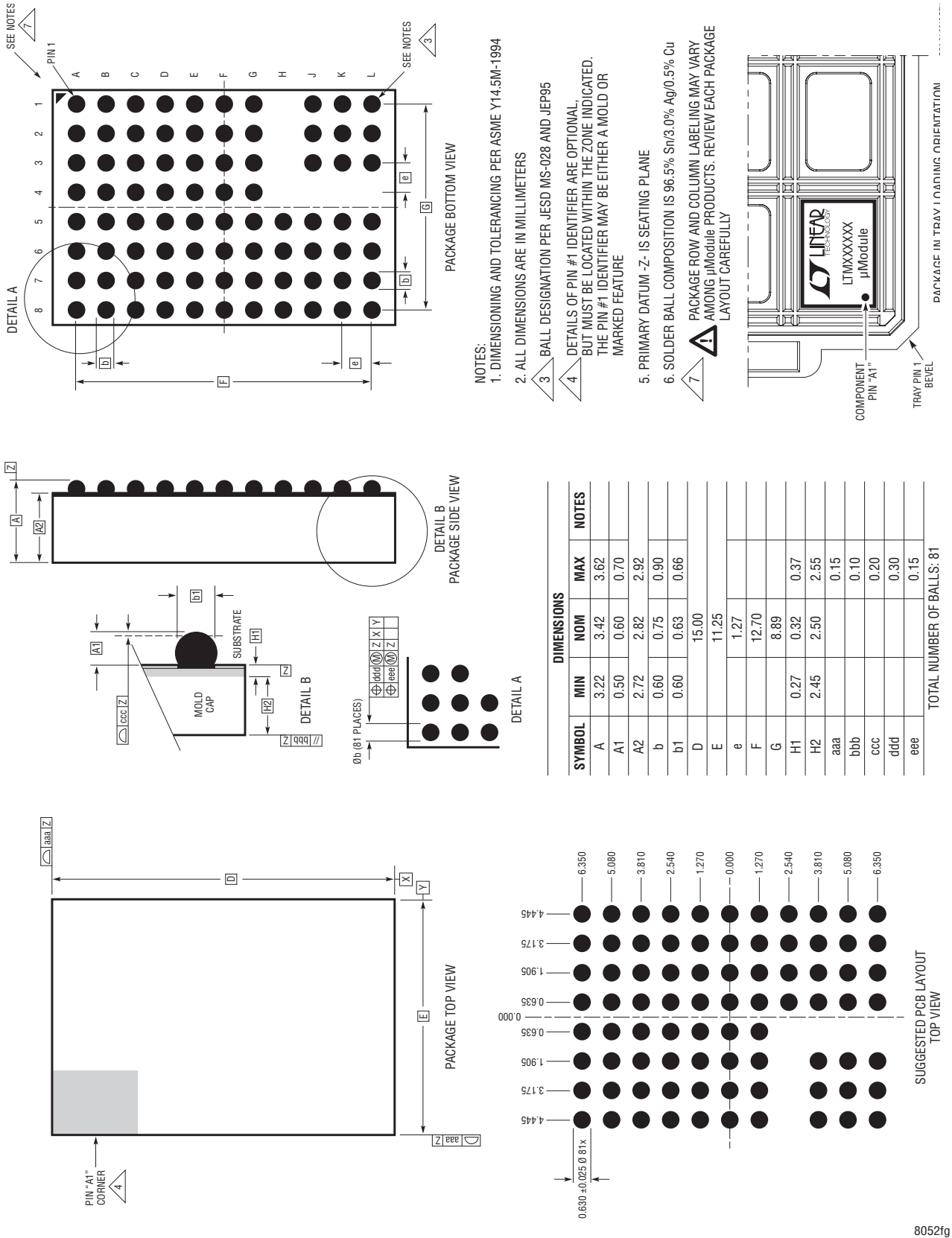
Please refer to http://www.linear.com/product/LTM8052#packaging for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.72	2.82	2.92	
b	0.60	0.63	0.66	
D		15.0		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
aaa			0.15	
bbb			0.10	
eee			0.05	
TOTAL NUMBER OF LGA PADS: 81				

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM8052#packaging for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
H1	0.27	0.32	0.37	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

TOTAL NUMBER OF BALLS: 81

PACKAGE DESCRIPTION

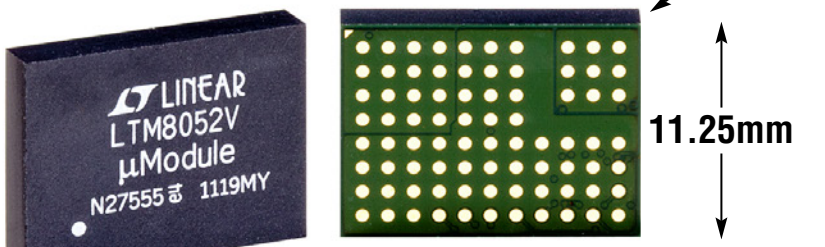
Table 3. Pin Assignment Table (Arranged by Pin Number)

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT}	B1	V_{OUT}	C1	V_{OUT}	D1	V_{OUT}	E1	GND	F1	GND
A2	V_{OUT}	B2	V_{OUT}	C2	V_{OUT}	D2	V_{OUT}	E2	GND	F2	GND
A3	V_{OUT}	B3	V_{OUT}	C3	V_{OUT}	D3	V_{OUT}	E3	GND	F3	GND
A4	V_{OUT}	B4	V_{OUT}	C4	V_{OUT}	D4	V_{OUT}	E4	GND	F4	GND
A5	GND	B5	GND	C5	GND	D5	GND	E5	GND	F5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND	F6	GND
A7	GND	B7	GND	C7	GND	D7	GND	E7	GND	F7	GND
A8	GND	B8	GND	C8	GND	D8	CTL_T	E8	CTL_I	F8	V_{REF}

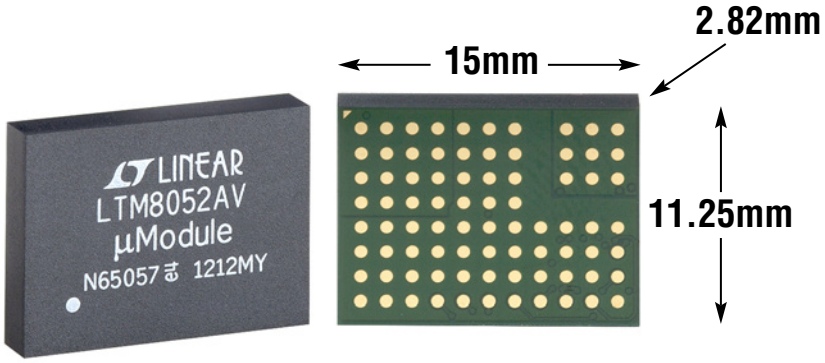
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	–	–	J1	V_{IN}	K1	V_{IN}	L1	V_{IN}
G2	GND	–	–	J2	V_{IN}	K2	V_{IN}	L2	V_{IN}
G3	GND	–	–	J3	V_{IN}	K3	V_{IN}	L3	V_{IN}
G4	GND	–	–	–	–	–	–	–	–
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND
G6	GND	H6	GND	J6	GND	K6	GND	L6	RUN
G7	GND	H7	GND	J7	GND	K7	GND	L7	SYNC
G8	RT	H8	COMP	J8	SS	K8	ADJ	L8	GND

PACKAGE PHOTOS

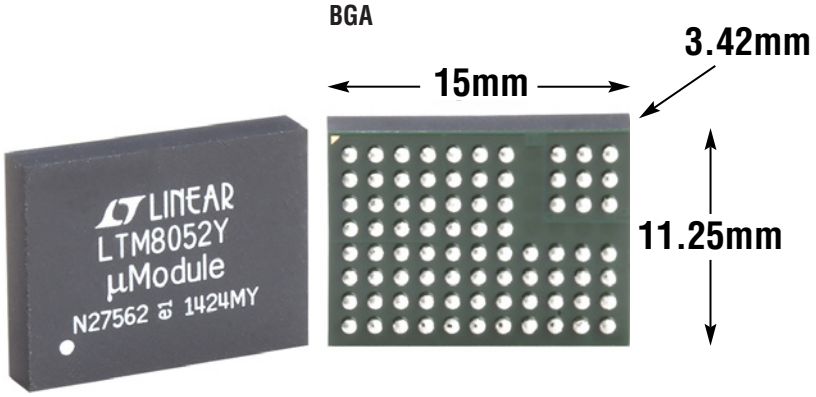
LGA



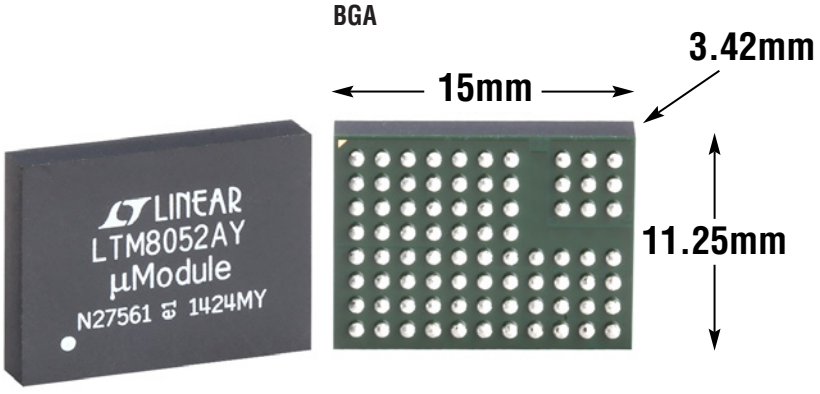
LGA



BGA



BGA

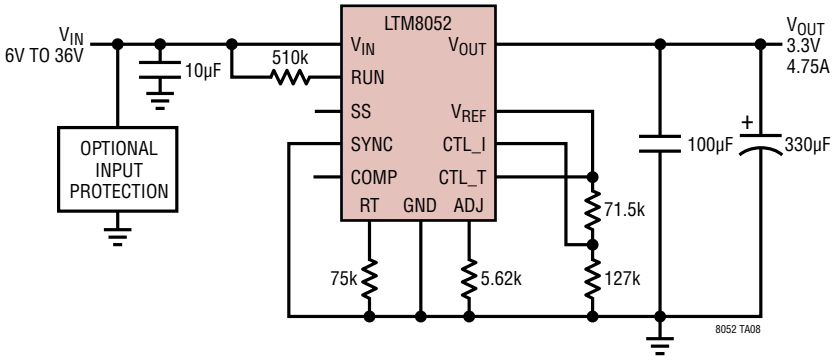


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/12	Modified the Description section.	1
		Updated the Absolute Maximum Ratings and Pin Configuration sections.	2
		Corrected the pin name on schematics using two LTM8052s.	24
		Updated the Related Parts table.	28
B	8/12	Updated the selection table and performance curve.	1
		Added the LTM8052A ordering information.	2
		Updated the Output Overvoltage Protection section.	17
		Modified the Peltier Driver circuit to use LTM8052A.	25
C	5/13	Updated solder temperature from 250°C to 245°C in the Absolute Maximum Ratings section.	2
			18
D	10/13	Added the MP-Grade for LTM8052 and LTM8052A	2
		Corrected Figure Description	24
E	6/14	Added TechClip Video hyperlink	1
		Updated Order Information table	2
		Updated Voltage Regulation and Output Overvoltage Protection sections	16, 17
F	6/15	Added BGA Package	1, 2, 30
G	11/16	Added parentheses to a equation of current limit	17
		Updated the Related Parts table	32

TYPICAL APPLICATION

36V_{IN}, 3.3V_{OUT} Step-Down Converter with 4.75A Accurate Current Limit



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8026	36V_{IN}, 5A Step-Down µModule Regulator with Adjustable Current Limit	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V, Adjustable Current Limit, Parallelable Outputs, CLK Input, 11.25mm × 15mm × 2.82mm LGA Package
LTM8025	36V_{IN}, 3A Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 24V, CLK Input, 9mm × 15mm × 4.32mm LGA Package
LTM8062/ LTM8062A	32V_{IN}, 2A µModule Battery Charger with Maximum Peak Power Tracking (MPPT)	Adjustable V_{BATT} up to 14.4V (18.8V for the LTM8062A), C/10 or Timer Termination, 9mm × 15mm × 4.32mm LGA Package
LTM8027	60V_{IN}, 4A DC/DC Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 60V, 2.5V ≤ V_{OUT} ≤ 24V, 15mm × 15mm × 4.32mm LGA Package
LTM4613	EN55022B Compliant 36V_{IN}, 8A Step-Down µModule Regulator	5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V, Synchronizable, Parallelable, 15mm × 15mm × 4.32mm LGA Package
LTM8064	58V_{IN}, 6A CVCC Step-Down µModule Regulator	6V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 36V, 16mm × 11.9mm × 4.92mm BGA Package
LTM8054	36V_{IN}, 5.4A Buck-Boost µModule Regulator with Current Limit Function	5V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 36V, 11.25mm × 15mm × 3.42mm BGA Package
LTM8055	36V_{IN}, 8.5A Buck-Boost µModule Regulator with Current Limit Function	5V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 36V, 15mm × 15mm × 4.92mm BGA Package
LTM8056	58V_{IN}, 48V_{OUT} Buck-Boost µModule Regulator with Current Limit Function	5V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 48V, 15mm × 15mm × 4.92mm BGA Package
LTM8053	40V_{IN}, 3.5A Step-Down µModule Regurator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA Package