LC²MOS Latchable 4-/8-Channel High Performance Analog Multiplexers

ADG428/ADG429

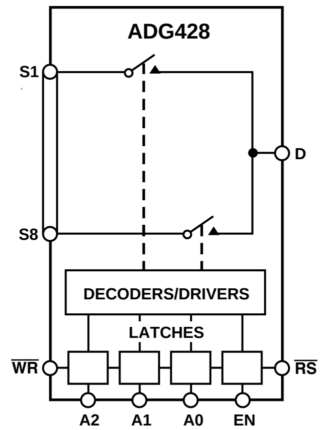
FEATURES

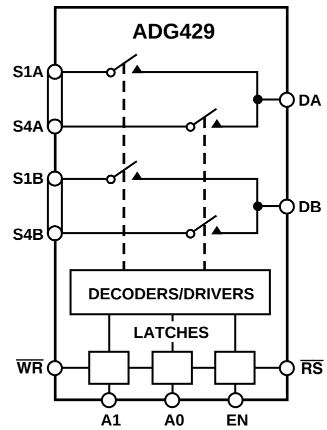
44 V Supply Maximum Ratings
V_{SS} to V_{DD} Analog Signal Range
Low On Resistance (60 Ω typ)
Low Power Consumption (1.6 mW max)
Low Charge Injection (<4 pC typ)
Fast Switching
Break-Before-Make Switching Action
Plug-In Replacement for DG428/DG429

APPLICATIONS

Automatic Test Equipment
Data Acquisition Systems
Communication Systems
Avionics and Military Systems
Microprocessor Controlled Analog Systems
Medical Instrumentation

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The ADG428 and ADG429 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels respectively. On-chip address and control latches facilitate microprocessor interfacing. The ADG428 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG429 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF. All the control inputs, address and enable inputs are TTL compatible over the full specified operating temperature range. This makes the part suitable for bus-controlled systems such as data acquisition systems, process controls, avionics and ATEs because the TTL-compatible address latches simplify the digital interface design and reduce the board space required.

The ADG428/ADG429 are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ADG428/ADG429 are improved replacements for the DG428/DG429 Analog Multiplexers.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG428/ADG429 are fabricated on an enhanced LC²MOS process, giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single/Dual Supply Operation
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG428/ADG429 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

REV. C

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ADG428/ADG429–SPECIFICATIONS

DUAL SUPPLY[1] (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, $\overline{WR}$ = 0 V, $\overline{RS}$ = 2.4 V unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	60		60		Ω typ	V_D = ±10 V, I_S = –1 mA
	100	125	100	125	Ω max	
ΔR_{ON}	10		10		% max	–10 V < V_S < 10 V, I_S = –1 mA
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.03	±0.3	±0.03	±0.3	nA typ	V_D = ±10 V, V_S = ∓10 V;
	±0.5	±50	±0.5	±50	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = ±10 V, V_S = ∓10 V;
ADG428	±0.07	±0.7	±0.07	±0.7	nA typ	Test Circuit 3
	±1	±100	±1	±100	nA max	
ADG429	±0.05	±0.5	±0.05	±0.5	nA typ	
	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = ±10 V;
ADG428	±1	±100	±1	±100	nA max	Test Circuit 4
ADG429	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	±0.1	±1	±0.1	±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	110		110		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	250	300	250	300	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 5
t_{OPEN}		10		10	ns min	R_L = 1 kΩ, C_L = 35 pF; V_S = +5 V; Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	115		115		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	225	150	225	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	105		105		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	300	150	300	ns max	V_S = +5 V; Test Circuit 7
t_W, Write Pulsewidth		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulsewidth		100		100	ns min	V_S = +5 V
Charge Injection	4		4		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 10
OFF Isolation	–75		–75		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	–60		–60		dB min	V_S = 7 V rms, V_{EN} = 0 V; Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz; Test Circuit 12
C_S (OFF)	11		11		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG428	40		40		pF typ	
ADG429	20		20		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG428	54		54		pF typ	
ADG429	34		34		pF typ	
POWER REQUIREMENTS						V_{IN} = 0 V, V_{EN} = 0 V
I_{DD}	20		20		µA typ	
	100		100		µA max	
I_{SS}	0.001		0.001		µA typ	
	5		5		µA max	

NOTES
[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

SINGLE SUPPLY[1] (V_{DD} = +12 V, V_{SS} = 0 V, GND = 0 V, $\overline{WR}$ = 0 V, $\overline{RS}$ = 2.4 V unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	90		90		Ω typ	V_D = +10 V, I_S = –500 µA
		200		200	Ω max	
ΔR_{ON}	10		10		% max	0 V < V_S < 10 V, I_S = –1 mA
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.005		±0.005		nA typ	V_D = 10 V/0 V, V_S = 0 V/10 V;
	±0.5	±50	±0.5	±50	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = 10 V/0 V, V_S = 0 V/10 V;
ADG428	±0.015		±0.015		nA typ	Test Circuit 3
	±1	±100	±1	±100	nA max	
ADG429	±0.008		±0.008		nA typ	
	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = 10 V/0 V;
ADG428	±0.02		±0.02		nA typ	Test Circuit 4
	±1	±100	±1	±100	nA max	
ADG429	±0.01		±0.01		nA max	
	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	250		250		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	350	450	350	450	ns max	V_{S1} = 10 V/0 V, V_{S8} = 0 V/10 V;
						Test Circuit 5
t_{OPEN}	25	10	25	10	ns min	R_L = 1 kΩ, C_L = 35 pF;
						V_S = +5 V; Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	200		200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	80		80		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_S = +5 V; Test Circuit 7
t_W, Write Pulsewidth		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulsewidth		100		100	ns min	V_S = +5 V
Charge Injection	4		4		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 10 nF;
						Test Circuit 10
OFF Isolation	–75		–75		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	–60		–60		dB min	V_S = 7 V rms, V_{EN} = 0 V; Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
						Test Circuit 12
C_S (OFF)	11		11		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG428	40		40		pF typ	
ADG429	20		20		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG428	54		54		pF typ	
ADG429	34		34		pF typ	
POWER REQUIREMENTS						V_{IN} = 0 V, V_{EN} = 0 V
I_{DD}	20		20		µA typ	
	100		100		µA max	

NOTES

[1] Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

[2] Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted.)

V_{DD} to V_{SS} . . . . +44 V
V_{DD} to GND . . . . –0.3 V to +25 V
V_{SS} to GND . . . . +0.3 V to –25 V
Analog, Digital Inputs[2] . . . . V_{SS} – 2 V to V_{DD} + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D . . . . 30 mA
Peak Current, S or D . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
  Industrial (B Version) . . . . –40°C to +85°C
  Extended (T Version) . . . . –55°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . +150°C
Cerdip Package, Power Dissipation . . . . 900 mW
  θ_{JA}, Thermal Impedance . . . . 73°C/W
  Lead Temperature, Soldering (10 sec) . . . . +300°C
Plastic Package, Power Dissipation . . . . 470 mW
  θ_{JA}, Thermal Impedance . . . . 115°C/W
  Lead Temperature, Soldering (10 sec) . . . . +260°C
SOIC Package, Power Dissipation . . . . 600 mW
  θ_{JA}, Thermal Impedance . . . . 77°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
PLCC Package, Power Dissipation . . . . 800 mW
  θ_{JA}, Thermal Impedance . . . . 90°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

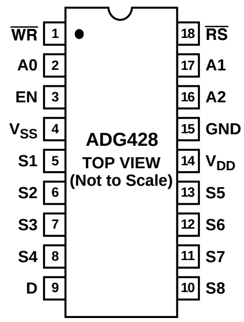
ORDERING GUIDE

Model[1]	Temperature Range	Package Options[2]
ADG428BN	–40°C to +85°C	N-18
ADG428BP	–40°C to +85°C	P-20A
ADG428BR	–40°C to +85°C	R-18
ADG428TQ	–55°C to +125°C	Q-18
ADG429BN	–40°C to +85°C	N-18
ADG429BP	–40°C to +85°C	P-20A
ADG429TQ	–55°C to +125°C	Q-18

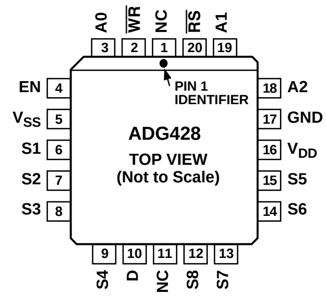
NOTES
[1]For availability of MIL-STD-883, Class B processed parts, contact factory.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC).

ADG428 PIN CONFIGURATIONS

DIP/SOIC



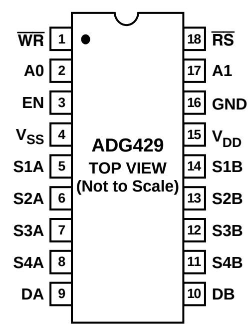
PLCC



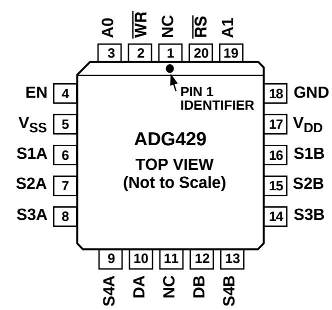
NC = NO CONNECT

ADG429 PIN CONFIGURATIONS

DIP



PLCC



NC = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG428/ADG429 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for "OFF" condition.
C_D (OFF)	Channel output capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for Logic "0."
V_{INH}	Minimum input voltage for Logic "1."
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

ADG428 Truth Table

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching						
X	X	X	X	$\uparrow$	1	Maintains Previous Switch Condition
Reset						
X	X	X	X	X	0	NONE (Latches Cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

ADG429 Truth Table

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
Latching					
X	X	X	$\uparrow$	1	Maintains Previous Switch Condition
Reset					
X	X	X	X	0	NONE (Latches Cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

TIMING DIAGRAMS

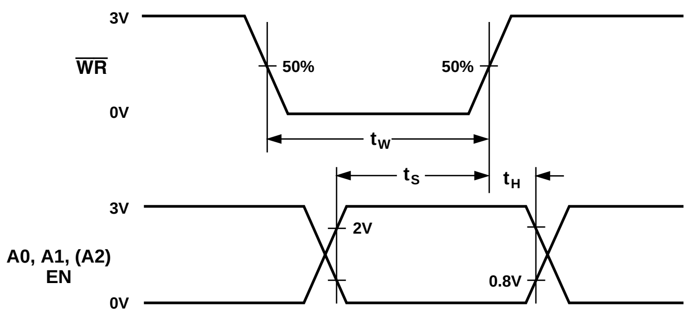


Figure 1.

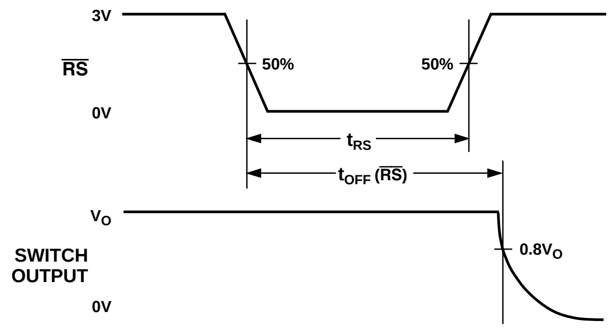


Figure 2.

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

Figure 2 shows the Reset Pulsewidth, t_{RS}, and the Reset Turnoff Time, t_{OFF}, ($\overline{RS}$).

Note: All digital input signals rise and fall times are measured from 10% to 90% of 3 V. tr = tf = 20 ns.

Typical Characteristics

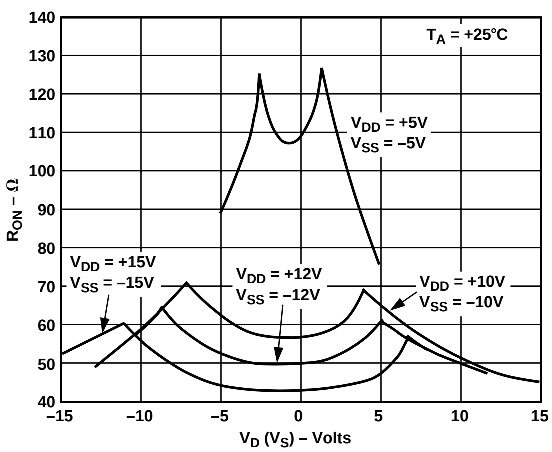


Figure 3. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage

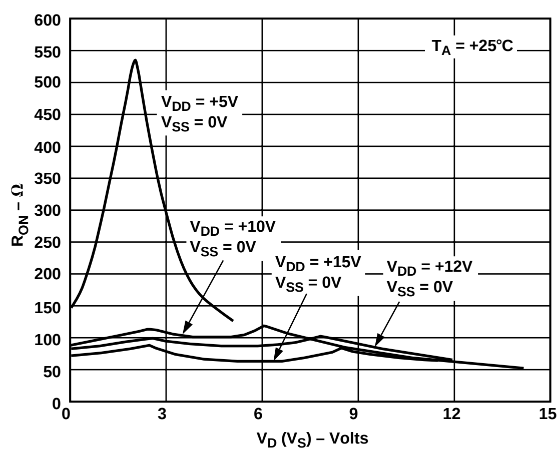


Figure 5. R_{ON} as a Function of V_D (V_S): Single Supply Voltage

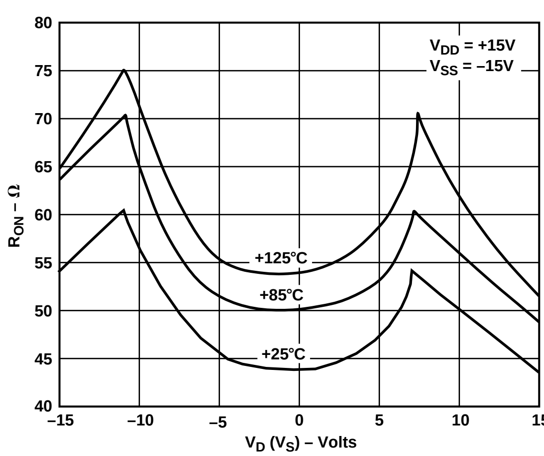


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

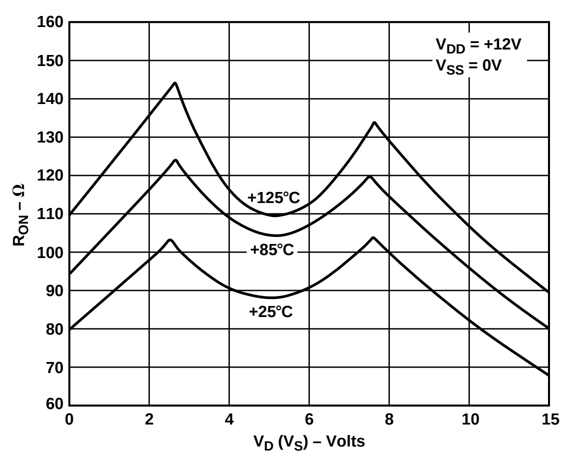


Figure 6. R_{ON} as a Function of V_D (V_S) for Different Temperatures

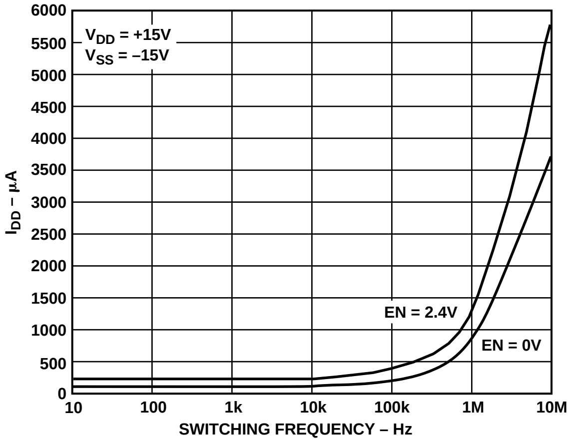


Figure 7. Positive Supply Current vs. Switching Frequency

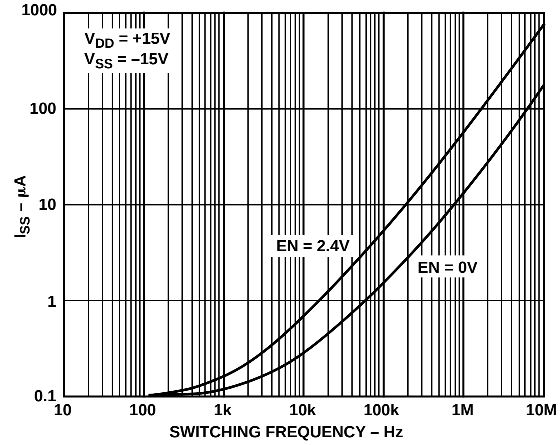


Figure 10. Negative Supply Current vs. Switching Frequency

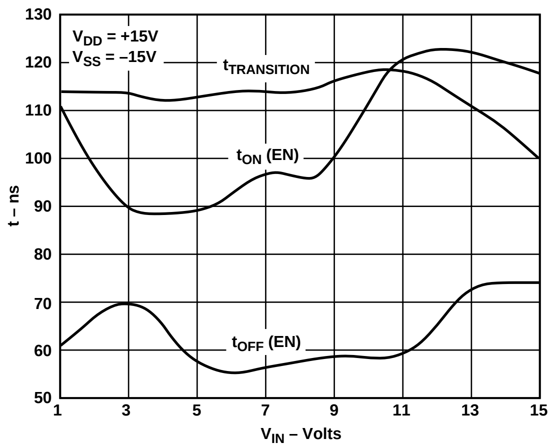


Figure 8. Switching Time vs. V_{IN} (Bipolar Supply)

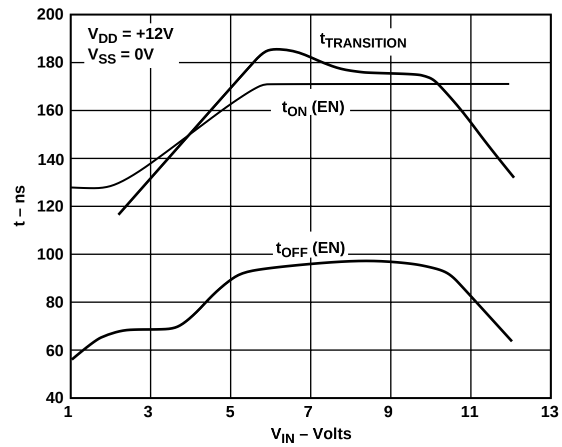


Figure 11. Switching Time vs. V_{IN} (Single Supply)

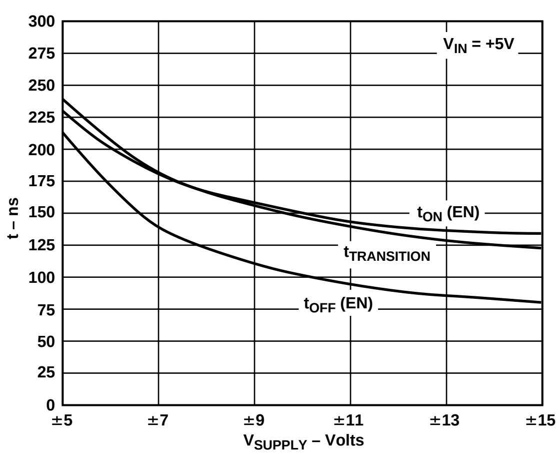


Figure 9. Switching Time vs. Bipolar Supply

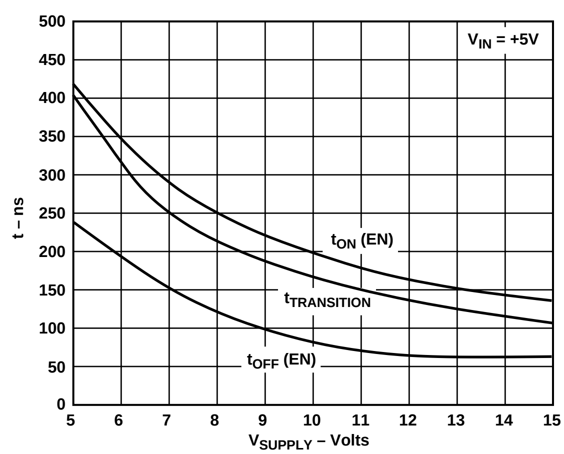


Figure 12. Switching Time vs. Single Supply

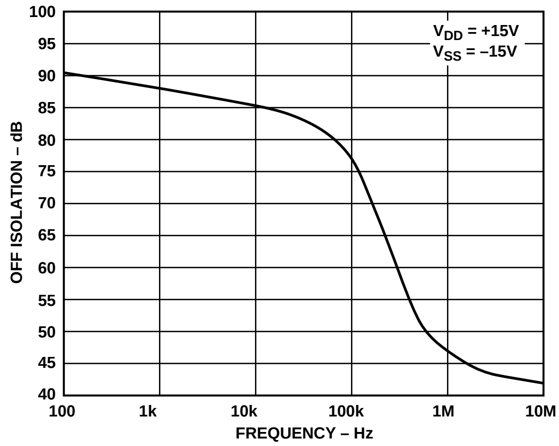


Figure 13. OFF Isolation vs. Frequency

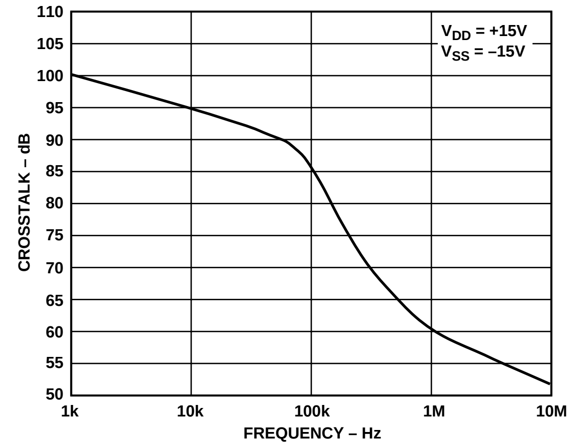


Figure 15. Crosstalk vs. Frequency

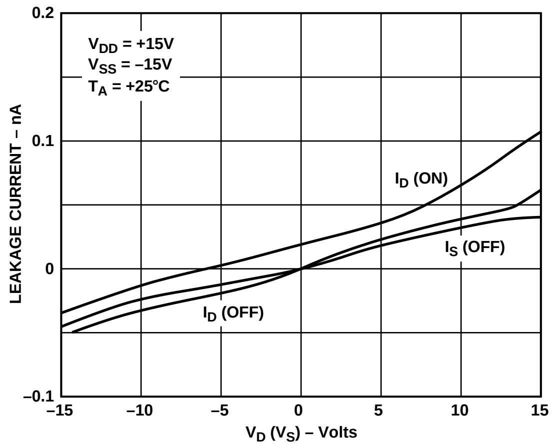


Figure 14. Leakage Currents as a Function of V_D (V_S)

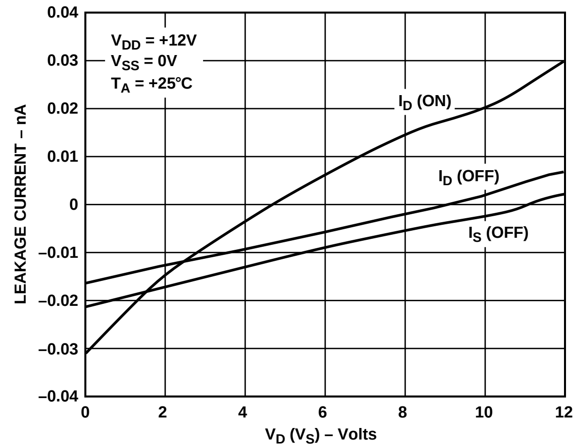
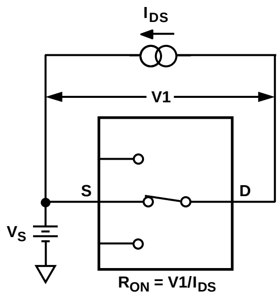
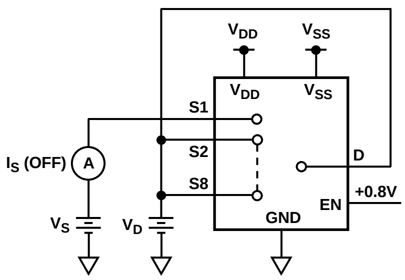


Figure 16. Leakage Currents as a Function of V_D (V_S)

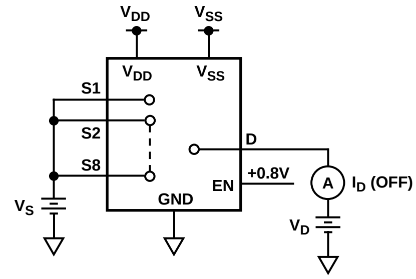
TEST CIRCUITS



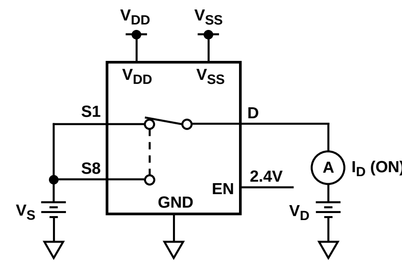
Test Circuit 1. On Resistance



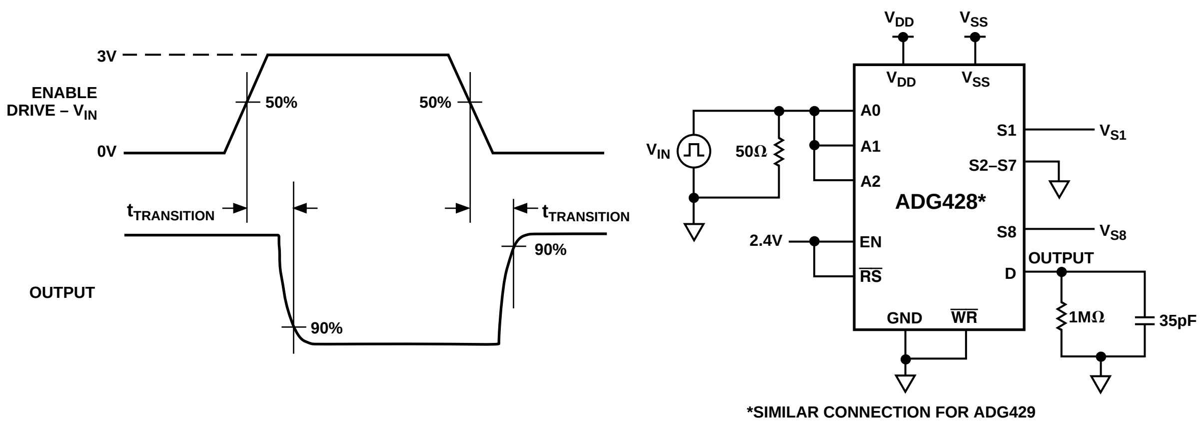
Test Circuit 2. I_S (OFF)



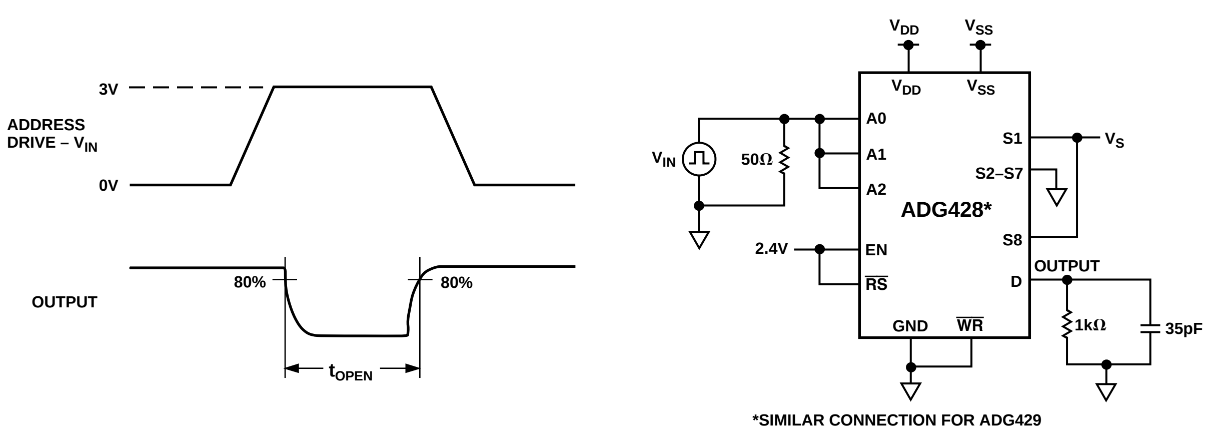
Test Circuit 3. I_D (OFF)



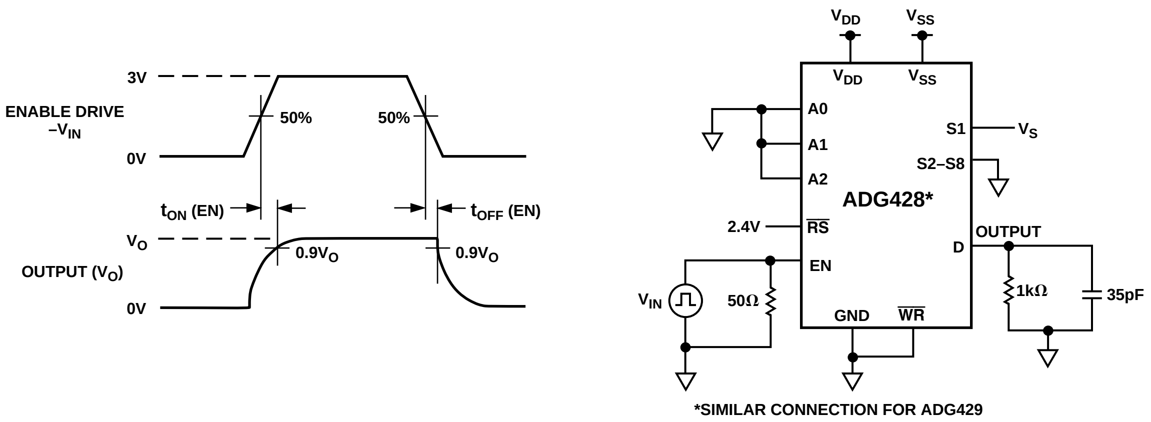
Test Circuit 4. I_D (ON)



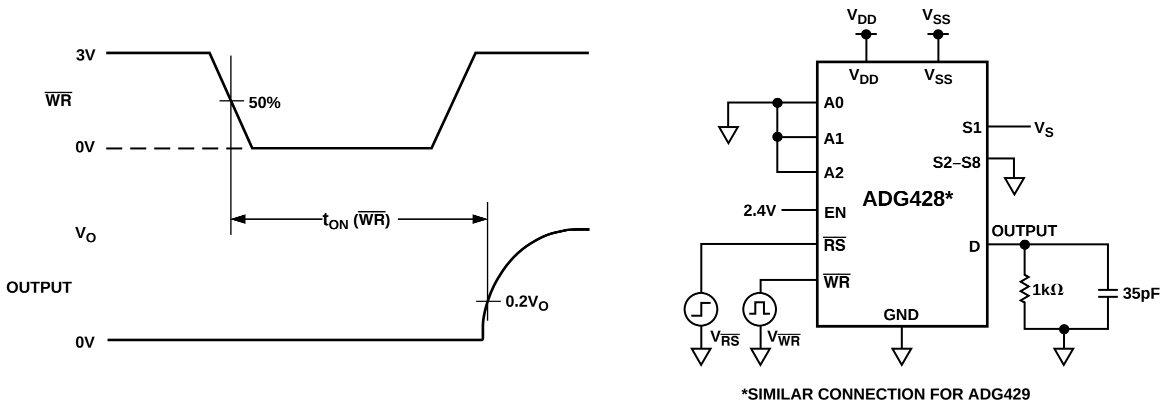
Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$



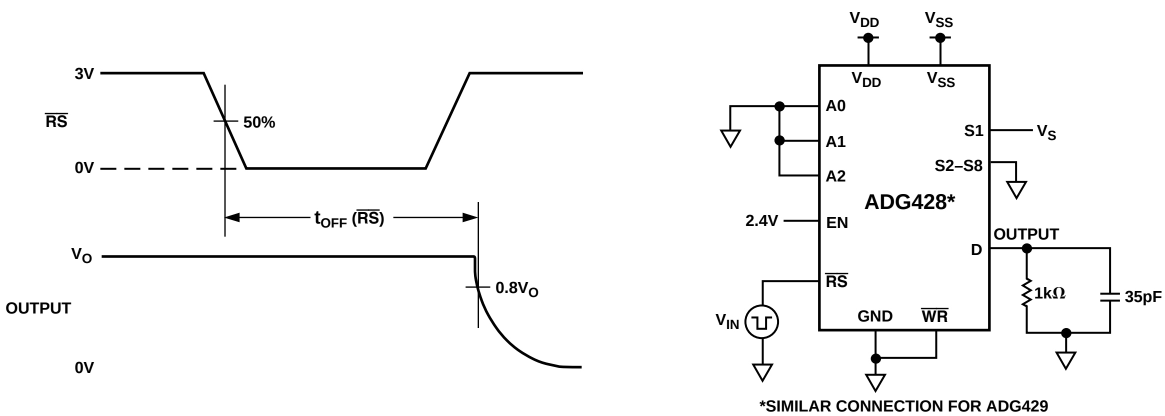
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}



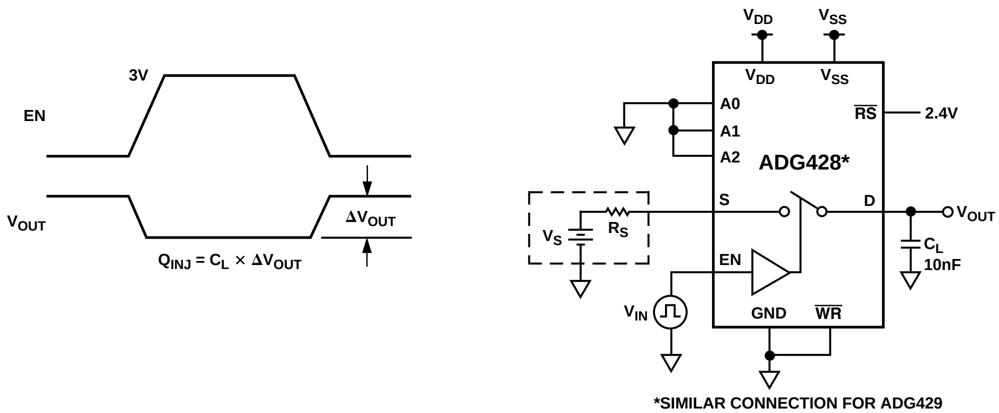
Test Circuit 7. Enable Delay, t_{ON} (EN), t_{OFF} (EN)



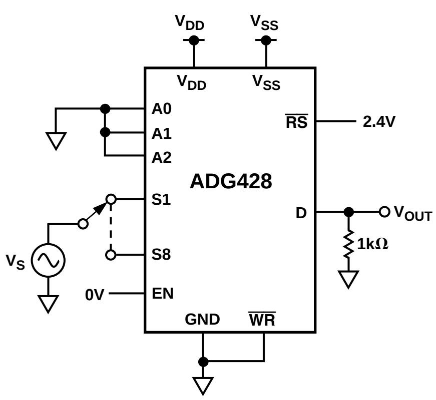
Test Circuit 8. Write Turn-On Time, t_{ON} ($\overline{WR}$)



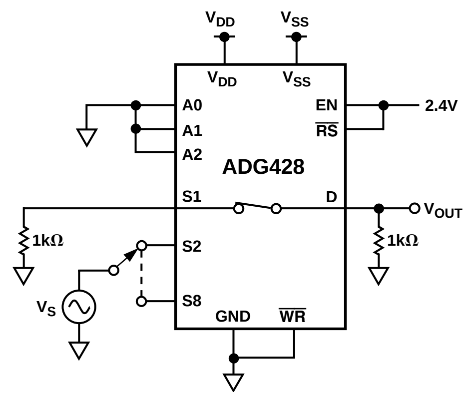
Test Circuit 9. Reset Turn-Off Time, t_{OFF} ($\overline{RS}$)



Test Circuit 10. Charge Injection



Test Circuit 11. OFF Isolation

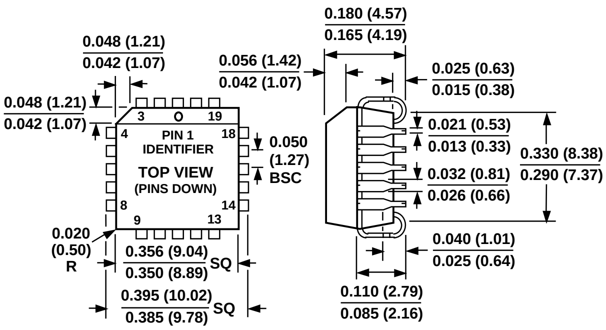


Test Circuit 12. Crosstalk

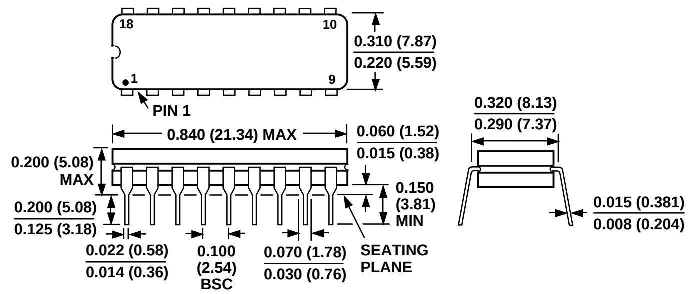
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

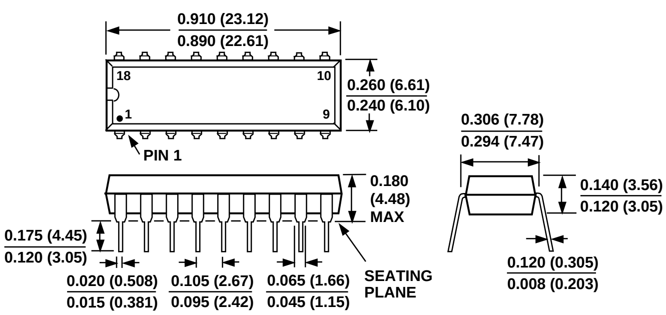
PLCC (P-20A)



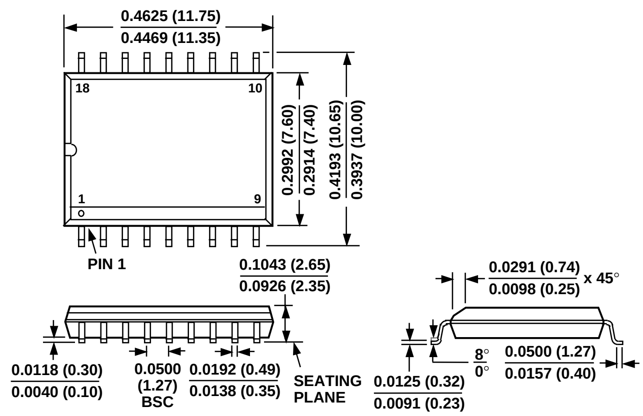
Cerdip (Q-18)



Plastic DIP (N-18)



SOIC (R-18)



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