12-Bit, 41 MSPS Monolithic ADC

AD9042

FEATURES

41 MSPS minimum sample rate
80 dB spurious-free dynamic range
595 mW power dissipation
Single 5 V supply
On-chip track-and-hold (T/H) and reference
Twos complement output format
CMOS-compatible output levels

APPLICATIONS

Cellular/PCS base stations
GPS anti jamming receivers
Communications receivers
Spectrum analyzers
Electro-optics
Medical imaging
ATE

FUNCTIONAL BLOCK DIAGRAM

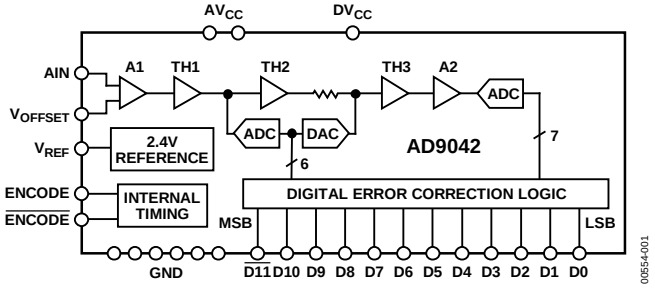

Figure 1.

GENERAL DESCRIPTION

The AD9042 is a high speed, high performance, low power, monolithic 12-bit analog-to-digital converter (ADC). All necessary functions, including track-and-hold (T/H) and reference, are included on chip to provide a complete conversion solution. The AD9042 operates from a single 5 V supply and provides CMOS-compatible digital outputs at 41 MSPS.

Designed specifically to address the needs of wideband, multi-channel receivers, the AD9042 maintains 80 dB spurious-free dynamic range (SFDR) over a bandwidth of 20 MHz. Noise performance is also exceptional; typical signal-to-noise ratio (SNR) is 68 dB.

The AD9042 is built on a high speed complementary bipolar process (XFCB) used by Analog Devices, Inc., and uses an innovative multipass architecture. Units are packaged in a 44-lead LQFP low profile quad flat package. The AD9042 industrial grade is specified from −40°C to +85°C. However, the AD9042 was designed to perform over the full military temperature range (−55°C to +125°C); consult the factory for military grade product options.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate is 41 MSPS.
2. Dynamic performance specified over entire Nyquist band; spurious signals 80 dBc typical for −1 dBFS input signals.
3. Low power dissipation: 595 mW off a single 5 V supply.
4. Reference and track-and-hold included on chip.
5. Packaged in 44-lead LQFP.

Rev. B

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SPECIFICATIONS

DC SPECIFICATIONS

AV_{CC} = DV_{CC} = 5 V; V_{REF} tied to V_{OFFSET} through 50 Ω; T_{MIN} = −40°C, T_{MAX} = +85°C.

Table 1.

Parameter[1]	Temperature	Test Level	Min	Typ	Max	Unit
RESOLUTION				12		Bits
DC ACCURACY						
No Missing Codes	Full	VI		Guaranteed		
Offset Error	Full	VI	−10	±3	+10	mV
Offset Tempco	Full	V		25		ppm/°C
Gain Error	Full	VI	−6.5	0	+6.5	% FS
Gain Tempco	Full	V		−50		ppm/°C
REFERENCE OUT (V_{REF})[2]	25°C	V		2.4		V
ANALOG INPUT (AIN)						
Input Voltage Range				V_{REF} ± 0.500		V
Input Resistance	Full	IV	200	250	300	Ω
Input Capacitance	25°C	V		5.5		pF
ENCODE INPUT[3]						
Logic Compatibility[4]				TTL/CMOS		
Logic 1 Voltage	Full	VI	2.0		5.0	V
Logic 0 Voltage	Full	VI	0		0.8	V
Logic 1 Current (V_{INH} = 5 V)	Full	VI	450	625	800	µA
Logic 0 Current (V_{INL} = 0 V)	Full	VI	−400	−300	−200	µA
Input Capacitance	25°C	V		2		pF
DIGITAL OUTPUTS						
Logic Compatibility				CMOS		
Logic 1 Voltage (I_{OH} = 10 µA)	25°C	I	3.5	4.2		V
	Full	IV	3.5			V
Logic 0 Voltage (I_{OL} = 10 µA)	25°C	I		0.75	0.80	V
	Full	IV			0.85	V
Output Coding				Twos complement		
POWER SUPPLY						
AV_{CC} Supply Voltage	Full	VI		5.0		V
AV_{CC} Current (I)	Full	V		109		mA
DV_{CC} Supply Voltage	Full	VI		5.0		V
DV_{CC} Current (I)	Full	V		10		mA
I_{CC} (Total) Supply Current	Full	VI		119	147	mA
Power Dissipation	Full	VI		595	735	mW
Power Supply Rejection Ratio (PSRR)	25°C	I	−20	±1	+20	mV/V
	Full	V		±5		mV/V

[1] C1 (Pin 10) tied to GND through a 0.01 µF capacitor.
[2] V_{REF} is normally tied to V_{OFFSET} through 50 Ω. If V_{REF} is used to provide dc offset to other circuits, it should first be buffered.
[3] ENCODE driven by single-ended source; $\overline{\text{ENCODE}}$ bypassed to ground through a 0.01 µF capacitor.
[4] ENCODE may also be driven differentially in conjunction with $\overline{\text{ENCODE}}$; see the Encoding the AD9042 section for details.

SWITCHING SPECIFICATIONS

AV_{CC} = DV_{CC} = 5 V; ENCODE and $\overline{\text{ENCODE}}$ = 41 MSPS; V_{REF} tied to V_{OFFSET} through 50 Ω; T_{MIN} = −40°C, T_{MAX} = +85°C.

Table 2.

Parameter[1]	Temperature	Test Level	Min	Typ	Max	Unit
Maximum Conversion Rate	Full	VI	41			MSPS
Minimum Conversion Rate	Full	IV			5	MSPS
Aperture Delay (t_A)	25°C	V		−250		ps
Aperture Uncertainty (Jitter)	25°C	V		0.7		ps rms
ENCODE Pulse Width High	25°C	IV	10			ns
ENCODE Pulse Width Low	25°C	IV	10			ns
Output Delay (t_{OD})	Full	IV	5	9	14	ns

[1] C1 (Pin 10) tied to GND through a 0.01 µF capacitor.

AC SPECIFICATIONS

AV_{CC} = DV_{CC} = 5 V; ENCODE and $\overline{\text{ENCODE}}$ = 41 MSPS; V_{REF} tied to V_{OFFSET} through 50 Ω; T_{MIN} = −40°C, T_{MAX} = +85°C.

Table 3.

Parameter[1, 2]	Temp	Test Level	Min	Typ	Max	Units
SNR[3]						
Analog Input at −1 dBFS						
1.2 MHz	25°C	V		68		dB
	Full	V		67.5		dB
9.6 MHz	25°C	V		67.5		dB
	Full	V		67		dB
19.5 MHz	25°C	I	64	67		dB
	Full	V		66.5		dB
SINAD[4]						
Analog Input at −1 dBFS						
1.2 MHz	25°C	V		67.5		dB
	Full	V		67		dB
9.6 MHz	25°C	V		67.5		dB
	Full	V		67		dB
19.5 MHz	25°C	I	64	67		dB
	Full	V		66.5		dB
WORST SPUR[5]						
Analog Input at −1 dBFS						
1.2 MHz	25°C	V		80		dBc
	Full	V		78		dBc
9.6 MHz	25°C	V		80		dBc
	Full	V		78		dBc
19.5 MHz	25°C	I	73	80		dBc
	Full	V		78		dBc
SMALL SIGNAL SFDR (WITH DITHER)[6]						
Analog Input						
1.2 MHz	Full	V		90		dBFS
9.6 MHz	Full	V		90		dBFS
19.5 MHz	Full	V		90		dBFS
TWO-TONE IMD REJECTION[7]						
F1, F2 @ −7 dBFS	Full	V		80		dBc
TWO-TONE SFDR (WITH DITHER)[8]	Full	V		90		dBFS
THERMAL NOISE	25°C	V		0.33		LSB rms

Parameter[1, 2]	Temp	Test Level	Min	Typ	Max	Units
DIFFERENTIAL NONLINEARITY	25°C	I	−1.0	±0.3	+1.0	LSB
(ENCODE = 20 MSPS)	Full	V		±0.4		LSB
INTEGRAL NONLINEARITY						
(ENCODE = 20 MSPS)	Full	V		±0.75		LSB
ANALOG INPUT BANDWIDTH	25°C	V		100		MHz
TRANSIENT RESPONSE	25°C	V		10		ns
OVERVOLTAGE RECOVERY TIME	25°C	V		25		ns

[1] All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially; see the Encoding the AD9042 section for details.
[2] C1 (Pin 10 on AD9042ASTZ only) tied to GND through a 0.01 µF capacitor.
[3] Analog input signal power at −1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed).
[4] Analog input signal power at −1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics.
[5] Analog input signal power at −1 dBFS; worst spur is the ratio of the signal level to worst spur, usually limited by harmonics.
[6] Analog input signal power swept from −20 dBFS to −95 dBFS; dither power = −32.5 dBm; dither circuit used on input signal (see the Overcoming Static Nonlinearities with Dither section); SFDR is the ratio of converter full scale to worst spur.
[7] Tones at −7 dBFS (f1 = 15.3 MHz, f2 = 19.5 MHz); two-tone intermodulation distortion (IMD) rejection is ratio of either tone to worst-third order intermodulation product.
[8] Both input tones swept from −20 dBFS to −95 dBFS; dither power = −32.5 dBm; dither circuit used on input signal (see the Overcoming Static Nonlinearities with Dither section); two-tone spurious-free dynamic range (SFDR) is the ratio of converter full scale to worst spur.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter[1]	Rating
AV_{CC} Voltage	0 V to 7 V
DV_{CC} Voltage	0 V to 7 V
Analog Input Voltage	0.5 V to 4.5 V
Analog Input Current	20 mA
Digital Input Voltage (ENCODE)	0 V to AV_{CC}
ENCODE, $\overline{\text{ENCODE}}$ Differential Voltage	4 V
Digital Output Current	−40 to +40 mA
Operating Temperature Range (Ambient)	−40 °C to +85°C
Maximum Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
44-Lead LQFP	55	°C/W

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at +25°C; sample tested at temperature extremes.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

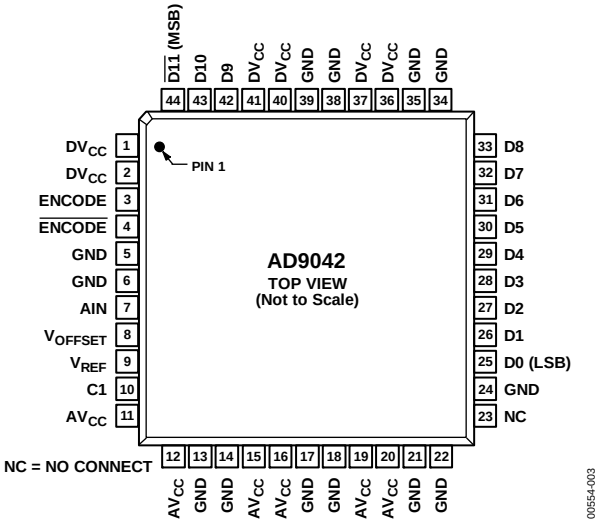


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	DV_{CC}	5 V Power Supply (Digital). Powers output stage only.
3	ENCODE	Encode Input. Data conversion initiated on rising edge.
4	$\overline{\text{ENCODE}}$	Complement of ENCODE. Drive differentially with ENCODE or bypass to ground for single-ended clock mode.
5, 6	GND	Ground.
7	AIN	Analog Input.
8	V_{OFFSET}	Voltage Offset Input. Sets mid point of analog input range. Normally tied to V_{REF} through a 50 Ω resistor.
9	V_{REF}	Internal Voltage Reference. Nominally 2.4 V; normally tied to V_{OFFSET} through a 50 Ω resistor. Bypass to ground and with 0.1 µF + 0.01 µF microwave chip capacitor.
10	C1	Internal Bias Point. Bypass to ground with a 0.01 µF capacitor.
11, 12	AV_{CC}	5 V Power Supply (Analog).
13, 14	GND	Ground.
15, 16	AV_{CC}	5 V Power Supply (Analog).
17, 18	GND	Ground.
19, 20	AV_{CC}	5 V Power Supply (Analog).
21, 22	GND	Ground.
23	NC	No Connect
24	GND	Ground.
25	D0 (LSB)	Digital Output Bit (Least Significant Bit).
26 to 33	D1 to D8	Digital Output Bits.
34, 35	GND	Ground.
36, 37	DV_{CC}	5 V Power Supply (Digital). Powers output stage only.
38, 39	GND	Ground.
40, 41	DV_{CC}	5 V Power Supply (Digital). Powers output stage only.
42, 43	D9 to D10	Digital Output Bits.
44	$\overline{\text{D11}}$ (MSB)	Digital Output Bit (Most Significant Bit). Output coded as twos complement.

TYPICAL PERFORMANCE CHARACTERISTICS

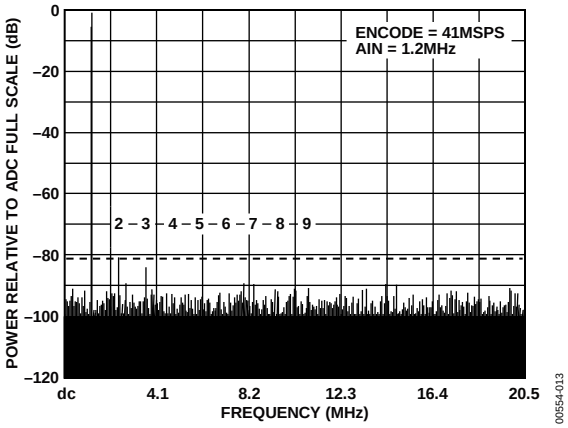


Figure 3. Single Tone at 1.2 MHz

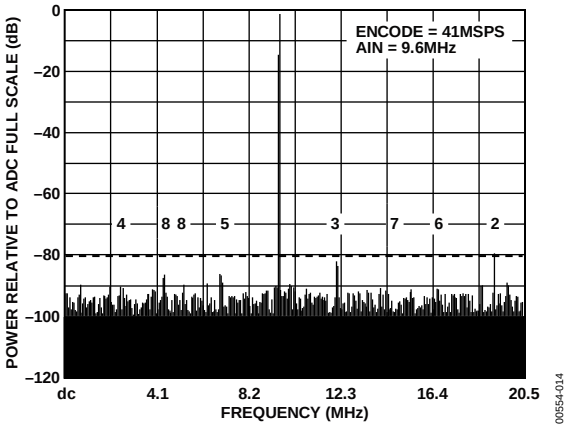


Figure 4. Single Tone at 9.6 MHz

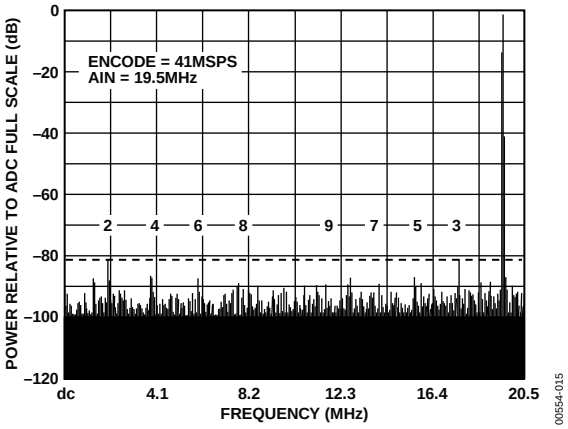


Figure 5. Single Tone at 19.5 MHz

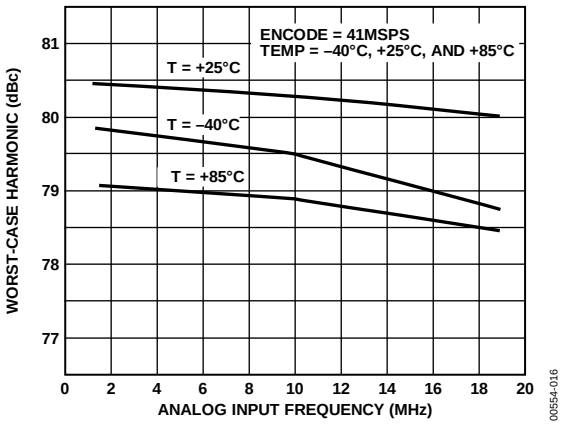


Figure 6. Worst-Case Harmonics vs. AIN

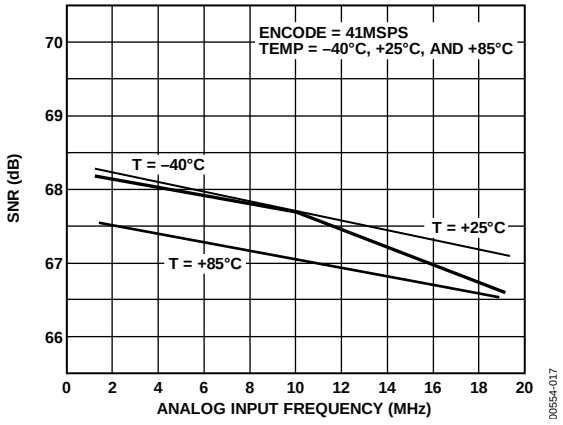


Figure 7. SNR vs. AIN

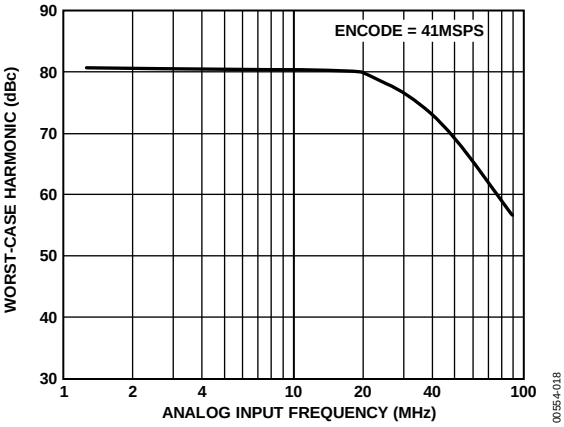


Figure 8. Worst-Case Harmonics vs. AIN

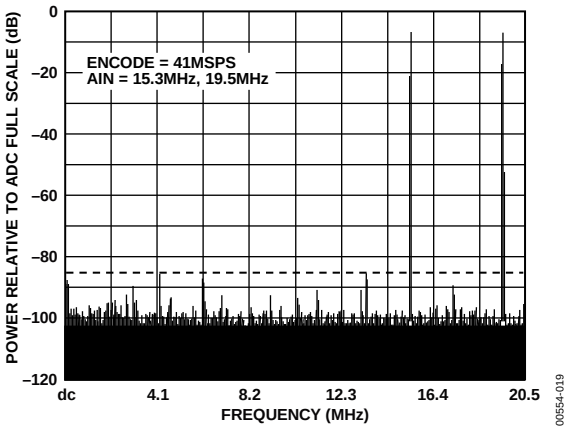


Figure 9. Two Tones at 15.3 MHz and 19.5 MHz

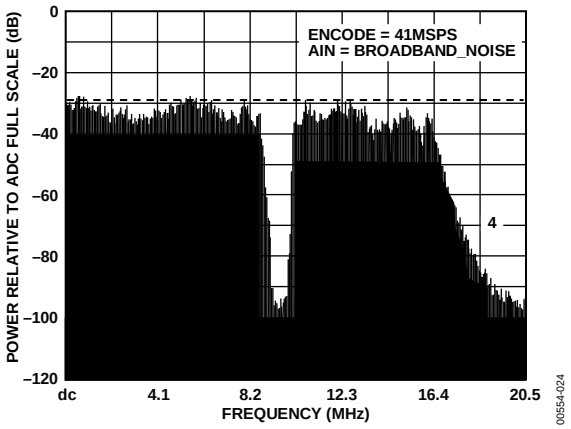


Figure 12. NPR Output Spectrum

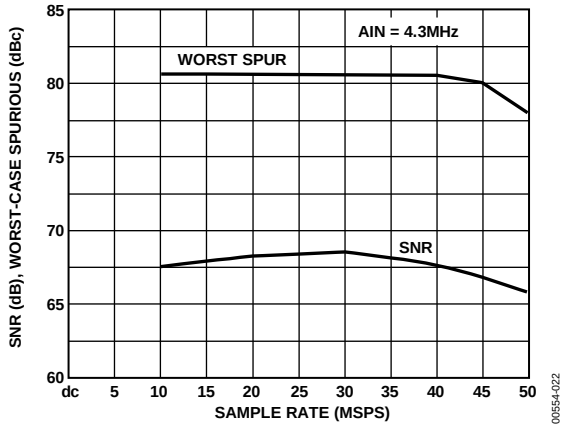


Figure 10. SNR, Worst Harmonic vs. Encode

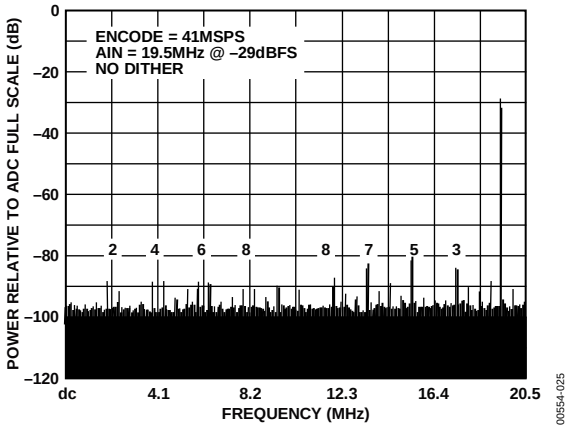


Figure 13. 4K FFT Without Dither

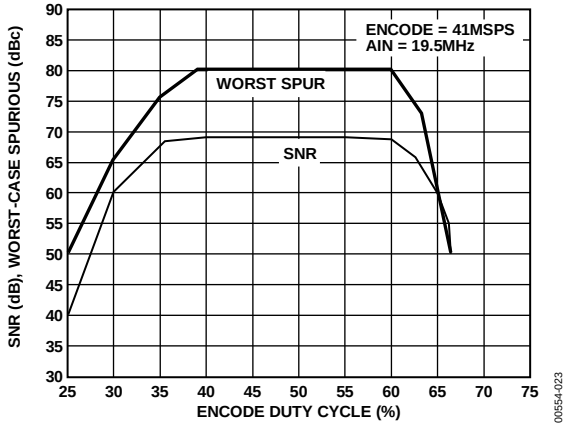


Figure 11. SNR, Worst Spurious vs. Duty Cycle

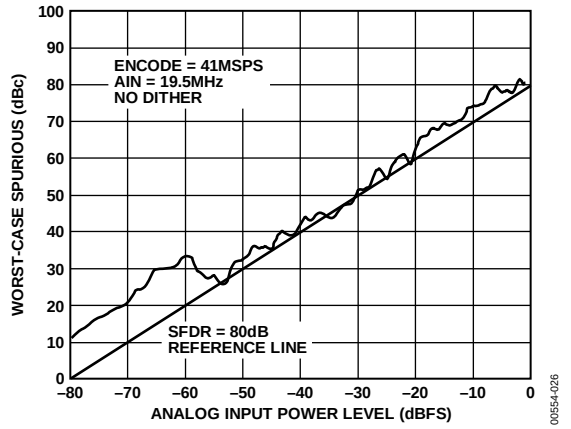


Figure 14. SFDR Without Dither

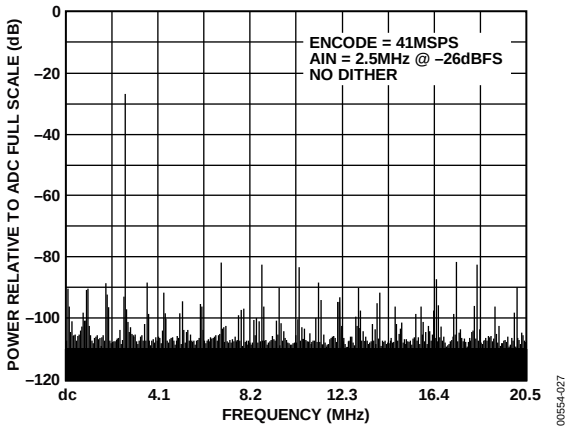


Figure 15. 128K FFT Without Dither

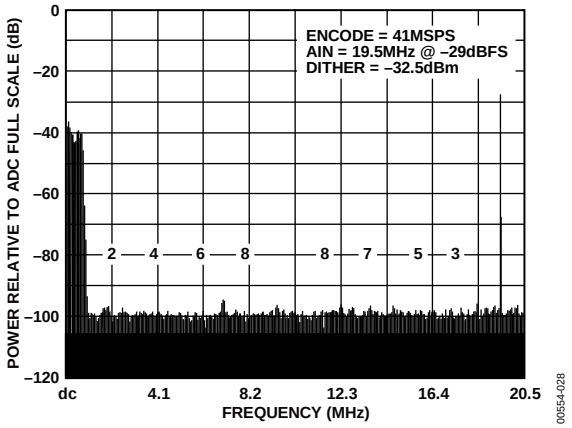


Figure 16. 4K FFT with Dither

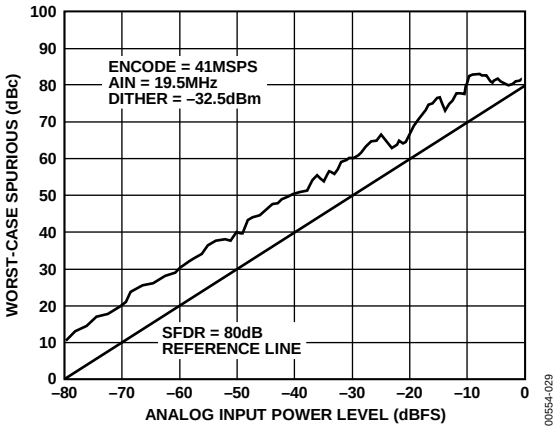


Figure 17. SFDR with Dither

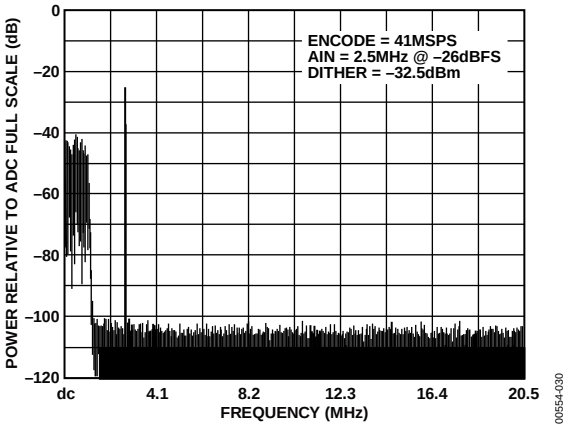


Figure 18. 128K FFT with Dither

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity (DNL)
The deviation of any code from an ideal 1 LSB step.

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the ENCODE pulse should be left in a Logic 1 state to achieve the rated performance; pulse width low is the minimum time that the ENCODE pulse should be left in low state. At a given clock rate, these specifications define an acceptable encode duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component, reported in dBc.

Integral Nonlinearity (INL)
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least square curve fit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Output Propagation Delay
The delay between the 50% point of the rising edge of the ENCODE command and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 0.02% accuracy after an analog input signal 150% of full scale is reduced to midscale.

Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD) Ratio
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio SNR (Without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in decibels (degrades as signal levels is lowered) or in decibels relative to full scale (always related back to converter full scale).

Transient Response
The time required for the converter to achieve 0.02% accuracy when a one-half full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

EQUIVALENT CIRCUITS

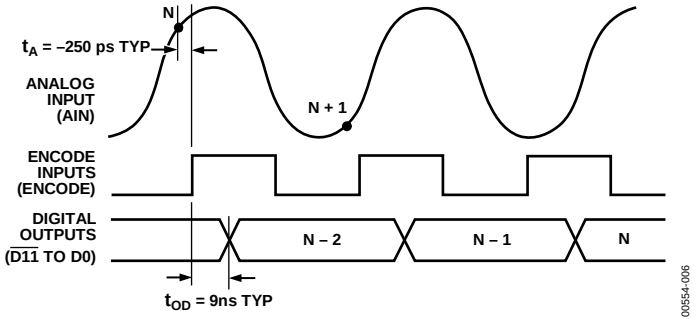


Figure 19. Timing Diagram

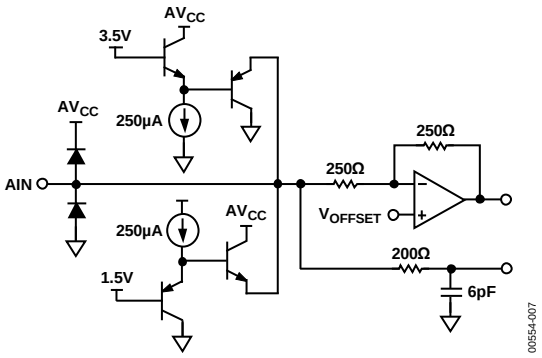


Figure 20. Analog Input Stage

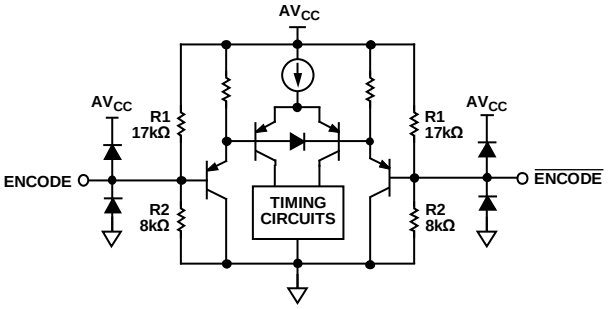


Figure 21. Encode Inputs

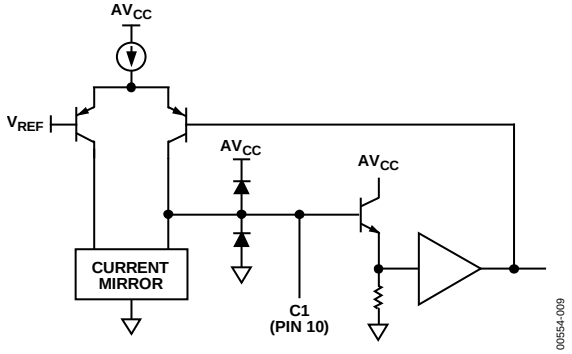


Figure 22. Compensation Pin, C1

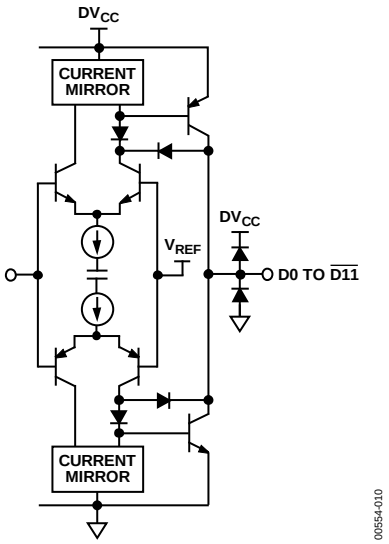


Figure 23. Digital Output Stage

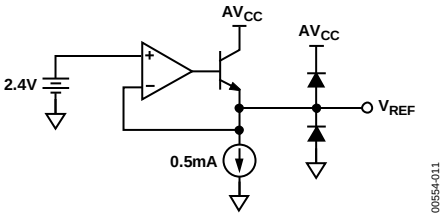


Figure 24. 2.4 V Reference

THEORY OF OPERATION

The AD9042 analog-to-digital converter (ADC) employs a two-stage subrange architecture. This design approach ensures 12-bit accuracy, without the need for laser trim, at low power.

As shown in Figure 1, the 1 V p-p single-ended analog input, centered at 2.4 V, drives a single-input to differential-output amplifier, A1. The output of A1 drives the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of the 6-bit coarse ADC. The digital output of the coarse ADC drives a 6-bit DAC; the DAC is 12 bits accurate. The output of the 6-bit DAC is subtracted from the delayed analog signal at the input to TH3 to generate a residue signal. TH2 is used as an analog pipeline to null out the digital delay of the coarse ADC.

The residue signal is passed to TH3 on a subsequent clock cycle where the signal is amplified by the residue amplifier, A2, and converted to a digital word by the 7-bit residue ADC. One bit of overlap is used to accommodate any linearity errors in the coarse ADC.

The 6-bit coarse ADC word and 7-bit residue word are added together and corrected in the digital error correction logic to generate the output word. The result is a 12-bit parallel digital word, which is CMOS-compatible, coded as twos complement.

ENCODING THE AD9042

The AD9042 is designed to interface with TTL and CMOS logic families. The source used to drive the ENCODE pin(s) must be clean and free from jitter. Sources with excessive jitter limit SNR (see Equation 1 in the Noise Floor and SNR section).

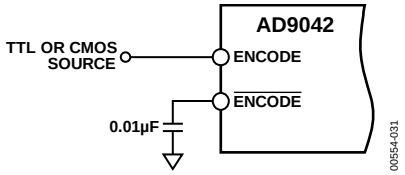


Figure 25. Single-Ended TTL/CMOS Encode

The AD9042 encode inputs are connected to a differential input stage (see Figure 21 in the Equivalent Circuits section). With no input connected to either the ENCODE or input, the voltage dividers bias the inputs to 1.6 V. For TTL or CMOS usage, the encode source should be connected to ENCODE. $\overline{\text{ENCODE}}$ should be decoupled using a low inductance or microwave chip capacitor to ground. Devices such as the AVX 05085C103MA15, a 0.01 µF capacitor, work well.

If a logic threshold other than the nominal 1.6 V is required, the following equations show how to use an external resistor, Rx, to raise or lower the trip point (see Figure 21; R1 = 17 kΩ, R2 = 8 kΩ).

To lower the logic threshold, use the following equation:

$$V_1 = \frac{5R_2R_X}{R_1R_2 + R_1R_X + R_2R_X}$$

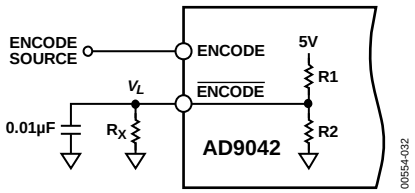


Figure 26. Lower Logic Threshold for Encode

To raise the logic threshold, use the following equation:

$$V_1 = \frac{5R_2}{R_2 + \frac{R_1R_X}{R_1 + R_X}}$$

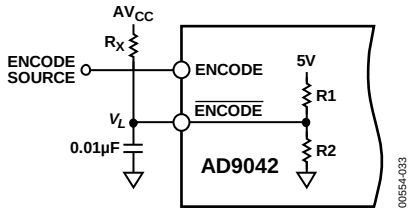


Figure 27. Raise Logic Threshold for Encode

Although the single-ended encode works well for many applications, driving the encode differentially provides increased performance. Depending on circuit layout and system noise, a 1 dB to 3 dB improvement in SNR can be realized. It is not recommended that differential TTL logic be used, however, because most TTL families that support complementary outputs are not delay or slew rate matched. Instead, it is recommended that the encode signal be ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins.

The simplest option is shown in Figure 28. The low jitter TTL signal is coupled with a limiting resistor, typically 100 Ω, to the primary side of an RF transformer (these transformers are inexpensive and readily available; part number in Figure 28 is from Mini-Circuits). The secondary side is connected to the ENCODE and $\overline{\text{ENCODE}}$ pins of the converter. Because both encode inputs are self-biased, no additional components are required.

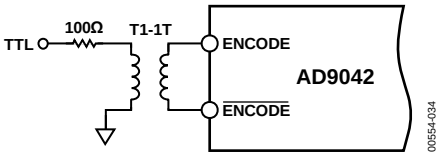


Figure 28. TTL Source Differential Encode

If no TTL source is available, a clean sine wave can be substituted. In the case of the sine source, the matching network is shown in Figure 29. Because the matching transformer specified is a 1:1 impedance ratio, R, the load resistor should be selected to match the source impedance. The input impedance of the AD9042 is negligible in most cases.

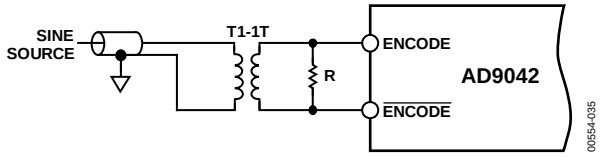


Figure 29. Sine Source Differential Encode

If a low jitter ECL clock is available, another option is to ac-couple a differential ECL signal to the encode input pins as shown in Figure 30. The capacitors shown here should be chip capacitors but do not need to be of the low inductance variety.

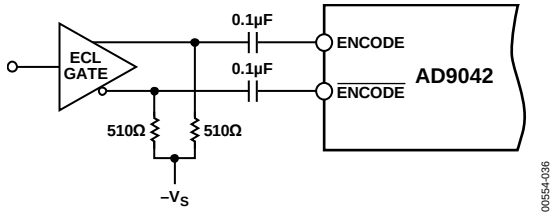


Figure 30. Differential ECL for Encode

As a final alternative, the ECL gate can be replaced by an ECL comparator. The input to the comparator could then be a logic signal or a sine signal.

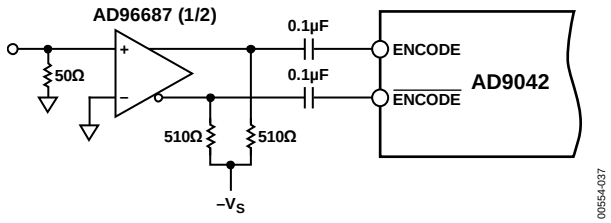


Figure 31. ECL Comparator for Encode

Care should be taken not to overdrive the encode input pins when ac-coupled. Although the input circuitry is electrically protected from overvoltage or undervoltage conditions, improper circuit operations may result from overdriving the encode input pins.

DRIVING THE ANALOG INPUT

Because the AD9042 operates from a single 5 V supply, the analog input range is offset from ground by 2.4 V. The analog input, AIN, is an operational amplifier configured in an inverting mode (see Figure 32). V_{OFFSET} is the noninverting input, which is normally tied through a 50 Ω resistor to V_{REF} (see Figure 32). Because the operational amplifier forces its inputs to the same voltage, the inverting input is also at 2.4 V. Therefore, the analog input has a Thevenin equivalent of 250 Ω in series with a 2.4 V source. It is strongly recommended that the internal voltage reference of the AD9042 be used for the amplifier offset; this reference is designed to track internal circuit shifts over temperature.

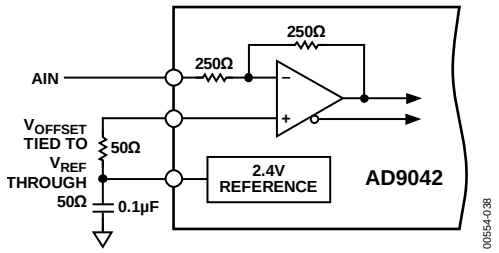


Figure 32. Analog Input Offset by 2.4 V Reference

Although the AD9042 can be used in many applications, it was specifically designed for communications systems that must digitize wide signal bandwidths. As such, the analog input was designed to be ac-coupled. Because most communications products do not downconvert to dc, this should not pose a problem. One example of a typical analog input circuit is shown in Figure 33. In this application, the analog input is coupled with a high quality chip capacitor, the value of which can be chosen to provide a low frequency cutoff that is consistent with the signal being sampled; in most cases, a 0.1 µF chip capacitor works well.

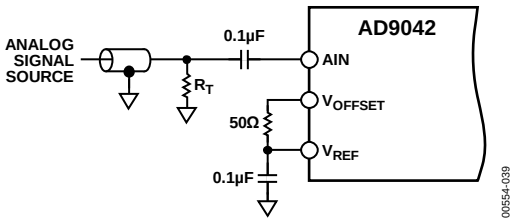


Figure 33. AC-Coupled Analog Input Signal

Another option for ac coupling is a transformer. The impedance ratio and frequency characteristics of the transformer are determined by examining the characteristics of the input signal source (transformer primary connection), and the AD9042 input characteristics (transformer secondary connection). Given the transformer turns ratio, R_T should be chosen to satisfy the termination requirements of the source. A blocking capacitor is required to prevent AD9042 dc bias currents from flowing through the transformer.

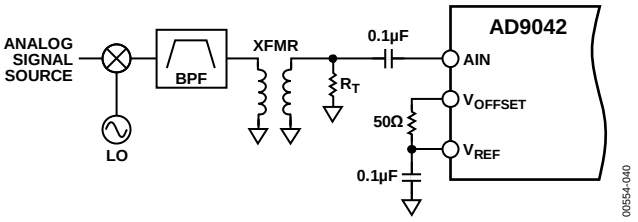


Figure 34. Transformer-Coupled Analog Input Signal

When calculating the proper termination resistor, note that the external load resistor is in parallel with the AD9042 analog input resistance, 250 Ω. The external resistor value can be calculated from the following equation:

$$R_T = \frac{1}{\frac{1}{Z} - \frac{1}{250}}$$

where Z is desired impedance.

A dc-coupled input configuration (shown in Figure 35) is limited by the drive amplifier performance. The on-chip reference of the AD9042 is buffered using the OP279 dual, rail-to-rail operational amplifier. The resulting voltage is combined with the analog source using an AD9631. Pending improvements in drive amplifiers, this dc-coupled approach is limited to ~75 dB to 80 dB of dynamic performance depending on which drive amplifier is used. The AD9631 and OP279 run off ±5 V.

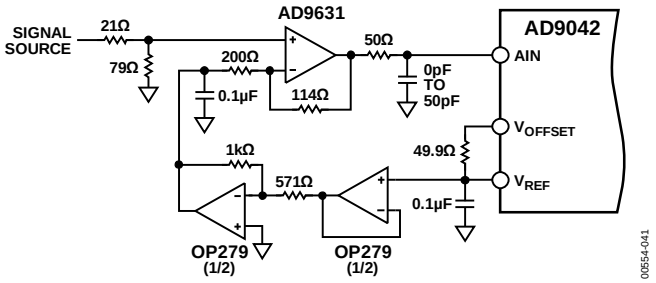


Figure 35. DC-Coupled Analog Input Circuit

POWER SUPPLIES

Care should be taken when selecting a power source. Linear supplies are strongly recommended because switching supplies tend to have radiated components that may be received by the AD9042. Each of the power supply pins should be decoupled as close to the package as possible using 0.1 µF chip capacitors.

The AD9042 has separate digital and analog 5 V pins. The AV_{CC} pins are the analog supply pins, and the DV_{CC} pins are the digital supply pins. Although analog and digital supplies may be tied together, best performance is achieved when the supplies are separate. This is because the fast digital output swings can couple switching noise back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 V.

OUTPUT LOADING

Care must be taken when designing the data receivers for the AD9042. It is recommended that the digital outputs drive a series resistor of 499 Ω followed by a CMOS gate such as the 74AC574. To minimize capacitive loading, there should be only one gate on each output pin. The digital outputs of the AD9042 have a unique constant slew rate output stage. The output slew rate is about 1 V/ns independent of output loading. A typical CMOS gate combined with PCB trace and through hole has a load of approximately 10 pF. Therefore, as each bit switches, 10 mA of dynamic current per bit flows in or out of the device. A full-scale transition can cause up to 120 mA (12 bits × 10 mA/bit) of current to flow through the digital output stage. The series resistor minimizes the output currents that can flow in the output stage. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided because they can appreciably add to the dynamic switching currents of the AD9042.

$$\left(10\ pF \times \frac{1\ V}{1\ ns}\right)$$

LAYOUT INFORMATION

The pinout of the AD9042 facilitates ease of use and the implementation of high frequency/high resolution design practices. All of the digital outputs are on one side of the package, and all of the inputs are on the other sides of the package. It is highly recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. Depending on the configuration used for the encode and analog inputs, one or more capacitors are required on those input pins. The capacitors used on the $\overline{\text{ENCODE}}$ and V_{REF} pins must be low inductance chip capacitors as noted previously.

Although a multilayer board is recommended, it is not required to achieve good results. Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connected directly to the receiving gate (broken only by the insertion of the series resistor). Logic fanout for each bit should be one CMOS gate.

DIGITAL WIDEBAND RECEIVERS

INTRODUCTION

Several key technologies are now being introduced that may forever alter the vision of radio. Figure 36 shows the typical dual conversion superheterodyne receiver. The signal picked up by the antenna is mixed down to an intermediate frequency (IF) using a mixer with a variable local oscillator (LO); the variable LO is used to tune in the desired signal. This first IF is mixed down to a second IF using another mixer stage and a fixed LO. Demodulation takes place at the second or third IF using either analog or digital techniques.

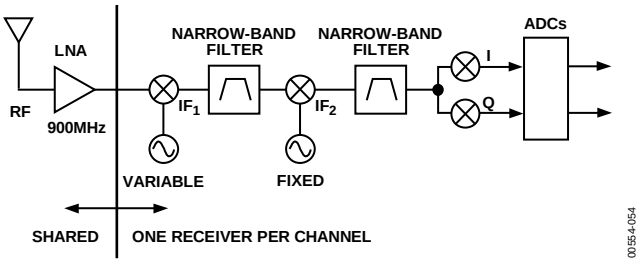


Figure 36. Narrow-Band Digital Receiver Architecture

If demodulation takes place in the analog domain, then traditional discriminators, envelope detectors, phase-locked loops, or other synchronous detectors are generally used to strip the modulation from the selected carrier.

However, as general-purpose DSP chips such as the ADSP-2181 become more popular, they can be used in many baseband sampled application such as the one shown in Figure 36. As shown in the figure, prior to ADC conversion, the signal must be mixed down and filtered, and the I and Q components must be separated. These functions are realized through DSP techniques; however, several key technology breakthroughs are required: high dynamic range ADCs, such as the AD9042, new DSPs (highly programmable with fast onboard memory), digital tuner and filter (with programmable frequency and BW), and wideband mixers (high dynamic range with >12.5 MHz BW).

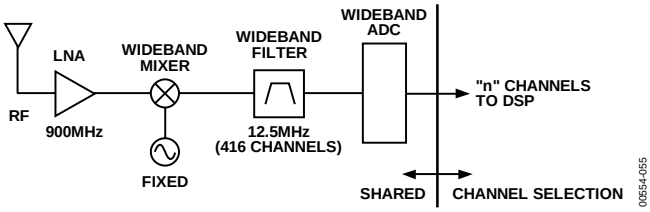


Figure 37. Wideband Digital Receiver Architecture

Figure 37 shows such a wideband system. This design shows that the front-end variable local oscillator has been replaced with a fixed oscillator (for single-band radios), and the back end has been replaced with a wide dynamic range ADC, digital tuner, and DSP. This technique offers many benefits.

First, many passive discrete components that formed the tuning and filtering functions have been eliminated. These passive components often require adjusting and special handling during assembly and final system alignment. Digital components require no such adjustments; tuner and filter characteristics are always exactly the same. Moreover, the tuning and filtering characteristics can be changed through software. Because software is used for demodulation, different routines may be used to demodulate different standards such as AM, FM, GMSK, or any other desired standard. In addition, as new standards arise or new software revisions are generated, they may be field installed with standard software update channels. A radio that performs demodulation in software as opposed to hardware is often referred to as a soft radio because it can be changed or modified simply through code revision.

System Description

In the wideband digital radio (see Figure 37), the first down-conversion functions in much the same way as a block converter does. An entire band is shifted in frequency to the desired intermediate frequency. In the case of cellular base station receivers, 5 MHz to 20 MHz of bandwidth are downconverted simultaneously to an IF frequency suitable for digitizing with a wideband ADC. Once digitized, the broadband digital data stream contains all of the in-band signals. The remainder of the radio is constructed digitally using special-purpose and general-purpose programmable DSP to perform filtering, demodulation, and signal conditioning, not unlike the analog counterparts.

In the narrow-band receiver (see Figure 36), the signal to be received must be tuned. This is accomplished by using a variable local oscillator at the first mix-down stage. The first IF then uses a narrow-band filter to reject out-of-band signals and condition the selected carrier for signal demodulation.

In the digital wideband receiver (see Figure 37), the variable local oscillator has been replaced with a fixed oscillator, so tuning must be accomplished in another manner. Tuning is performed digitally using a digital downconversion and a filter chip frequently called a channelizer. The term, channelizer, is used because the purpose of these chips is to select one channel out of the many within the broadband of spectrum actually present in the digital data stream of the ADC.

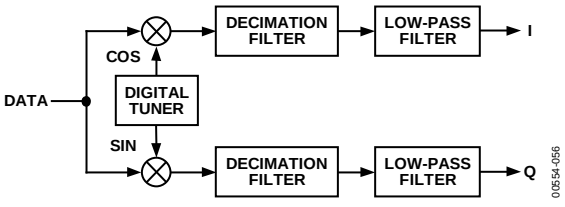


Figure 38. Digital Channelizer

Figure 38 shows the block diagram of a typical channelizer. Channelizers consist of a complex NCO (numerically controlled oscillator), dual multiplier (mixer), and matched digital filters. These are the same functions that would be required in an analog receiver but implemented in digital form. The digital output from the channelizer is the desired carrier, frequently in I and Q format; all other signals are filtered and removed based on the filtering characteristics desired. Because the channelizer output consists of one selected RF channel, one tuner chip is required for each frequency received, although only one wideband RF receiver is needed for the entire band. Data from the channelizer can then be processed using a digital signal processor such as the ADSP-2181 or the SHARC ADSP-21062 processor. This data may then be processed through software to demodulate the information from the carrier.

Figure 39 shows a typical wideband receiver subsystem based around the AD9042. This strip consists of a wideband IF filter, amplifier, ADC, latches, channelizer, and interface to a digital signal processor. This design shows a typical clocking scheme used in many receiver designs. All timing within the system is referenced back to a single clock. Although this is not necessary, it facilitates PLL design, ease of manufacturing, system test, and calibration. Keeping in mind that the overall performance goal is to maintain the best possible dynamic range, many choices must be considered.

One of the biggest challenges is selecting the amplifier used to drive the AD9042. Because this is a communications application, the key specification for this amplifier is spurious-free dynamic range (SFDR). An amplifier should be selected that can provide SFDR performance better than 80 dB into 250 Ω. One such amplifier is the AD9631. These low spurious levels are necessary because harmonics due to the drive amplifier and ADC can distort the desired signals of interest.

Two other key considerations for the digital wideband receiver are converter sample rate and IF frequency range. Because performance of the AD9042 converter is nearly independent of both sample rate and analog input frequency (see Figure 6, Figure 7, and Figure 10), the designer has greater flexibility in the selection of these parameters. Also, because the AD9042 is a bipolar device, power dissipation is not a function of sample rate. Thus, there is no penalty paid in power by operating at faster sample rates. By carefully selecting input frequency range and sample rate, the drive amplifier and ADC harmonics can actually be placed out-of-band. Thus, other components such as filters and IF amplifiers may actually end up being the limiting factor on dynamic range.

For example, if the system has second and third harmonics that are unacceptably high, the careful selection of the encode rate and signal bandwidth can place these second and third harmonics out-of-band. For the case of an encode rate equal to 40.96 MSPS and a signal bandwidth of 5.12 MHz, placing the fundamental at 5.12 MHz places the second and third harmonics out-of-band as shown in Table 7.

Table 7. Example Frequency Plan

Parameter	Value
Encode Rate	40.96 MSPS
Fundamental	5.12 MHz to 10.24 MHz
Second Harmonic	10.24 MHz to 20.48 MHz
Third Harmonic	15.36 MHz to 10.24 MHz

Another option is found through band-pass sampling. If the analog input signal range is from dc to FS/2, then the amplifier and filter combination must perform to the specification required. However, if the signal is placed in the third Nyquist zone (FS to 3 FS/2), the amplifier is no longer required to meet the harmonic performance required by the system specifications because all harmonics fall outside the pass-band filter. For example, the pass-band filter ranges from f_S to 3 FS/2. The second harmonic would span from 2 FS to 3 FS, well outside the range of the pass-band filter. The burden then is placed on the filter design, provided that the ADC meets the basic specifications at the frequency of interest. In many applications, this is a worthwhile trade-off because many complex filters can easily be realized using SAW and LCR techniques alike at these relatively high IF frequencies. Although the harmonic performance of the drive amplifier is relaxed by this technique, intermodulation performance cannot be sacrificed because intermods must be assumed to fall in-band for both amplifiers and converters.

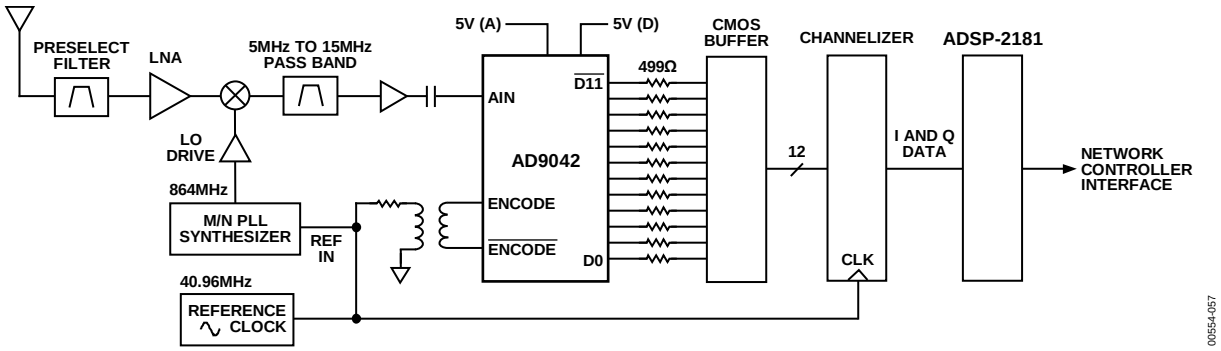


Figure 39. Simplified 5 MHz Wideband "A" Carrier Receiver

NOISE FLOOR AND SNR

Oversampling is the act of sampling at a rate that is greater than twice the bandwidth of the signal desired. Oversampling has nothing to do with the actual frequency of the sampled signal. It is the bandwidth of the signal that is key. Band-pass or IF sampling refers to sampling a frequency that is higher than Nyquist and often provides additional benefits such as downconversion using the ADC and track-and-hold as a mixer. Oversampling leads to processing gains because the faster the signal is digitized, the wider the distribution of noise. Because the integrated noise must remain constant, the actual noise floor is lowered by 3 dB each time the sample rate is doubled. The effective noise density for an ADC may be calculated by the following equation:

$$V_{NOISE\,rms} / \sqrt{Hz} = \frac{10^{-SNR/20}}{\sqrt{4\,FS}}$$

For a typical SNR of 68 dB and a sample rate of 40.96 MSPS, this is equivalent to 31 nV/√Hz . This equation shows the relationship between the SNR of the converter and the sample rate FS. This equation can be used todetermine overall receiver noise.

The SNR for an ADC can be predicted. When normalized to ADC codes, the following equation accurately predicts the SNR based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

$$SNR = -20\log\left[\left(2\pi F_{ANALOG} \times t_{J\,rms}\right)^2 + \left(\frac{1+\varepsilon}{2^{12}}\right)^2 + \left(\frac{V_{NOISE\,rms}}{2^{12}}\right)^2\right]^{1/2}$$

where

F_{ANALOG} is analog input frequency.
$t_{J\,rms}$ is rms jitter of the encode (rms sum of encode source and internal encode circuitry).
ε is average DNL of the ADC.
$V_{NOISE\,rms}$ is V rms thermal noise referred to the analog input of the ADC.

PROCESSING GAIN

Processing gain is the improvement in SNR gained through DSP processes. Most of this processing gain is accomplished using the channelizer chips. These special-purpose DSP chips not only provide channel selection and filtering but also provide a data rate reduction. Few, if any, general-purpose DSPs can accept and process data at 40.96 MSPS. The required rate reduction is accomplished through a process called decimation. The term decimation rate is used to indicate the ratio of input data rate to output data rate. For example, if the input data rate is 40.96 MSPS and the output data rate is 30 kSPS, then the decimation rate is 1365.

Large processing gains may be achieved in the decimation and filtering process. The purpose of the channelizer, beyond tuning, is to provide the narrow-band filtering and selectivity that traditionally has been provided by the ceramic or crystal filters of a narrow-band receiver. This narrow-band filtering is the source of the processing gain associated with a wideband receiver and is simply the ratio of the pass-band to whole band expressed in dBc. For example, if a 30 kHz AMPS signal is digitized with an AD9042 sampling at 40.96 MSPS, the ratio is 0.030 MHz/20.48 MHz. Expressed in log form, the processing gain is −10 × log (0.030 MHz/20.48 MHz) or 28.3 dB.

Additional filtering and noise reduction techniques can be achieved through DSP techniques; many applications obtain additional process gains through proprietary noise reduction algorithms.

OVERCOMING STATIC NONLINEARITIES WITH DITHER

Typically, high resolution data converters use multistage techniques to achieve high bit resolution without large comparator arrays that would be required if traditional flash ADC techniques were used. The multistage converter typically provides better wafer yields, meaning lower cost and much lower power. However, because it is a multistage device, certain portions of the circuit are used repetitively as the analog input sweeps from one end of the converter range to the other. Although the worst DNL error may be less than 1 LSB, the repetitive nature of the transfer function can create havoc with low level dynamic signals. Spurious signals for a full-scale input may be −88 dBc; however, at 29 dB below full scale, these repetitive DNL errors can cause SFDR to fall to 80 dBc as shown in Figure 13.

A common technique for randomizing and reducing the effects of repetitive static linearity is through the use of dither. The purpose of dither is to force the repetitive nature of static linearity to appear as if it were random. Then, the average linearity over the range of dither dominates the SFDR performance. In the AD9042, the repetitive cycle is every 15.625 mV p-p.

To ensure adequate randomization, 5.3 mV rms is required; this equates to a total dither power of −32.5 dBm. This randomizes the DNL errors over the complete range of the residue converter. Although lower levels of dither such as that from previous analog stages reduces some of the linearity errors, the full effect is gained only with this larger dither. Increasing dither even more can be used to reduce some of the global INL errors. However, signals much larger than the microvolts proposed in this data sheet begin to reduce the usable dynamic range of the converter.

Even with the 5.3 mV rms of noise suggested, SNR is limited to 36 dB if injected as broadband noise. To avoid this problem, noise can be injected as an out-of-band signal. Typically, this may be around dc but may just as well be at FS/2 or at some other frequency not used by the receiver. The bandwidth of the noise is several hundred kilohertz. By band-limiting and controlling its location in frequency, large levels of dither can be introduced into the receiver without seriously disrupting receiver performance. The result can be a marked improvement in the SFDR of the data converter.

performance. The result can be a marked improvement in the SFDR of the data converter.

Figure 16 shows the same converter shown in Figure 13 but with this injection of dither (see Figure 13). SFDR is now 94 dBFS. Figure 14 and Figure 17 show an SFDR sweep before and after adding dither.

To fully appreciate the improvement that dither can have on performance, Figure 15 and Figure 18 show similar dither plots, one using and one not using dither. Increasing to 128k sample points lowers the noise floor of the FFT; this simply makes it easier to see the dramatic reduction in spurious levels resulting from dither.

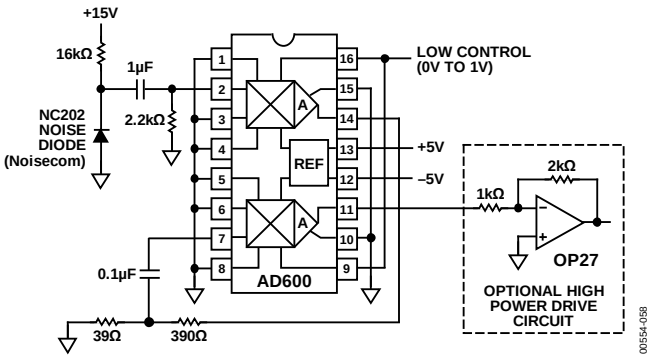


Figure 40. Noise Source (Dither Generator)

The simplest method for generating dither is through the use of a noise diode (see Figure 40). In this circuit, the noise diode, NC202, generates the reference noise that is gained up and driven by the AD600 and OP27 amplifier chain. The level of noise can be controlled by either presetting the control voltage when the system is set up or by using a digital-to-analog converter (DAC) to adjust the noise level based on input signal conditions. Once generated, the signal must be introduced to the receiver strip. The easiest method is to inject the signal into the drive chain after the last downconversion, as shown in Figure 41.

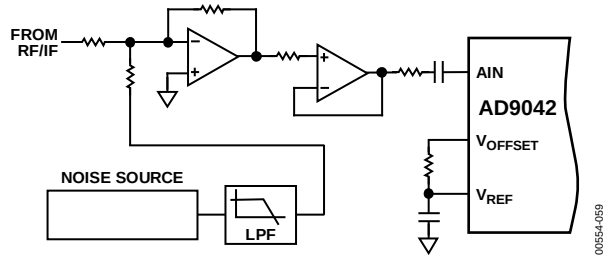


Figure 41. Using the AD9042 with Dither

RECEIVER EXAMPLE

To determine how the ADC performance relates to overall receiver sensitivity, the simple receiver in Figure 42 can be examined. This example assumes that the overall downconversion process can be grouped into one set of specifications, instead of individually examining all components within the system and summing them together. Although a more detailed analysis should be employed in a real design, this model provides a good approximation.

In examining a wideband digital receiver, several considerations must be applied. Although other specifications are important, receiver sensitivity determines the absolute limits of a radio, excluding the effects of other outside influences. Assuming that receiver sensitivity is limited by noise and not by adjacent signal strength, several sources of noise can be identified and their overall contribution to receiver sensitivity calculated.

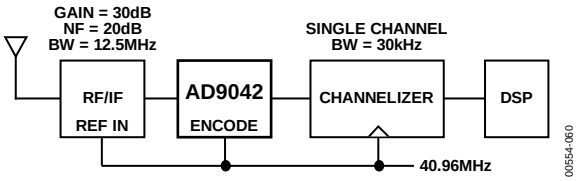


Figure 42. Receiver Analysis

The first noise calculation to make is based on the signal bandwidth at the antenna. In a typical broadband cellular receiver, the IF bandwidth is 12.5 MHz. Given that the power of noise in a given bandwidth is defined by $P_n = kTB$, where B is bandwidth, $k = 1.38 \times 10^{-23}$ is Boltzmann's constant, and $T =$ 300k is absolute temperature, this gives an input noise power of 5.18×10^{-14} watts or −102.86 dBm. If the receiver front end has a gain of 30 dB and a noise figure of 20 dB, then the total noise presented to the ADC input becomes −52.86 dBm (−102.86 + 30 + 20) or 0.51 mV rms. Comparing receiver noise to the dither required for good SFDR, note that in this example, the receiver supplies about 10% of the dither required for good SFDR.

Based on a typical ADC SNR specification of 68 dB, the equivalent internal converter noise is 0.140 mV rms. Therefore, total broadband noise is 0.529 mV rms. Before processing gain, this is an equivalent SNR (with respect to full scale) of 56.5 dB. Assuming a 30 kHz AMPS signal and a sample rate of 40.96 MSPS, the SNR, through processing gain, is increased by 28.3 dB to 84.8 dB. However, if eight strong and equal signals are present in the ADC bandwidth, each must be placed 18 dB below full scale to prevent ADC overdrive. In addition, 3 dB to 15 dB should be used for ADC headroom should another signal come in-band unexpectedly. For this example, 12 dB of headroom can be allocated. Therefore, 30 dB of range is given away and the carrier-to-noise ratio (C/N) is reduced to 54.8 dB (C/N is the ratio of signal to in-band noise).

Assuming that the C/N ratio must be 6 dB or better for accurate demodulation, one of the eight signals can be reduced by 48.8 dB before demodulation becomes unreliable. At this point, the input signal power would be 40.6 µV rms on the ADC input or −74.8 dBm. Referenced to the antenna, this is −104.8 dBm.

To improve sensitivity, several things can be done. First, the noise figure of the receiver can be reduced. Because front-end noise dominates the 0.529 mV rms, each dB reduction in noise figure translates to an additional dBc of sensitivity. Second, providing broadband AGC can improve sensitivity by the range of the AGC. However, the AGC only provides useful improvements if all in-band signals are kept to an absolute minimal power level so that AGC can be kept near the maximum gain.

This noise-limited example does not adequately demonstrate the true limitations in a wideband receiver. Other limitations such as SFDR are more restrictive than SNR and noise. Assume that the ADC has an SFDR specification of −80 dBFS or −76 dBm (full scale = 4 dBm). Also assume that a tolerable carrier-to-interferer (C/I) (different from C/N) ratio is 18 dB (C/I is the ratio of signal to in-band interfere). This means that the minimum signal level is −62 dBFS (−80 plus 18) or −58 dBm. At the antenna, this is −88 dBm. Therefore, as can be seen, SFDR (single or multitone) would limit receiver performance in this example. However, SFDR can be greatly improved through the use of dither (see Figure 15 and Figure 18). In many cases, the addition of the out-of-band dither can improve receiver sensitivity nearly to that limited by thermal noise.

Multitone Performance

Figure 43 shows the AD9042 in a worst-case scenario of four strong tones spaced fairly close together. In this plot, no dither was used, and the converter still maintains 85 dBFS of spurious-free range. As noted in the Overcoming Static Nonlinearities with Dither section, a modest amount of dither introduced out-of-band can be used to lower the nonlinear components.

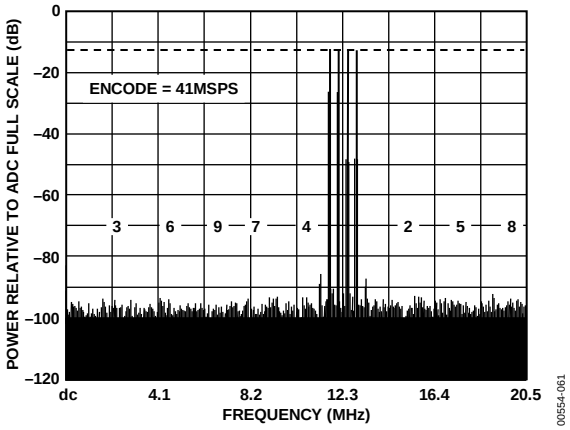


Figure 43. Multitone Performance

IF SAMPLING, USING THE AD9042 AS A MIX-DOWN STAGE

Because the performance of the AD9042 extends beyond the baseband region into the second and third Nyquist zone, the converter may find many uses as a mix-down converter in both narrow-band and wideband applications. Many common IF frequencies exist in this range of frequencies. If the ADC is used to sample these signals, they are aliased down to baseband during the sampling process in much the same manner that a mixer downconverts a signal. For signals in various Nyquist zones, the following equations may be used to determine the final frequency after aliasing.

$$f_{1NYQUISTS} = f_{SAMPLE} - f_{SIGNAL}$$
$$f_{2NYQUISTS} = abs\ (f_{SAMPLE} - f_{SIGNAL})$$
$$f_{3NYQUISTS} = 2 \times (f_{SAMPLE} - f_{SIGNAL})$$
$$f_{4NYQUISTS} = abs\ (2 \times f_{SAMPLE} - f_{SIGNAL})$$

Using the converter to alias down these narrow-band or wideband signals has many potential benefits. First and foremost is the elimination of a complete mixer stage, along with amplifiers, filters, and other devices, reducing cost and power dissipation.

One common example is the digitization of a 21.4 MHz IF using a 10 MSPS sample clock. Using the equation for the fifth Nyquist zone, the resultant frequency after sampling is 1.4 MHz. Figure 44 shows performance under these conditions. Even under these conditions, the AD9042 typically maintains better than 80 dB SFDR.

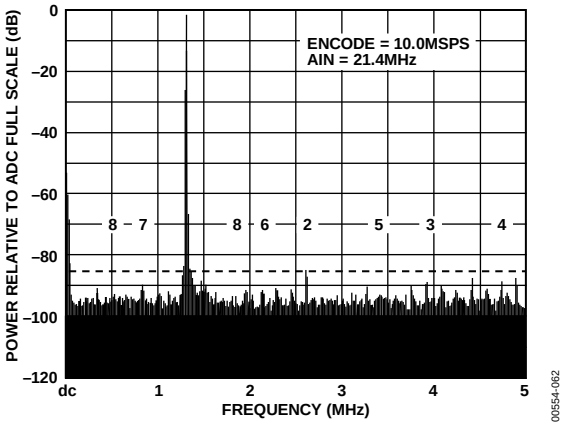


Figure 44. IF Sampling at 21.4 MHz Input

RECEIVE CHAIN FOR DIGITAL AND ANALOG BEAM FORMING MEDICAL ULTRASOUND USING THE AD9042

The AD9042 is an excellent digitizer for digital and analog beam-forming medical ultrasound systems. The price/performance ratio of the AD9042 allows ultrasound designers the luxury of using state-of-the-art ADCs without jeopardizing their cost budgets. ADC performance is critical for image quality. The high dynamic range and excellent noise performance of the AD9042 enable higher image quality medical ultrasound systems.

Figure 45 shows the AD9042 used in one channel of the receive chain of a medical ultrasound system. The AD604 receives its input directly from the transducer or from an external preamp connected to the transducer. The AD604 contains two separate stages. The first stage is a preamp with a fixed gain (14 dB to 20 dB) selected by a fixed resistor. The second stage is a variable gain amplifier with the gain set by the AD7226 DAC. The gain is increased over time to compensate for the attenuation of signal level in the body.

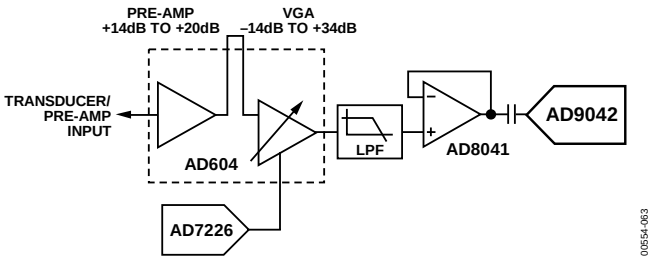
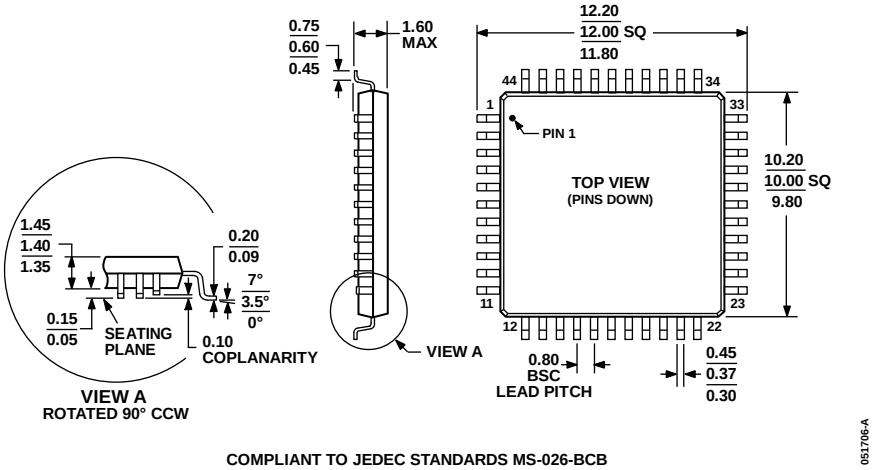


Figure 45. Using the AD9042 in Ultrasound Applications

Following the AD604, a low-pass filter is used to minimize the amount of noise presented to the ADC. The AD8041 is used to buffer the filter from the AD9042 input. This function may not be required depending on the filter configuration and PCB partitioning. The digital outputs of the AD9042 are then presented to the digital system for processing.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BCB

Figure 46. 44-Lead Low Profile Quad Flat Package [LQFP]
(ST-44-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9042ASTZ[1]	−40°C to +85°C	44-Lead Low Profile Quad Flat Package [LQFP]	ST-44-1

[1]Z = RoHS Compliant Part.

NOTES

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