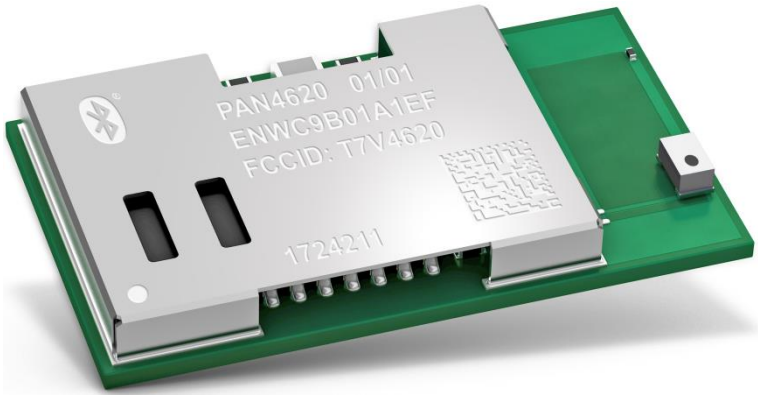
Panasonic

PAN4620

IEEE® 802.15.4 and Bluetooth® Low Energy Module

Product Specification

Rev. 0.1



Wireless Modules

Overview

The PAN4620 is Panasonic's Internet of Things dual mode module comprising NXP®'s Kinetis MKW41Z512CAT4 SoC - a 2.4 GHz 802.15.4 and Bluetooth® Low Energy wireless radio microcontroller based on an ARM® Cortex-M0+ core.

Features

- UART, SPI, I²C, TSI, ADC & DAC
- Same form factor and compatible pinout for VCC, GND, Reset, UART, I²C, and SWD as PAN1026, PAN1760, PAN1760A, and PAN1761
- Single and concurrent operation of IEEE® 802.15.4 and BLE
- Open to various known application layers or proprietary solutions
- Surface Mount Type dimensions: 15.6 mm x 8.7 mm x 1.9 mm
- On module 32 MHz and 32 kHz crystal
- SoC: NXP® Kinetis® KW41Z – 2.4 GHz 802.15.4 and BLE 4.2 Wireless Radio Microcontroller
- Core: Up to 48 MHz 32 bit ARM® Cortex-M0+
- Memory: 512 kB of flash and 128 kB of SRAM
- Voltage range: 1.8 V to 4.2 V
- Temperature range: -40 °C to 85 °C

Characteristics

- Transceiver frequency range 2360 MHz to 2483.5 MHz
- Programmable transmitter output power: -30 dBm to 3 dBm
- Receiver sensitivity (BLE): -93 dBm
- Receiver sensitivity typical for IEEE® Standard 802.15.4: -98 dBm
- Typical receiver current consumption (3.6 V supply): 8.5 mA
- Transmitter current consumption (3.6 V supply, 0 dBm): 7.6 mA

Bluetooth®

- Bluetooth® LE 4.2 compliant implementation certified by BT SIG
- Supporting software consisting of BLE host stack and profiles and IPv6 6LoBLE
- Bluetooth® Developer Studio Plug-In

IEEE® 802.15.4

- IEEE® standard 802.15.4 compliant
- Supporting software consisting of 802.15.4 MAC/PHY implementation, Simple Media Access Controller (SMAC), and NXP®'s certified Thread® stack

Block Diagram

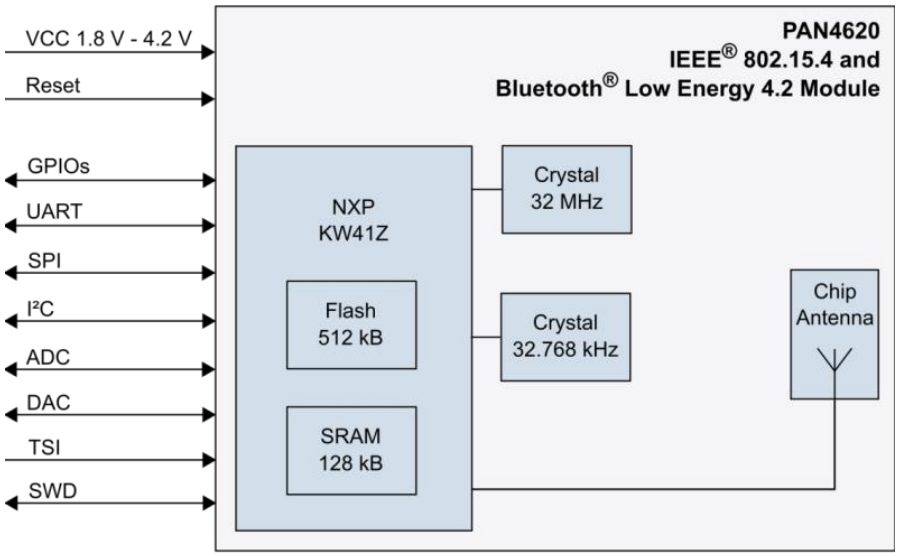


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Table of Contents

1 About This Document

1.1 Purpose and Audience

This Product Specification provides details on the functional, operational, and electrical characteristics of the Panasonic PAN4620 module. It is intended for hardware design, application, and Original Equipment Manufacturers (OEM) engineers. The product is referred to as “the PAN4620” or “the module” within this document.

1.2 Revision History

Revision	Date	Modifications/Remarks
0.1	28.02.2018	1st preliminary version.

1.3 Use of Symbols

Symbol	Description
	**Note** Indicates important information for the proper use of the product. Non-observance can lead to errors.
	**Attention** Indicates important notes that, if not observed, can put the product’s functionality at risk.
⇨ [chapter number] [chapter title]	**Cross reference** Indicates cross references within the document. **Example:** Description of the symbols used in this document ⇨ 1.3 Use of Symbol.

1.4 Related Documents

Please refer to the Panasonic website for related documents ⇨ 7.3.2 Product Information.

2 Overview

The PAN4620 is Panasonic's Internet of Things dual mode module comprising NXP's Kinetis KW41Z SoC - a 2.4 GHz 802.15.4 and Bluetooth® Low Energy wireless radio microcontroller based on an ARM® Cortex-M0+ core.

To provide maximum flexibility, the module can be operated in stand-alone and hosted mode. With 512 kB flash memory and 128 kB SRAM the PAN4620 can easily be used as a stand-alone controller eliminating the need for an external processor, saving complexity, space and cost. It is thus well suited for very small and low-power applications. However, also the integration of 802.15.4 and/or BLE connectivity into existing applications can easily be achieved when using the PAN4620 in hosted mode.

Using the PAN4620 with low power consumption in combination with NXP®'s certified Thread® stack, BLE stack or a combination of both for concurrent operation allows to meet IoT application requirements without the need for a gateway. Since Thread® does not define an application layer, various application layers can be used, such as dotdot, IoTivity, OpenDOF, and others.

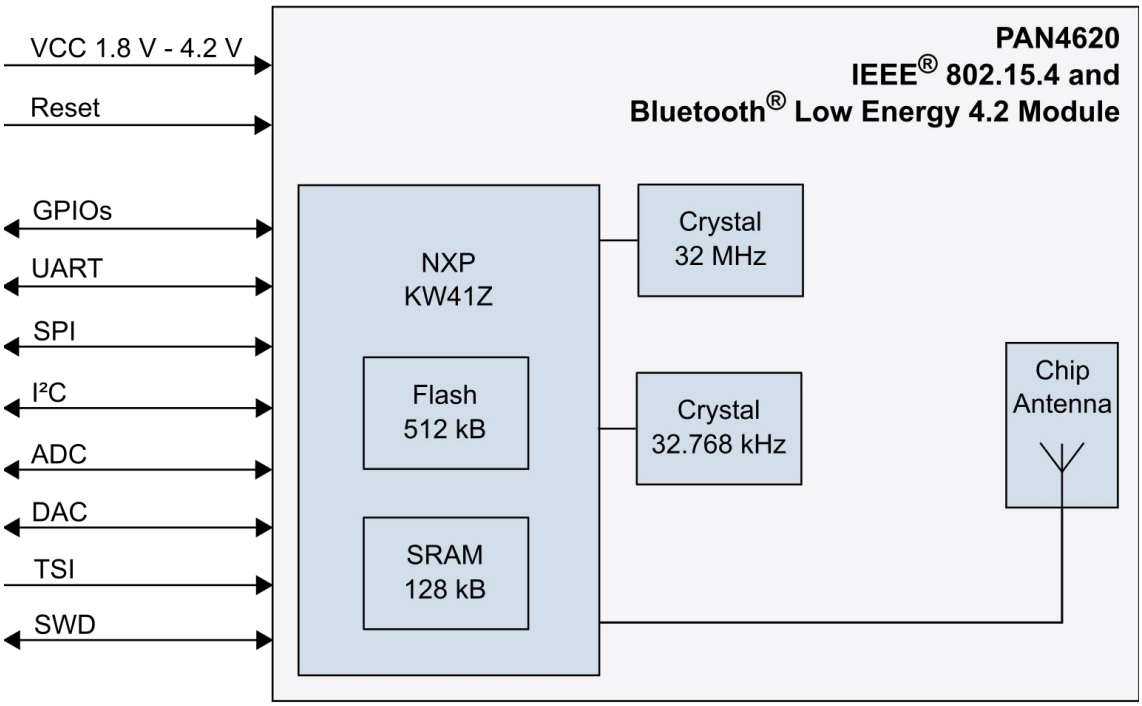
FCC, IC, and CE approval are under way.

Please refer to the Panasonic website for related documents ⇨ 7.3.2 Product Information.

Further information on the variants and versions ⇨ 7.1 Ordering Information.

For further information please also refer to the MKW41Z512CAT4 datasheet and reference manual from NXP®.

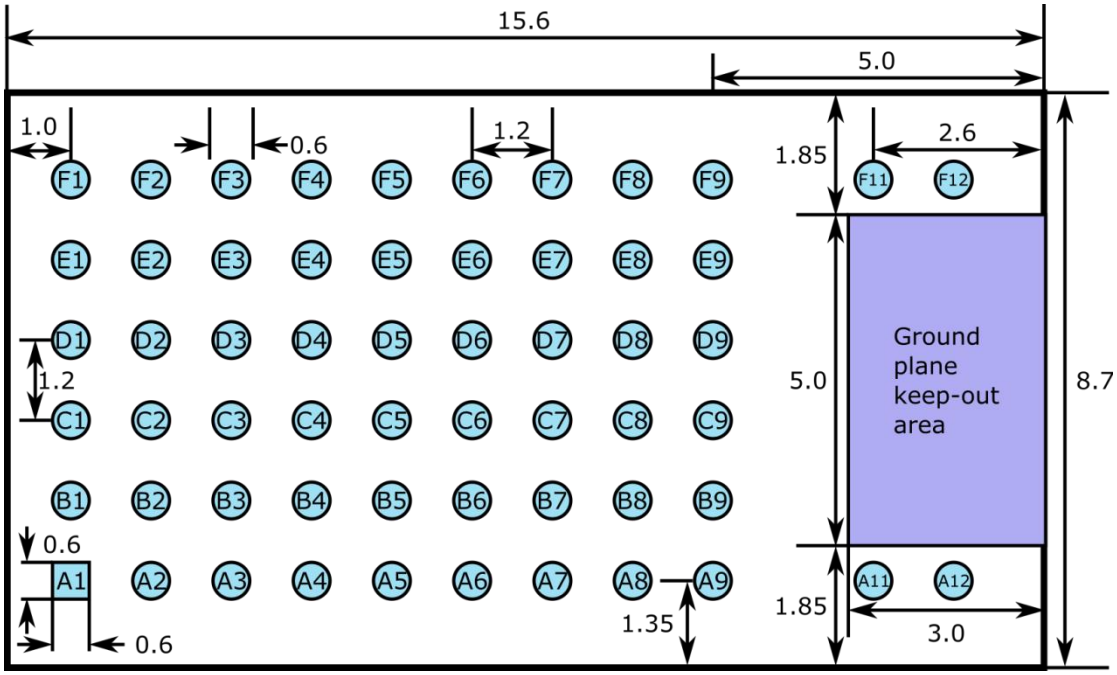
2.1 Block Diagram



2.2 Pin Configuration

Pin Assignment

Top view with all values in [mm]



Pin Functions

No	Pin Name	Alternative Pin	Pin Type	Description
A1	GND		Ground	Connect to ground
A2	NC			Not connected
A3	RESET	PTA2, TPM0_CH3	Digital I/O	Can be configured to use the mentioned alternative pin functions.
A4	NC			Not connected
A5	VCC		Power	Supply voltage 1.8 V to 4.2 V
A6	VCC		Power	Supply voltage 1.8 V to 4.2 V
A7	GND		Ground	Connect to ground
A8	PTC18	TSI0_CH6, LLWU_P2, SPI0_SIN, I2C1_SDA, LPUART0_TX, BSM_DATA, DTM_TX	Digital I/O	Can be configured to use the mentioned alternative pin functions.

No	Pin Name	Alternative Pin	Pin Type	Description
A9	GND		Ground	Connect to ground
A11	GND		Ground	Connect to ground
A12	GND		Ground	Connect to ground
B1	NC			Not connected
B2	PTA17	TSI0_CH11, LLWU_P5, RF_RESET, SPI1_SIN, TPM_CLKIN1	Digital I/O	Can be configured to use the mentioned alternative pin functions.
B3	PTC19	TSI0_CH7, LLWU_P3, SPI0_PCS0, I2C0_SCL, LPUART0_CTS_b, BSM_CLK, BLE_RF_ACTIVE	Digital I/O	Can be configured to use the mentioned alternative pin functions.
B4	PTC17	TSI0_CH5, LLWU_P1 SPI0_SOUT, I2C1_SCL LPUART0_RX, BSM_FRAME, DTM_RX	Digital I/O	Can be configured to use the mentioned alternative pin functions.
B5	PTC16	TSI0_CH4, LLWU_P0, SPI0_SCK, I2C0_SDA, LPUART0_RTS_b, TPM0_CH3	Digital I/O	Can be configured to use the mentioned alternative pin functions.
B6	PTA16	TSI0_CH10, LLWU_P4, SPI1_SOUT, TPM0_CH0	Digital I/O	Can be configured to use the mentioned alternative pin functions.
B7	NC			Not connected
B8	NC			Not connected
B9	NC			Not connected
C1	NC			Not connected
C2	PTA19	TSI0_CH13, ADC0_SE5, LLWU_P7, SPI1_PCS0, TPM2_CH1	Digital I/O	Can be configured to use the mentioned alternative pin functions.
C3	PTA18	TSI0_CH12, LLWU_P6, SPI1_SCK, TPM2_CH0	Digital I/O	Can be configured to use the mentioned alternative pin functions.
C4	SWDIO	PTA0, TSI0_CH8, SPI0_PCS1, TPM1_CH0, SWD_DIO	Digital I/O	Can be configured to use the mentioned alternative pin functions.
C5	SWDCLK	PTA1, TSI0_CH9, SPI1_PCS0, TPM1_CH1, SWD_CLK	Digital I/O	Can be configured to use the mentioned alternative pin functions.

No	Pin Name	Alternative Pin	Pin Type	Description
C6	PTC1	I2C0_SDA, LPUART0_RTS_b, TPM0_CH2, BLE_RF_ACTIVE	Digital I/O	Can be configured to use the mentioned alternative pin functions.
C7	NC			Not connected
C8	GND		Ground	Connect to ground
C9	GND		Ground	Connect to ground
D1	PTB0	LLWU_P8, XTAL_OUT_EN, I2C0_SCL, CMP0_OUT, TPM0_CH1, CLKOUT	Digital I/O	Can be configured to use the mentioned alternative pin functions.
D2	PTB1	ADC0_SE1, CMP0_IN5, DTM_RX, I2C0_SDA, LPTMR0_ALT1, TPM0_CH2, CMT_IRO	Digital I/O	Can be configured to use the mentioned alternative pin functions.
D3	PTB2	ADC0_SE3, CMP0_IN3, RF_NOT_ALLOWED, DTM_TX, TPM1_CH0	Digital I/O	Can be configured to use the mentioned alternative pin functions.
D4	PTB3	ADC0_SE2, CMP0_IN4, CLKOUT, TPM1_CH1, RTC_CLKOUT	Digital I/O	Can be configured to use the mentioned alternative pin functions.
D5	NC			Not connected
D6	NC			Not connected
D7	GND		Ground	Connect to ground
D8	GND		Ground	Connect to ground
D9	ANT			
E1	PTC3	TSI0_CH15, LLWU_P11, RX_SWITCH, I2C1_SDA, LPUART0_TX, TPM0_CH1, DTM_TX	Digital I/O	Can be configured to use the mentioned alternative pin functions.
E2	PTC2	TSI0_CH14, LLWU_P10, TX_SWITCH, I2C1_SCL, LPUART0_RX, CMT_IRO, DTM_RX	Digital I/O	Can be configured to use the mentioned alternative pin functions.
E3	NC			Not connected
E4	NC			Not connected
E5	PTC0	LLWU_P9, I2C0_SCL, LPUART0_CTS_b, TPM0_CH1	Digital I/O	Can be configured to use the mentioned alternative pin functions.

No	Pin Name	Alternative Pin	Pin Type	Description
E6	PTC6	TSI0_CH2, LLWU_P14, XTAL_OUT_EN, I2C1_SCL, LPUART0_RX, TPM2_CH0, BSM_FRAME	Digital I/O	Can be configured to use the mentioned alternative pin functions.
E7	NC			Not connected
E8	GND		Ground	Connect to ground
E9	GND		Ground	Connect to ground
F1	GND		Ground	Connect to ground
F2	NC			Not connected
F3	ADC0_DP0, CMP0_IN0		Analog	
F4	ADC0_DM0, CMP0_IN1		Analog	
F5	PTC4	TSI0_CH0, LLWU_P12, LPUART0_CTS_b, TPM1_CH0, BSM_DATA	Digital I/O	Can be configured to use the mentioned alternative pin functions.
F6	PTB18	DAC0_OUT, ADC0_SE4, CMP0_IN2, I2C1_SCL, TPM_CLKIN0, TPM0_CH0	Digital I/O	Can be configured to use the mentioned alternative pin functions.
F7	PTC7	TSI0_CH3, LLWU_P15, SPI0_PCS2, I2C1_SDA, LPUART0_TX, TPM2_CH1, BSM_DATA	Digital I/O	Can be configured to use the mentioned alternative pin functions.
F8	PTC5	TSI0_CH1, LLWU_P13, RF_NOT_ALLOWED LPTMR0_ALT2, LPUART0_RTS_b, TPM1_CH1, BSM_CLK	Digital I/O	Can be configured to use the mentioned alternative pin functions.
F9	GND		Ground	Connect to ground
F11	GND		Ground	Connect to ground
F12	GND		Ground	Connect to ground

2.3 Transceiver Features

The PAN4620 features an integrated chip antenna and corresponding matching networks.

Both, a high accuracy 32 MHz crystal and a low frequency clock are integrated in the module. Therefore, no external crystal is required to make full use of the reduced power modes.

The operating frequency is in the ISM band and the MBAN band from 2360 MHz to 2483.5 MHz with a programmable output power from -30 dBm to 3 dBm

2.3.1 Bluetooth® Features

- Bluetooth® LE v4.2 (1 Mbps)
- Two simultaneous connections (2 independent hardware connection engines)
- Receive sensitivity of –93 dBm

For further information see ⇨ 4.9 Transceiver Feature Summary.

2.3.2 IEEE® 802.15.4 Features

- IEEE® Standard 802.15.4-2011 compliant OQPSK modulation
- Receive sensitivity of -98 dBm (Receive sensitivity in generic FSK modes depends on mode selection and data rate.)
- Hardware acceleration for packet processing/link layer
- NXP®'s certified Thread® stack

For further information see ⇨ 4.9 Transceiver Feature Summary.

2.3.3 MCU Features

The KW41Z features an ARM® Cortex-M0+MCU with up to 48 MHz. As compared to Cortex-M0, the Cortex-M0+ uses an optimized 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction).

2.3.3.1 Interrupt Controller

- Supports up to 32 interrupt request sources
- 32 vectored interrupts, 4 programmable priority levels
- Includes a single non-maskable interrupt
- Supports interrupt handling when system clocking is disabled in low power modes

2.3.3.2 On chip memory

- 512 kB flash memory implemented as two equal 256 kB blocks.
- One block can be read or erased, while code is being executed or read from the other.
- Flash can be marked execute only in 8 kB blocks to prevent code being from being read by third parties.
- 128 kB SRAM
- The chip features security circuitry to prevent unauthorized access to RAM and flash contents through the debugger.

2.3.3.3 Debug Controller

- Serial wire debug (SWD) interface
- Hardware breakpoint unit for 2 code addresses
- Hardware watchpoint unit for 2 data items
- Micro trace buffer for program tracing

2.3.4 Security Features

- Advanced encryption standard accelerator (AES-128 Accelerator)
- True random number generator (TRNG)
- Flash memory protection

2.3.5 Power Management Control Unit

- Supports external voltage sources of 2.1 V to 4.2 V and is therefore ideally suited for single coin-cell battery operation.
- Programmable power saving modes
- Integrated low frequency clock to make full use of the reduced power modes
- Available wake-up from power saving modes via internal and external sources
- Integrated power-on reset (POR)
- Integrated low voltage detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable low voltage warning (LVW) interrupt capability
- Individual peripheral clocks can be gated off to reduce current consumption
- Internal buffered bandgap reference voltage
- Factory programmed trim for bandgap and LVD
- 1 kHz low power oscillator (LPO)

2.3.6 Peripheral Features

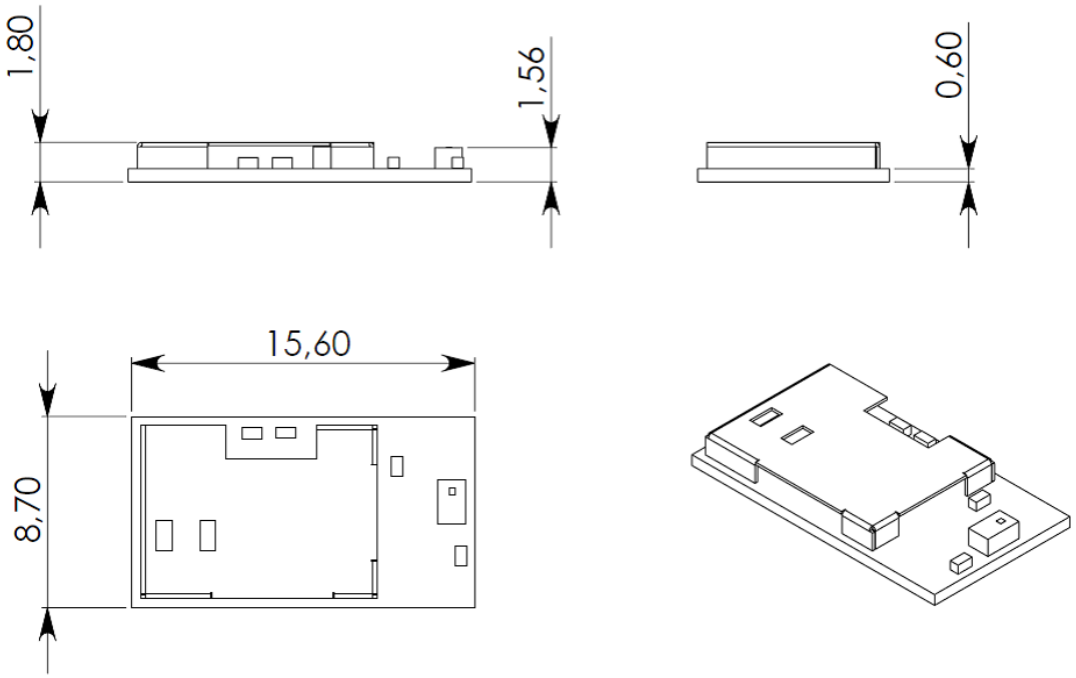
- 16-bit analog-to-digital converter
- 12-Bit digital-to-analog converter
- High-speed analog comparator (CMP)
- Timer: low power timer (LPTMR), timer/PWM, programmable interrupt timer (PIT),
- Real-time clock (RTC)
- Inter-integrated circuit (I^2C), two channels, up to 400 kHz, multi-master operation
- Low power universal asynchronous receiver transmitter (LPUART), one channel full-duplex operation
- Serial peripheral interface (SPI), master and slave mode, full-duplex, three-wire synchronous transfers
- Carrier modulator timer (CMT) with four modes of operation
- Touch sensor input with up to 16 external electrodes
- 24 General purpose Input/Outputs
- GPIOs can be configured to function as a interrupt driven keyboard scanning matrix

For further information see ⇨4.6 Interface Specification.

3 Detailed Description

3.1 Dimensions

All dimensions are in millimeters.

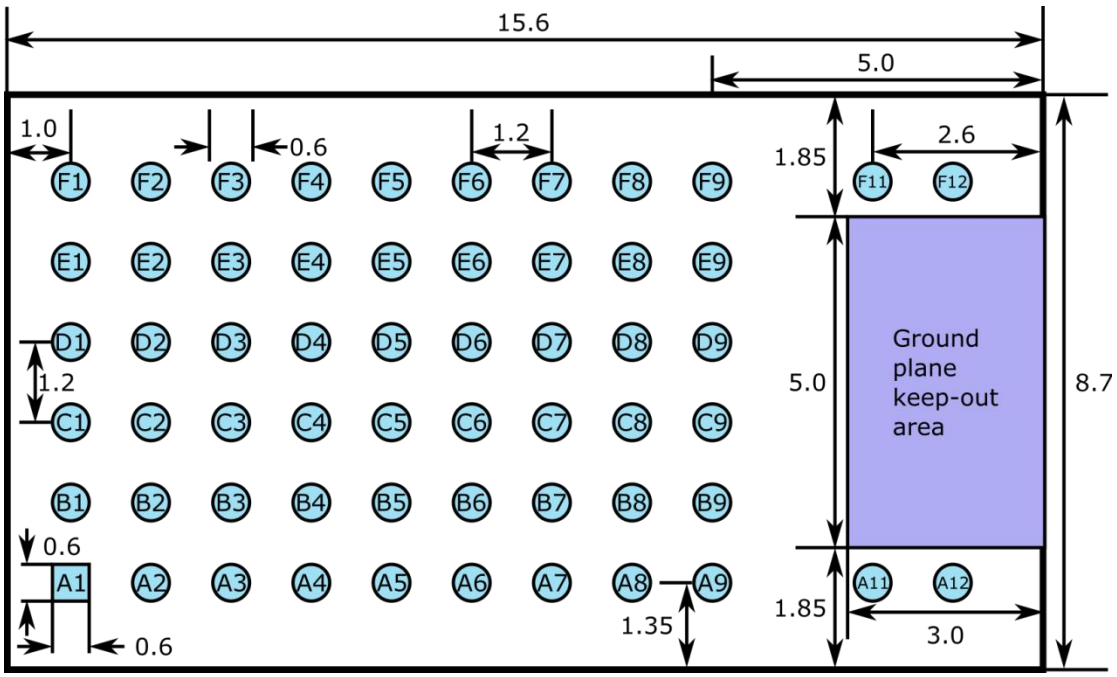


No.	Item	Dimension	Tolerance	Remark
1	Width	8.70	± 0.35	
2	Length	15.60	± 0.35	
3	Height	1.80	± 0.35	With case

3.2 Footprint

The outer dimensions have a tolerance of ±0.35 mm.

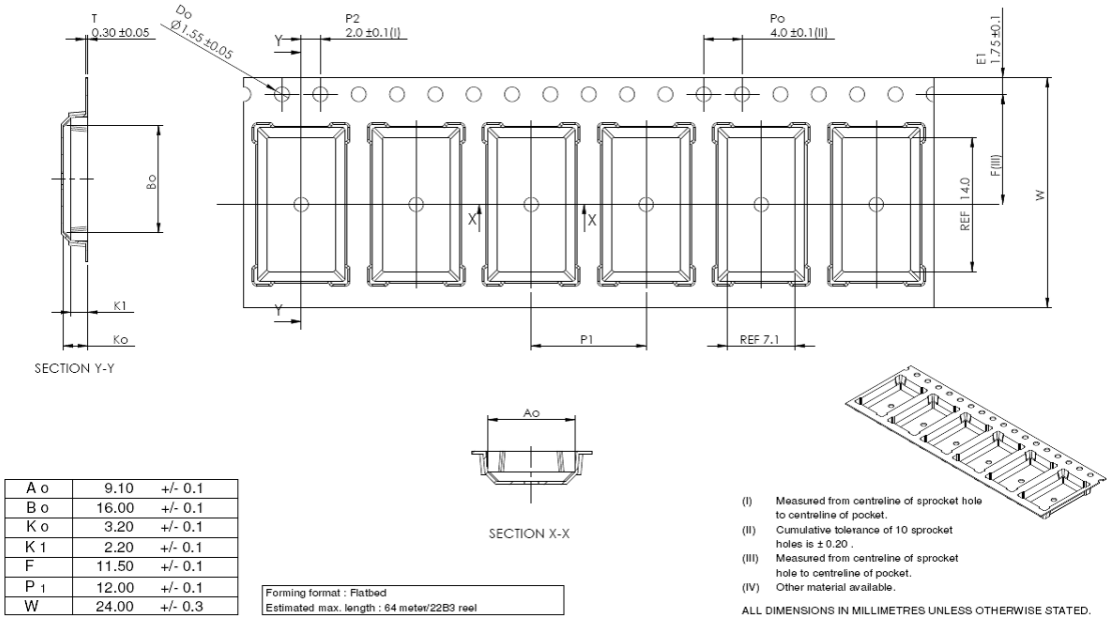
Top view with all values in [mm]



3.3 Packaging

The product is an engineering sample status product and will be delivered in the package described below.

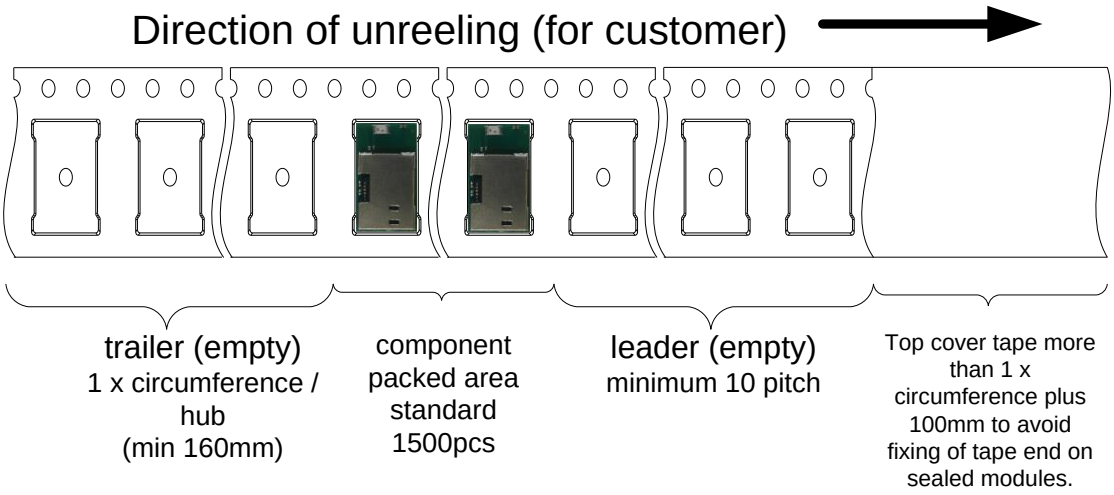
3.3.1 Tape Dimensions



A o	9.10	+/- 0.1
B o	16.00	+/- 0.1
K o	3.20	+/- 0.1
K 1	2.20	+/- 0.1
F	11.50	+/- 0.1
P 1	12.00	+/- 0.1
W	24.00	+/- 0.3

Forming format : Flatbed
Estimated max. length : 64 meter/22B3 reel

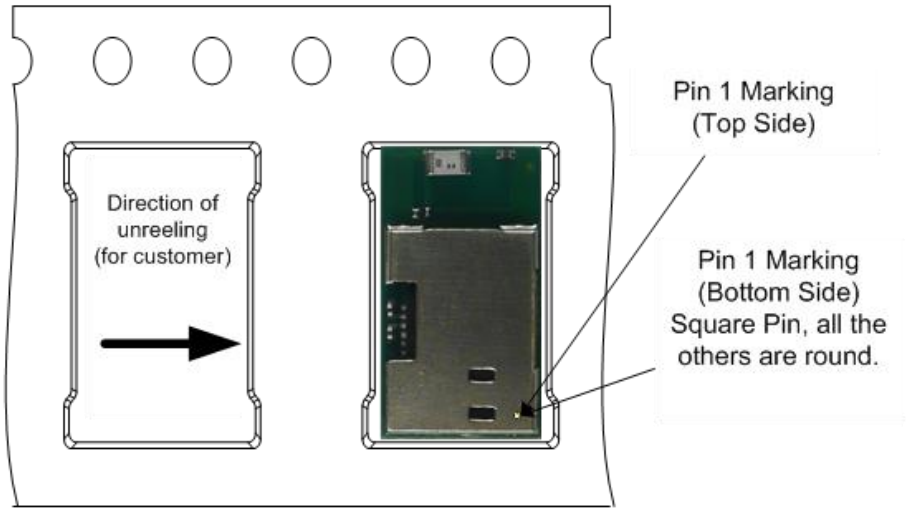
3.3.2 Packing in Tape



Empty spaces in the component packed area shall be less than two per reel and those spaces shall not be consecutive.

The top cover tape shall not be found on reel holes and it shall not stick out from the reel.

3.3.3 Component Direction



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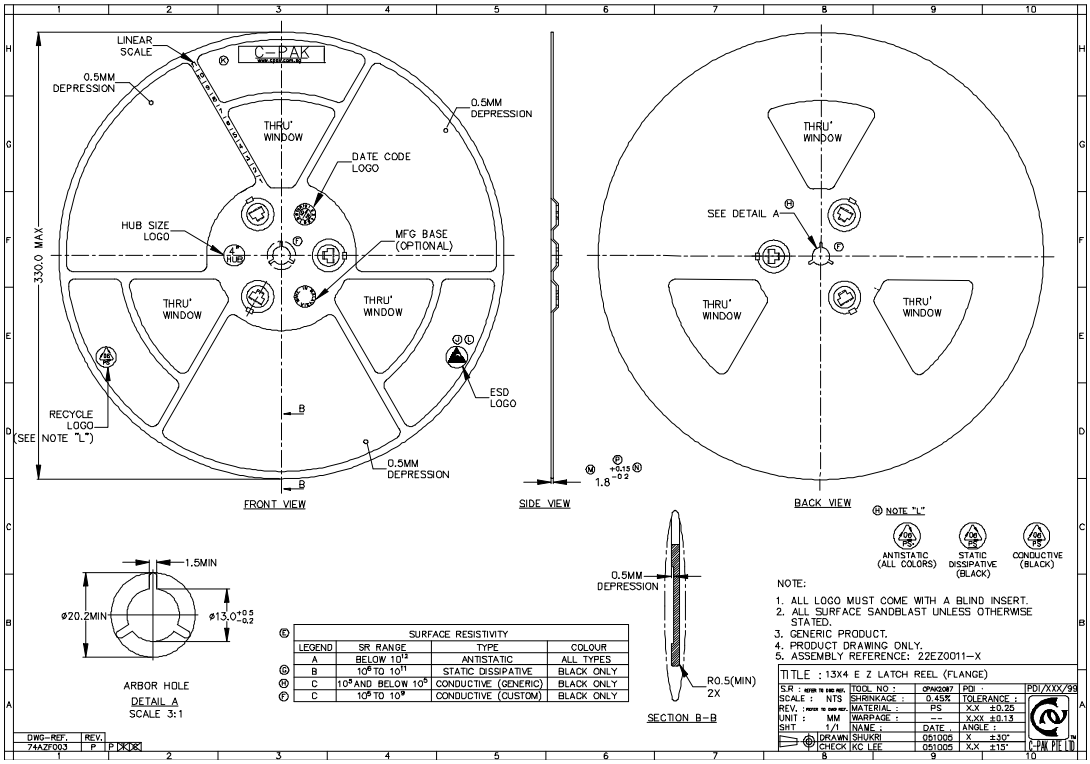
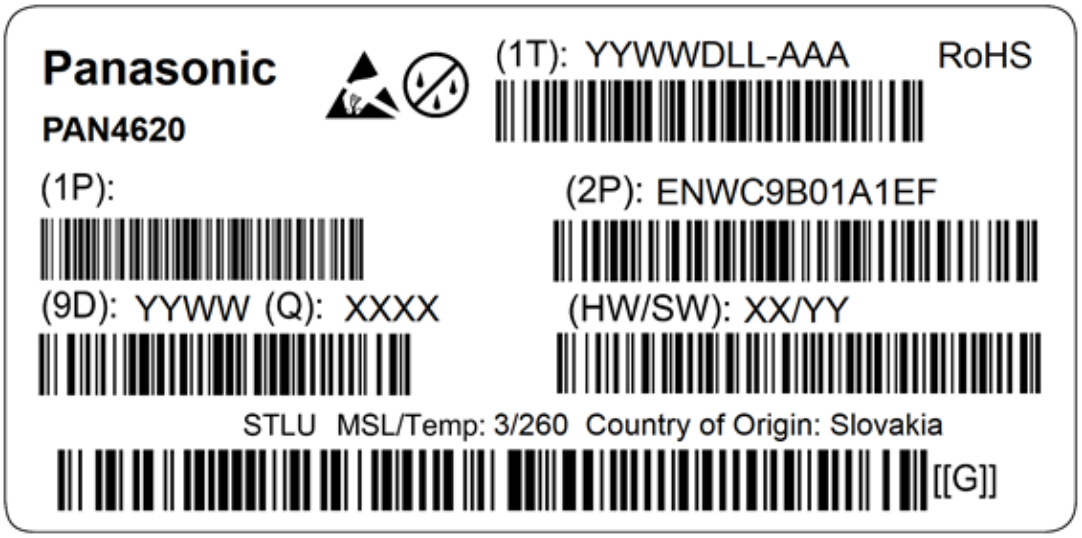
3.3.4 Reel Dimension



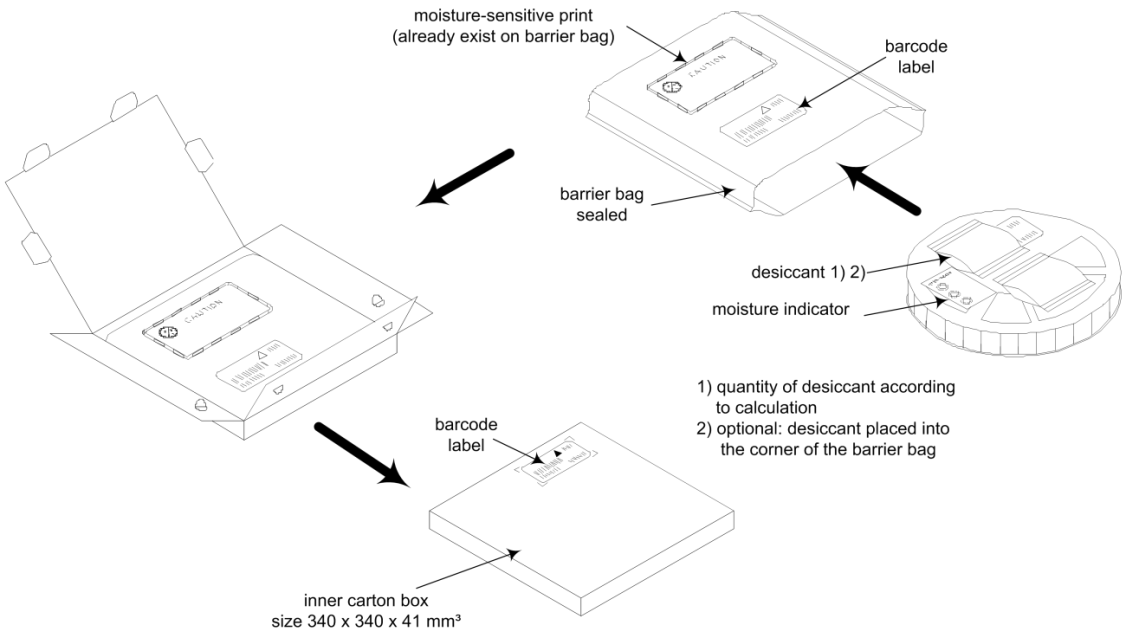
SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{3} AND BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
C	10^{5} TO 10^{6}	CONDUCTIVE (CUSTOM)	BLACK ONLY

3.3.5 Package Label

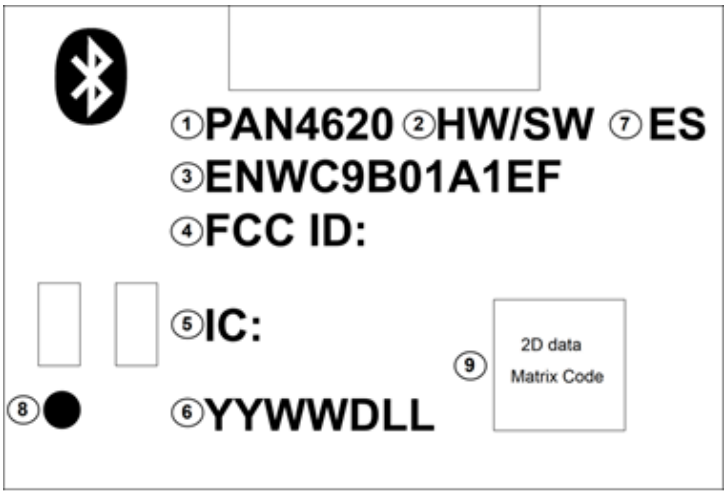


(1T)	Lot code
(1P)	Customer order number, if applicable
(2P)	Order number
(9D)	Date code
(Q)	Quantity
(HW/SW)	Hardware/software version

3.3.6 Total Package



3.4 Case Marking



1	PAN4620
2	Hardware/Software Version
3	ENW-No. / Model Name
4	FCC ID
5	IC ID
6	Lot code
7	Engineering Sample marking, if applicable
8	Marking for Pin 1
9	2D barcode, for internal usage only

4 Specification

All specifications are over temperature and process, unless indicated otherwise.

4.1 Default Test Conditions

Temperature:	25 ± 10 °C
Humidity:	40 to 85 % RH
Supply Voltage:	3.6 V

4.2 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{STOR}	Storage Temperature		-40		+85	°C
V_{ESD}	ESD robustness	Electrostatic discharge voltage, human body model	-2000		+2000	V
		Electrostatic discharge voltage, charged-device model	-500		+500	V
RF input power	P_{max}				10	dBm
V_{DD}	Supply voltage		-0.3		4.2	V
V_{IO}	Voltage on any IO pin		-0.3		V_{DD}+0.3	V

4.3 Recommended Operating Conditions

The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	DCDC converter needs 2.1 V min to start, the supply can drop to min. of 1.8 V after DCDC converter settles.	Start up 2.1 Operating 1.8[1]		4.2	V
f_{IN}	Input frequency		2.36		2.48	GHz
T_A	Ambient temperature range		-40	25	85	°C
V_{IO}	Voltage on any IO pin		-0.3		V_{DD}+0.3	V
I_D	Instantaneous max. current	Single pin limit (applies to all port pins)	-25		25	mA
V_{IL}	Logic low input voltage		0		0.3· $V_{DD\,INT}$[2]	V
V_{IH}	Logic high input voltage		0.7·$V_{DD\,INT}$		$V_{DD\,INT}$	V

[1] DC-DC converter requires slightly higher input voltage during startup. Bit DCDC_STS_DC_OK will be set when the DC-DC converter finished the startup sequence. Typical startup time is 50 ms and it varies with the loading of the converter.

[2] $V_{DD\,INT}$ is the internal LDO regulated voltage supplying various circuit blocks, $V_{DD\,INT}$=1.2 V.

4.4 Current Consumption

The current consumption depends on the user scenario and on the setup and timing in the power modes.

Assume V_{DD} = 3.6 V, T_{amb} = 25 °C, if nothing else is stated.

Parameter	Condition	Min.	Typ.	Max.	Units
Typical average RX current	Measured under continuous RX with MCU stop / Flash doze		8.4		mA
Typical average TX (0 dBm) current	Measured under continuous TX with MCU stop / Flash doze		7.6		mA
Typical average RX current	Measured under continuous RX with MCU run / Flash enabled		10.2		mA
Typical average TX (0 dBm) current	Measured under continuous TX with MCU run / Flash enabled		9.6		mA
Low Power Mode current	Current consumption in very low leakage stop mode		182		nA

4.5 Internal Operating Frequencies

Symbol	Parameter	Condition	Max.	Unit
f_{SYS}	System and core clock	Normal run mode	48	MHz
f_{BUS}	Bus clock	Normal run mode	24	MHz
f_{FLASH}	Flash clock	Normal run mode	24	MHz
f_{LPTMR}	LPTMR clock	Normal run mode	24	MHz
f_{SYS}	System and core clock	VLPR and VLPS mode[3]	4	MHz
f_{BUS}	Bus clock	VLPR and VLPS mode[3]	1	MHz
f_{FLASH}	Flash clock	VLPR and VLPS mode[3]	1	MHz
f_{LPTMR}	LPTMR clock[4]	VLPR and VLPS mode[3]	24	MHz
f_{ERCLK}	External reference clock	VLPR and VLPS mode[3]	16	MHz

[3] The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.

[4] The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

Symbol	Parameter	Condition	Max.	Unit
$f_{LPTMR-ERCLK}$	LPTMR external reference clock	VLPR and VLPS mode[3]	16	MHz
f_{TPM}	TPM asynchronous clock	VLPR and VLPS mode[3]	8	MHz
$f_{LPUART0}$	LPUART0 asynchronous clock	VLPR and VLPS mode[3]	12	MHz

4.6 Interface Specification

4.6.1 LPUART

See also Section ⇨ 4.8 General switching specification.

Signal Name	Description	I/O	Pad
LPUART0_RX	Receive Data	I	B4, E2, E6
LPUART0_TX	Transmit Data	I/O	A8, E1, F7
LPUART0_CTS_b	Clear To Send	I	B3, E5, F5
LPUART0_RTS_b	Request To Send	O	B5, C6, F8

Description	Range	Default.
Baud rate	Programmable baud rates (13-bit modulo divider)	115200
Data bits	Programmable 8-bit or 9-bit data format	8 data bits
Parity bits	Hardware parity generation and checking	No parity
Stop bit	1-2	One stop bit

4.6.2 Inter-Integrated Circuit (I^2C)

Two I^2C channels. See also Section ⇨ 4.8 General switching specification.

Signal Name	Module	Description	I/O	Pad
I2C0_SCL	I2C0	I^2C serial clock line	I/O	B3, D1, E5
I2C0_SDA	I2C0	I^2C serial data line	I/O	B5, C6, D2
I2C1_SCL	I2C1	I^2C serial clock line	I/O	B4, E2, E6
I2C1_SDA	I2C1	I^2C serial data line	I/O	A8, E1, F7

I²C timing (compare **Figure 1**):

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{HD}; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4	-	0.6	-	µs
t_{SU}; STA	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
t_{HD}; DAT	Data hold time for I²C bus devices	0[5]	3.45[6]	0[7]	0.9[6]	µs
t_{SU}; DAT	Data set-up time	250[8]	-	100[6,9]	-	ns
t_r	Rise time of SDA and SCL signals	-	1000	20+0.1C_b[10]	300	ns
t_f	Fall time of SDA and SCL signals	-	300	20+0.1C_b[9]	300	ns
t_{SU}; STO	Set-up time for STOP condition	4	-	0.6	-	µs
t_{BUF}	Bus free time between STOP and START condition	4.7	-	1.3	-	µs
t_{SP}	Width of spikes that must be suppressed by the input filter	N/A	N/A	0	50	µs

[5] The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

[6] The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

[7] Input signal Slew = 10 ns and Output Load = 50 pF.

[8] Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.

[9] A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU}; DAT ≥ 250 ns must then be met. This is automatically the case, if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

[10] C_b = total capacitance of the one bus line in pF.

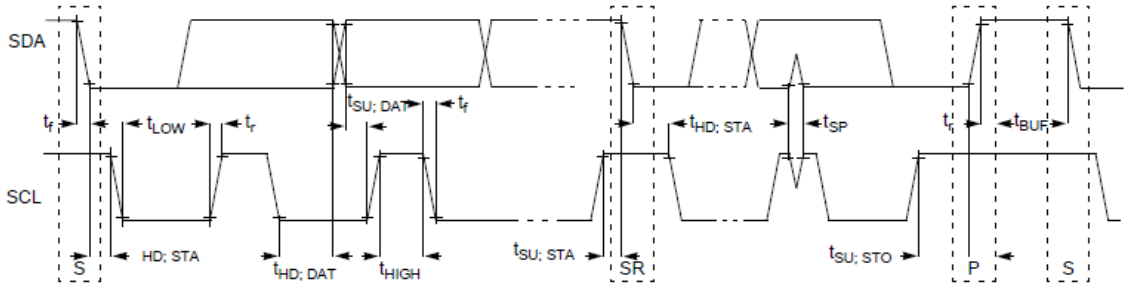


Figure 1 - Timing definition for fast and standard mode devices on the I^2C bus.

4.6.3 DMA Serial Peripheral Interface (DSPI)

Two independent SPI channels Master/Slave.

Signal Name	Module	Description	I/O	Pad
SPI0_PCS0	SPI0	Chip Select/Slave Select	I/O	B3
SPI0_PCS1	SPI0	Chip Select	O	C4
SPI0_PCS2	SPI0	Chip Select	O	F7
SPI0_SCK	SPI0	Serial Clock	I/O	B5
SPI0_SIN	SPI0	Data In	I	A8
SPI0_SOUT	SPI0	Data Out	O	B4
SPI1_PCS0	SPI1	Chip Select/Slave Select	I/O	B3
SPI1_SCK	SPI1	Serial Clock	I/O	C3
SPI1_SIN	SPI1	Data In	I	B2
SPI1_SOUT	SPI1	Data Out	O	B6

4.6.3.1 DSPI switching specifications (limited voltage range)

Master mode DSPI timing (compare **Figure 2**):

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation	-	12	MHz
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	-	ns
DS2	DSPI_SCK output high/low time	(t_{SCK}/2)-2	(t_{SCK}/2)+2	ns
DS3	DSPI_PCSn valid to DSPI_SCK delay[11]	(t_{BUS} x 2)-2	-	ns

[11] The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

Symbol	Description	Min.	Max.	Unit
DS4	DSPI_SCK to DSPI_PCSn invalid delay[12]	(t_{BUS} x 2)-2	-	ns
DS5	DSPI_SCK to DSPI_SOUT valid	-	8.5	ns
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	-	ns
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	-	ns
DS8	DSPI_SCK to DSPI_SIN input hold	0	-	ns

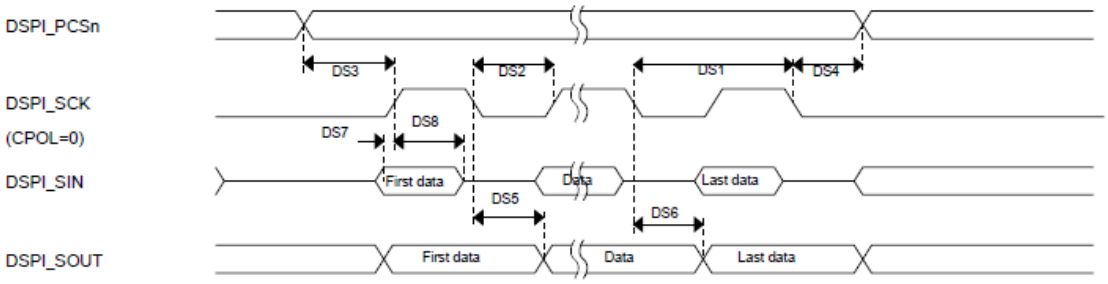


Figure 2 - Master mode DSPI timing.

Slave mode DSPI timing (compare **Figure 3**):

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation	-	6	MHz
DS9	DSPI_SCK output cycle time	4 x t_{BUS}	-	ns
DS10	DSPI_SCK output high/low time	(t_{SCK}/2)-2	(t_{SCK}/2)+2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	-	21.4	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	-	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	-	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	-	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	-	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	-	14	ns

[12] The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

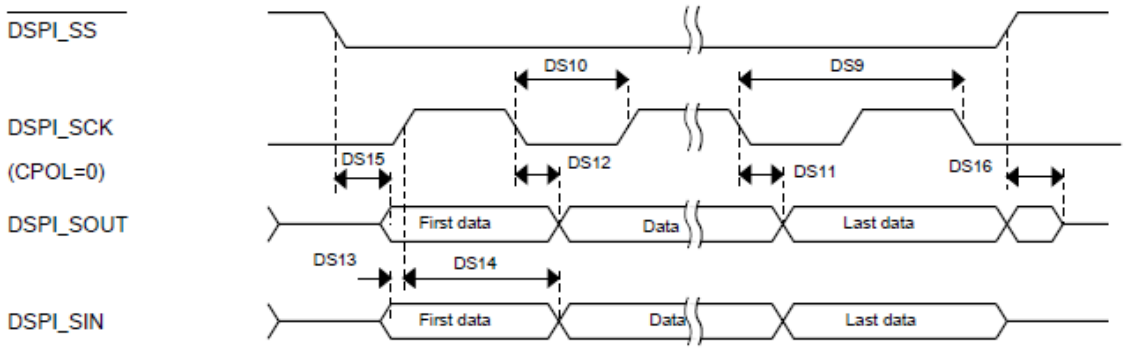


Figure 3 - Slave mode DSPI timing.

4.6.3.2 DSPI switching specifications (full voltage range)

Master mode DSPI timing (compare **Figure 4**):

Symbol	Description	Min.	Max.	Unit
	Operating voltage[13]	1.71	3.6	V
	Frequency of operation	-	12	MHz
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	-	ns
DS2	DSPI_SCK output high/low time	(t_{SCK}/2)-4	(t_{SCK}/2)+4	ns
DS3	DSPI_PCSn valid to DSPI_SCK delay[14]	(t_{BUS} x 2)-4	-	ns
DS4	DSPI_SCK to DSPI_PCSn invalid delay[15]	(t_{BUS} x 2)-4	-	ns
DS5	DSPI_SCK to DSPI_SOUT valid	-	10	ns
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	-	ns
DS7	DSPI_SIN to DSPI_SCK input setup	23.3	-	ns
DS8	DSPI_SCK to DSPI_SIN input hold	0	-	ns

[13] The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.

[14] The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

[15] The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

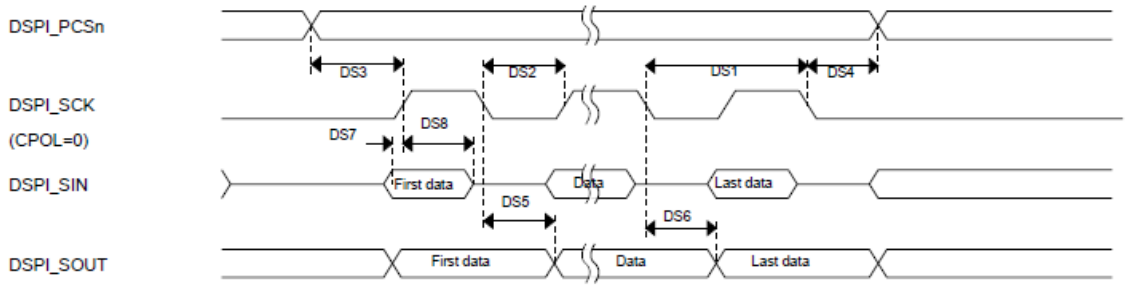


Figure 4 - Master mode DSPI timing.

Slave mode DSPI timing (compare **Figure 5**):

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	-	6	MHz
DS9	DSPI_SCK output cycle time	4 x t_{BUS}	-	ns
DS10	DSPI_SCK output high/low time	(t_{SCK}/2)-4	(t_{SCK}/2)+4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	-	29.1	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	-	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	-	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	-	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	-	25	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	-	25	ns

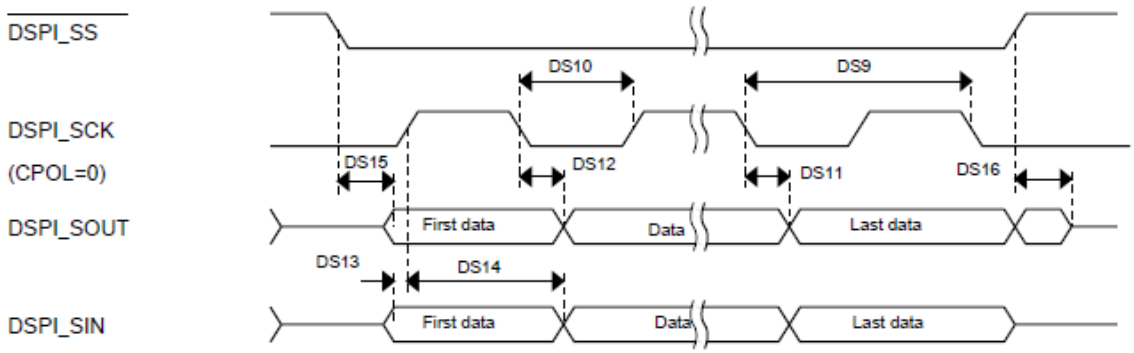


Figure 5 - Slave mode DSPI timing.

4.6.4 Carrier Modulator Timer (CMT)

Please see also Section ⇨ 4.8 General switching specification.

Signal Name	Description	I/O	Pad
CMT_IRO	Carrier Modulator Transmitter Infrared Output	O	D2, E2

4.6.5 Touch Sensing Input (TSI)

Signal Name	Description	I/O	Pad
TSI0_CH[15:0]	Touch sensing input capacitive pins	I/O	TSI0_CH0 → F5
			TSI0_CH1 → F8
			TSI0_CH2 → E6
			TSI0_CH3 → F7
			TSI0_CH4 → B5
			TSI0_CH5 → B4
			TSI0_CH6 → A8
			TSI0_CH7 → B3
			TSI0_CH8 → C4
			TSI0_CH9 → C5
			TSI0_CH10 → B6
			TSI0_CH11 → B2
			TSI0_CH12 → C3
			TSI0_CH13 → C2
			TSI0_CH14 → E2
			TSI0_CH15 → E1

TSI electrical specifications:

Symbol	Description	Min.	Typ	Max.	Unit
T_a	Ambient temperature	-30	-	85	°C
TSI_RUNF	Fixed power consumption in run mode	-	100	-	µA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	-	128	µA
TSI_EN	Power consumption in enable mode	-	100	-	µA
TSI_DIS	Power consumption in disable mode	-	1.2	-	µA
TSI_TEN	TSI analog enable time	-	66	-	µs

Symbol	Description	Min.	Typ	Max.	Unit
TSI_CREF	TSI reference capacitor	-	1.0	-	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	-	1.03	V

4.6.6 General Purpose Input/Output (GPIO)

Signal Name	Description	I/O	Pad
PTA[19:16][2:0]	General Purpose Input/Output	I/O	PTA0 → C4
			PTA1 → C5
			PTA2 → A3
			PTA16 → B6
			PTA17 → B2
			PTA18 → C3
			PTA19 → C2
PTB[18][3:0]	General Purpose Input/Output	I/O	PTB0 → D1
			PTB1 → D2
			PTB2 → D3
			PTB3 → D4
			PTB18 → F3
PTC[19:16][7:0]	General Purpose Input/Output	I/O	PTC0 → E5
			PTC1 → A8
			PTC2 → E2
			PTC3 → E1
			PTC4 → F5
			PTC5 → F8
			PTC6 → E6
			PTC7 → F7
			PTC16 → B5
			PTC17 → B4
			PTC18 → A8
			PTC19 → B3

The maximum input voltage on PTC0/1/2/3 is V_{DD}+0.3V.

Please see also ⇨ 4.8 General switching specification.

4.6.7 Low-Leakage Wakeup (LLWU)

Signal Name	Description	I/O	Pad
LLWU_P[15:0]	Wakeup inputs	I	LLWU_P0 → B5
			LLWU_P1 → B4
			LLWU_P2 → A8
			LLWU_P3 → B3
			LLWU_P4 → B6
			LLWU_P5 → B2
			LLWU_P6 → C3
			LLWU_P7 → C2
			LLWU_P8 → D1
			LLWU_P9 → E5
			LLWU_P10 → E2
			LLWU_P11 → E1
			LLWU_P12 → F5
			LLWU_P13 → F8
			LLWU_P14 → E6
			LLWU_P15 → F7

4.6.8 Radio Module Signals

Signal Name	Description	I/O	Pad
DTM_RX	Direct test mode receive	I	B4, D2, E2
DTM_TX	Direct test mode transmit	O	A8, D3, E1
BSM_CLK	Bit streaming mode (BSM) clock signal, 802.15.4 packet data stream clock line	O	B3, F8
BSM_FRAME	Bit streaming mode frame signal, 802.15.4 packet data stream frame line	O	B4, E6
BSM_DATA	Bit streaming mode data signal, 802.15.4 packet data stream data line	I/O	A8, F5, F7
RF_RESET	Radio reset signal	I	B2
BLE_RF_ACTIVE	Signal to indicate future BLE activity.	O	B3, C6
RF_NOT_ALLOWED	Radio off signal, intended for Wi-Fi coexistence control	I	D3, F8

Signal Name	Description	I/O	Pad
RX_SWITCH	Front end module receive mode signal	O	E1
TX_SWITCH	Front end module transmit mode signal	O	E2

4.6.9 Analog-to-Digital Converter (ADC)

Signal Name	Description	I/O	Pad
ADC0_DM0	ADC channel 0 differential input negative	I	F4
ADC0_DP0	ADC channel 0 differential input positive	I	F3
ADC0_SE[5:1]	ADC channel 0 single-ended input	I	ADC0_SE1 → D2
			ADC0_SE2 → D4
			ADC0_SE3 → D3
			ADC0_SE4 → F6
			ADC0_SE5 → C2

16-bit ADC operating conditions:

Symbol	Description	Min.	Typ[16]	Max.	Unit
V_{DDA}	Supply voltage absolute	1.71	-	3.6	V
V_{REFH}	ADC reference voltage high, internally sourced and factory trimmed	-	1.2	-	V
V_{REFL}	ADC reference voltage low	-	GND	-	
V_{ADIN}	Input voltage: 16-bit differential mode All other modes	 V_{REFL} V_{REFL}	 - -	 $31/32 \cdot V_{REFH}$ V_{REFH}	 V V
C_{ADIN}	Input capacitance: 16-bit mode 8-bit / 10-bit / 12-bit modes	 - -	 8 4	 10 5	 pF pF
R_{ADIN}	Input series resistance	-	2	5	kΩ
R_{AS}	Analog source resistance (external) 13-bit / 12-bit modes f_{ADCK} < 4 MHz	-	-	5	kΩ
f_{ADCK}	ADC conversion clock frequency[17]				

[16] Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.

Symbol	Description	Min.	Typ[16]	Max.	Unit
	≤ 13-bit mode	1.0	-	18.0	MHz
	16-bit mode	2.0	-	12.0	MHz
C_{rate}	ADC conversion rate: No ADC hardware averaging, continuous conversions enabled, subsequent conversion time				
	≤ 13-bit modes	20.000	-	818.330	ksps
	16-bit mode	37.037	-	461.467	ksps

4.6.10 12-bit Digital-to-analog converter (DAC)

Signal Name	Description	I/O	Pad
DAC0_OUT	DAC output	O	F6

12-bit DAC operating requirements:

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Supply voltage	1.71	3.6	V
V_{DACR}	Reference voltage[18]	1.2	3.6	V
C_L	Output load capacitance[19]	-	100	pF
I_L	Output load current	-	1	mA

12-bit DAC operating behaviors:

Symbol	Description	Min.	Typ	Max.	Unit
I_{DDA_DACLP}	Supply current - low-power mode	-	-	250	µA
I_{DDA_DACHP}	Supply current – high speed mode	-	-	900	µA
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) - low-power mode[20]	-	100	200	µs
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) - high-speed mode[20]	-	15	30	µs

[17] To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.

[18] The DAC reference can be selected to be V_{DDA} or V_{REFH}=1.2 V.

[19] A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

[20] Settling within ±1 LSB.

Symbol	Description	Min.	Typ	Max.	Unit
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) - low-power mode and high-speed mode[20]	-	0.7	1	µs
$V_{dacoutl}$	DAC output voltage range low - high-speed mode, no load, DAC set to 0x000	-	-	100	mV
$V_{dacouth}$	DAC output voltage range high – high-speed mode, no load, DAC set to 0xFFF	V_{DACR}-100	-	V_{DACR}	mV
INL	Integral non-linearity error – high-speed mode[21]	-	-	±8	LSB
DNL	Differential non-linearity error - V_{DACR} > 2 V[22]	-	-	±1	LSB
DNL	Differential non-linearity error - V_{DACR} = VREF_OUT[23]	-	-	±1	LSB
V_{OFFSET}	Offset error[24]	-	±0.4	±0.8	%FSR
E_G	Gain error[24]	-	±0.1	±0.6	%FSR
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	-	90	dB
T_{CO}	Temperature coefficient offset voltage[25]	-	3.7	-	µV/C
T_{GE}	Temperature coefficient gain error	-	0.000421	-	%FSR/C
R_{OP}	Output resistance (load = 3 kΩ)	-	-	250	Ω
SR	Slew rate: High-power Low-power	 1.2 0.05	 1.7 0.12	 - -	 V/µs V/µs
BW	3 dB bandwidth: High-power Low-power	 550 40	 - -	 - -	 kHz kHz

[21] The INL is measured for 0 + 100 mV to V_{DACR} −100 mV.

[22] The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV.

[23] The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V.

[24] Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV.

[25] V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high-power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device.

4.6.11 Analog Comparator (CMP)

Signal Name	Description	I/O	Pad
CMP0_IN[5:0]	Analog voltage inputs	I	CMP0_IN0 → F3
			CMP0_IN1 → F4
			CMP0_IN2 → F6
			CMP0_IN3 → D3
			CMP0_IN4 → D4
			CMP0_IN5 → D2
CMP0_OUT	Comparator output	O	D1

CMP and 6-bit DAC electrical specifications:

Symbol	Description	Min.	Typ	Max.	Unit
V_{DD}	Supply voltage	1.71	-	3.6	
I_{DDHS}	Supply current, high-speed mode (EN=1, PMODE=1)	-	-	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	-	-	20	µA
V_{AIN}	Analog input voltage	V_{SS}-0.3	-	V_{DD}	V
V_{AIO}	Analog input offset voltage	-	-	20	mV
V_H	Analog comparator hysteresis[26]				
	CR0[HYSTCTR] = 00	-	5	-	mV
	CR0[HYSTCTR] = 01	-	10	-	mV
	CR0[HYSTCTR] = 10	-	20	-	mV
	CR0[HYSTCTR] = 11	-	30	-	mV
V_{CMPOh}	Output high	V_{DD}-0.5	-	-	V
V_{CMPOl}	Output low	-	-	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[27]	-	-	40	µs

[26] Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.

Symbol	Description	Min.	Typ	Max.	Unit
I_{DAC6b}	6-bit DAC current adder (enabled)	-	7	-	µA
INL	6-bit DAC integral non-linearity	-0.5	-	0.5	LSB[28]
DNL	6-bit DAC differential non-linearity	-0.3	-	0.3	LSB

4.6.12 Timer

Signal Name	Module	Description	I/O	Pad
TPM_CLKIN[1:0]	TPM0	External clock	I	TPM_CLKIN0 → F6
				TPM_CLKIN1 → B2
TPM0_CH[3:0]	TPM0	TPM channel	I/O	TPM0_CH0 → F6, B6
				TPM0_CH1 → D1, E1
				TPM0_CH2 → C6, D2
				TPM0_CH3 → A3, B5
TPM_CLKIN[1:0]	TPM1	External clock	I	TPM_CLKIN0 → F6
				TPM_CLKIN1 → B2
TPM1_CH[1:0]	TPM1	TPM channel	I/O	TPM1_CH0 → C4, C5, F5
				TPM1_CH1 → D3, D4, F8
TPM_CLKIN[1:0]	TPM2	External clock	I	TPM_CLKIN0 → F6
				TPM_CLKIN1 → B2
TPM2_CH[1:0]	TPM2	TPM channel	I/O	TPM2_CH0 → C3, E6
				TPM2_CH1 → C2, F7
LPTMR0_ALT[2:1]	LPTMR0	Pulse counter input pin	I	LPTMR0_ALT1 → D2
				LPTMR0_ALT2 → F8
RTC_CLKOUT	RTC Module	1 Hz square-wave output	O	D4

[27] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.

[28] 1 LSB = $V_{reference}/64$

4.6.13 Clocks

Signal Name	Description	I/O	Pad
CLKOUT	Internal clocks monitor	O	D1, D4
XTAL_OUT_EN	32 MHz clock output enable	I	D1, E6

4.6.14 Serial Wire Debug (SWD)

Signal Name	Description	Comment	I/O	Pad
SWD_DIO	Serial wire debug data Input/Output	Pulled up internally by default	I/O	C4
SWD_CLK	Serial wire clock	Pulled down internally by default	I	C5

SWD full voltage range electricals as shown in **Figure 6** and **Figure 7**:

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation	-	25	MHz
J2	SWD_CLK cycle period	1/J1	-	ns
J3	SWD_CLK clock pulse width	20	-	ns
J4	SWD_CLK rise and fall times	-	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	-	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	-	ns
J11	SWD_CLK high to SWD_DIO data valid	-	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	-	ns

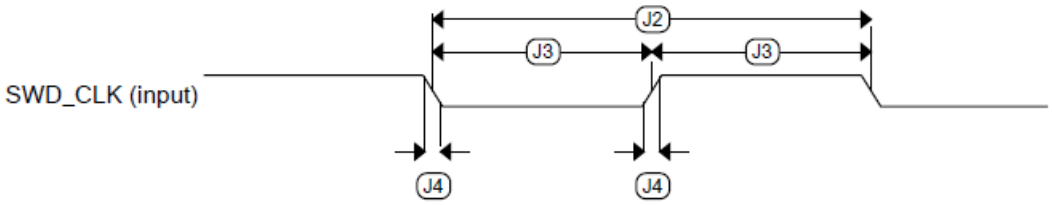


Figure 6 - SWD clock input timing.

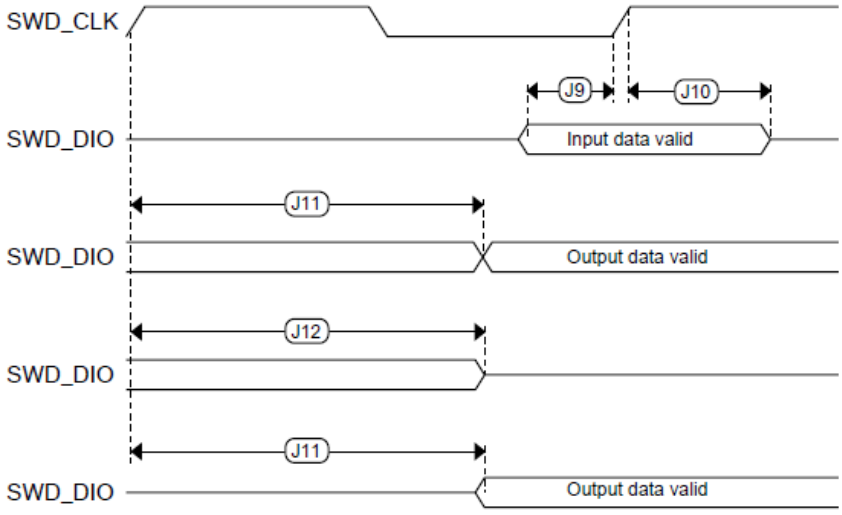


Figure 7 - SWD data timing.

4.7 Flash electrical specifications

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Flash timing specifications - program and erase:

Symbol	Description	Min.	Typ	Max.	Unit
t_{hvpgm4}	Longword program high-voltage time	-	7.5	18	µs
$t_{hversscr}$	Sector erase high-voltage time[29]	-	13	113	ms
$t_{hversblk256k}$	Erase block high-voltage time for 256 KB[29]	-	104	904	ms

Flash timing specifications - commands:

Symbol	Description	Min.	Typ	Max.	Unit
$t_{rd1blk256k}$	Read 1s block execution time[30] 256 KB program flash	-	-	1.7	ms
$t_{rd1sec2k}$	Read 1s section execution time (flash sector)[30]	-	-	60	µs
t_{pgmchk}	Program check execution time[30]	-	-	45	µs
t_{rdrsrc}	Read resource execution time[30]	-	-	30	µs

[29] Maximum time based on expectations at cycling end-of-life.

[30] Assumes 25 MHz flash clock frequency.

Symbol	Description	Min.	Typ	Max.	Unit
t_{pgm4}	Program longword execution time	-	65	145	µs
$t_{ersblk256k}$	Erase flash block execution time[31] 256 KB program flash	-	250	1500	ms
t_{ersscr}	Erase flash sector execution time[31]	-	14	114	ms
t_{rd1all}	Read 1s all blocks execution time[30]	-	-	1.8	ms
t_{rdonce}	Read once execution time[30]	-	-	30	µs
$t_{pgmonce}$	Program once execution time	-	100	-	µs
t_{ersall}	Erase all blocks execution time[31]	-	500	3000	ms
t_{vfykey}	Verify backdoor access key execution time[30]	-	-	30	µs
$t_{ersallu}$	Erase all blocks unsecure execution time[31]	-	500	3000	ms

Flash high voltage current behaviors:

Symbol	Description	Min.	Typ	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	-	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	-	1.5	4.0	mA

4.8 General switching specification

These specifications apply to GPIO, LPUART, CMT, and I2C signals.

Description	Min.	Max.	Unit
GPIO pin interrupt pulse width (digital glitch filter disabled) - Synchronous path[32,33]	1.5	-	Bus clock cycles
Reset pin interrupt pulse width (analog filter enabled) - Asynchronous path[34]	200	-	ns
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) - Asynchronous path[5]	20	-	ns
External RESET_b input pulse width (digital glitch filter disabled)	100	-	ns

[31] Maximum times for erase parameters based on expectations at cycling end-of-life.

[32] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.

[33] The greater of synchronous and asynchronous timing must be met.

[34] This is the minimum pulse width that is guaranteed to be recognized.

Description	Min.	Max.	Unit
Port rise and fall time(low drive strength)[35,36]			
Slew enabled:			
1.71 ≤ V_{DD} ≤ 2.7 V	-	25	ns
2.7 ≤ V_{DD} ≤ 3.6 V	-	16	ns
Slew disabled:			
1.71 ≤ V_{DD} ≤ 2.7 V	-	8	ns
2.7 ≤ V_{DD} ≤ 3.6 V	-	6	ns
Port rise and fall time(low drive strength)[37,38]			
Slew enabled:			
1.71 ≤ V_{DD} ≤ 2.7 V	-	24	ns
2.7 ≤ V_{DD} ≤ 3.6 V	-	16	ns
Slew disabled:			
1.71 ≤ V_{DD} ≤ 2.7 V	-	10	ns
2.7 ≤ V_{DD} ≤ 3.6 V	-	6	ns

4.9 Transceiver Feature Summary

The PAN4620 module meets or exceeds all Bluetooth® Low Energy v4.2 and IEEE® 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands.

4.9.1 Channel Plan

Channel Plan for Bluetooth® Low Energy:

Band	Carrier frequency [MHz][39]	Channel number k
ISM	2402 + k · 2	k = [0,1,…,38,39]

Channel Plan for IEEE® 802.15.4:

Band	Carrier frequency [MHz][40]	Channel number k
ISM	2405 + (k-11) · 5	k = [11,12,…,25,26]

[35] PTB0, PTB1, PTC0, PTC1, PTC2, PTC3, PTC6, PTC7, PTC17, PTC18.

[36] 75 pF load.

[37] Ports A, B, and C.

[38] 25 pF load.

[39] All the RX parameters are measured at the PAN4620 RF bottom pad.

[40] All the RX parameters are measured at the PAN4620 RF bottom pad.

Band	Carrier frequency [MHz][40]	Channel number k
MBAN	2363 + k · 5	k = [0,1,2,3,4,5,6]
	2367 + (k-7) · 5	k = [7,8,9,10,11,12,14]

4.9.2 Receiver Feature Summary

The current consumption and sensitivity depend on the user scenario.

Assume V_{DD} = 3.6 V, T_{amb} = 25 °C, if nothing else is stated.

Symbol	Description[40]	Min.	Typ.	Max.	Units
I_{RXon}	Supply current Rx On (V_{DD} = 3.6 V)[41]	-	8.4	-	mA
f_{IN}	Input RF frequency	2.36	-	2.4835	GHz
$SENS_{GFSK}$	GFSK Rx sensitivity (250 kbps GFSK-BT=0.5, h=0.5)	-	-98	-	dBm
$SENS_{BLE}$	BLE Rx sensitivity[42]	-	-93	-	dBm
$SENS_{15.4}$	IEEE® 802.15.4 Rx sensitivity[43]	-	-98	-	dBm
$RSSI_{Range}$	Receiver signal strength indicator range[44]	tbd	-	tbd	dBm
$RSSI_{Res}$	Receiver signal strength indicator resolution	-	1	-	dBm
	Typical RSSI variation over frequency	tbd	-	tbd	dB
	Typical RSSI variation over temperature	tbd	-	tbd	dB
$RSSI_{ACC}$	Narrowband RSSI accuracy[45]	-3	-	3	dBm
$BLE_{co\text{-}channel}$	BLE Co-channel Interference (Wanted signal at -67 dBm, BER <0.1 %. Measurement resolution 1 MHz)	-	tbd	-	dB
$15.4_{co\text{-}channel}$	IEEE® 802.15.4 Co-channel Interference (Wanted signal 3 dB over reference sensitivity level)	-	tbd	-	dB

Adjacent/Alternate channel performance[46]:

[41] Transceiver power consumption.

[42] Measured at 0.1 % BER using 37 byte long packets in max gain mode and nominal conditions.

[43] In max. gain mode and nominal conditions.

[44] RSSI performance in narrowband mode.

[45] With one point calibration over frequency and temperature.

[46] BLE adjacent and block parameters are measured with modulated interference signals.

Symbol	Condition	Min.	Typ.	Max.	Units
$SEL_{BLE, 1 MHz}$	BLE Adjacent +/- 1 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1 %. Measurement resolution 1 MHz.)	-	tbd	-	dB
$SEL_{BLE, 2 MHz}$	BLE Adjacent +/- 2 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1 %. Measurement resolution 1 MHz.)	-	tbd	-	dBm
$SEL_{BLE, 3 MHz}$	BLE Alternate ≥ +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1 %. Measurement resolution 1 MHz.)	-	tbd	-	dB
$SEL_{15.4, 5 MHz}$	IEEE® 802.15.4 Adjacent +/- 5 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level, PER <1 %)	-	tbd	-	dB
$SEL_{15.4, 5 MHz}$	IEEE® 802.15.4 Alternate ≥ +/- 10 MHz Interference offset (Wanted signal 3 dB over reference sensitivity level, PER <1 %.)	-	tbd	-	dBm

Intermodulation performance:

Condition	Min.	Typ.	Max.	Units
BLE Intermodulation with continuous wave interferer at ± 3MHz and modulated interferer is at ± 6 MHz (Wanted signal at -67 dBm, BER <0.1 %.)	-	tbd	-	dBm
BLE Intermodulation with continuous wave interferer at ± 5 MHz and modulated interferer is at ± 10 MHz (Wanted signal at -67 dBm, BER <0.1 %.)	-	tbd	-	dBm

Blocking performance[46]:

Condition[49]	Min.	Typ.	Max.	Units
BLE Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at -67 dBm, BER <0.1 %. Interferer continuous wave signal.)[47]	-	tbd	-	dBm
BLE Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000 MHz (Wanted signal at -67 dBm, BER <0.1 %. Interferer continuous wave signal.)	-	tbd	-	dBm
BLE Out of band blocking from 2001 MHz to 2339 MHz and 2484 MHz to 2999 MHz (Wanted signal at -67 dBm, BER <0.1 %. Interferer continuous wave signal.)	-	tbd	-	dBm
BLE Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at -67 dBm, BER <0.1 %. Interferer continuous wave signal.)[47]	-	tbd	-	dBm
IEEE® 802.15.4 Out of band blocking for frequency offsets > 10 MHz and <= 80 MHz (Wanted signal 3 dB over reference sensitivity level, PER <1 %. Interferer continuous wave signal.)[48]	-	tbd	-	dBm
IEEE® 802.15.4 Out of band blocking from carrier frequencies in 1 GHz to 4 GHz range excluding frequency offsets < ±80 MHz (Wanted signal 3 dB over reference sensitivity level, PER <1 %. Interferer continuous wave signal.)	-	tbd	-	dBm
IEEE® 802.15.4 Out of band blocking frequency from carrier frequencies < 1 GHz and > 4 GHz (Wanted signal 3 dB over reference sensitivity level, PER <1 %. Interferer continuous wave signal.)[47]	-	tbd	-	dBm

4.9.3 Transmitter Feature Summary

The current consumption and output power depend on the user scenario.

Assume V_{DD} = 3.6 V, T_{amb} = 25 °C, if nothing else is stated.

Symbol	Description[49]	Min.	Typ.	Max.	Units
I_{TXon}	Supply current TX On with P_{RF} = 0 dBm (V_{DD} = 3.6 V)	-	7.6	-	mA
f_c	Output Frequency	2.36	-	2.4835	GHz
P_{RFmax}	Maximum RF Output power	-	3	-	dBm
P_{RFmin}	Minimum RF Output power	-	-30	-	dBm

[47] Exceptions allowed for carrier frequency harmonics.

[48] Exception to the 10 MHz > frequency offset <= 80 MHz out-of-band blocking limit allowed for frequency offsets of twice the reference frequency.

[49] All the TX parameters are measured at the PAN4620 RF bottom pad.

Symbol	Description[49]	Min.	Typ.	Max.	Units
P_{RFCR}	RF Output power control range	-	33	-	dB
$F_{dev15.4}$	IEEE® 802.15.4 Peak frequency deviation	-	tbd	-	kHz
$EVM_{15.4}$	IEEE® 802.15.4 Error Vector Magnitude (EVM)	-	tbd	-	%
$OEVM_{15.4}$	IEEE® 802.15.4 Offset Error Vector Magnitude	-	tbd	-	%
$TXPSD_{15.4}$	IEEE® 802.15.4 TX spectrum level at 3.5 MHz offset	-	-	tbd	dBc
$\Delta f1_{avg,BLE}$	BLE average frequency deviation using a 00001111 modulation sequence	-	tbd	-	kHz
$\Delta f2_{avg,BLE}$	BLE average frequency deviation using a 01010101 modulation sequence	-	tbd	-	kHz
$F_{cdev,BLE}$	BLE Maximum Deviation of the Center Frequency	-	tbd	-	kHz
$P_{RF2MHz,BLE}$	BLE Adjacent Channel Transmit Power at 2MHz offset	-	-	tbd	dBm
$P_{RF3MHz,BLE}$	BLE Adjacent Channel Transmit Power at >= 3 MHz offset	-	-	tbd	dBm
	BLE Frequency Hopping Support		Yes		
TXH2	2nd Harmonic of Transmit Carrier Frequency (for $P_{out} = P_{RF,max}$),	-	tbd	-	dBm/ MHz
TXH3	3rd Harmonic of Transmit Carrier Frequency (for $P_{out} = P_{RF,max}$),	-	tbd	-	dBm/ MHz
TXH4	4rd Harmonic of Transmit Carrier Frequency (for $P_{out} = P_{RF,max}$),	-	tbd	-	dBm/ MHz
TXH5	5rd Harmonic of Transmit Carrier Frequency (for $P_{out} = P_{RF,max}$),	-	tbd	-	dBm/ MHz
TXH6	6rd Harmonic of Transmit Carrier Frequency (for $P_{out} = P_{RF,max}$),	-	tbd	-	dBm/ MHz

Transmitter output power temperature dependence:

Symbol	Description[50]	-40 °C	25 °C	85 °C	Units
$P_{RF,max}$	Typical maximum RF Output power	tbd	3	tbd	dBm
$P_{RF,min}$	Typical minimum RF Output power	tbd	-30	tbd	dBm

[50] All the TX parameters are measured at the PAN4620 RF bottom pad.

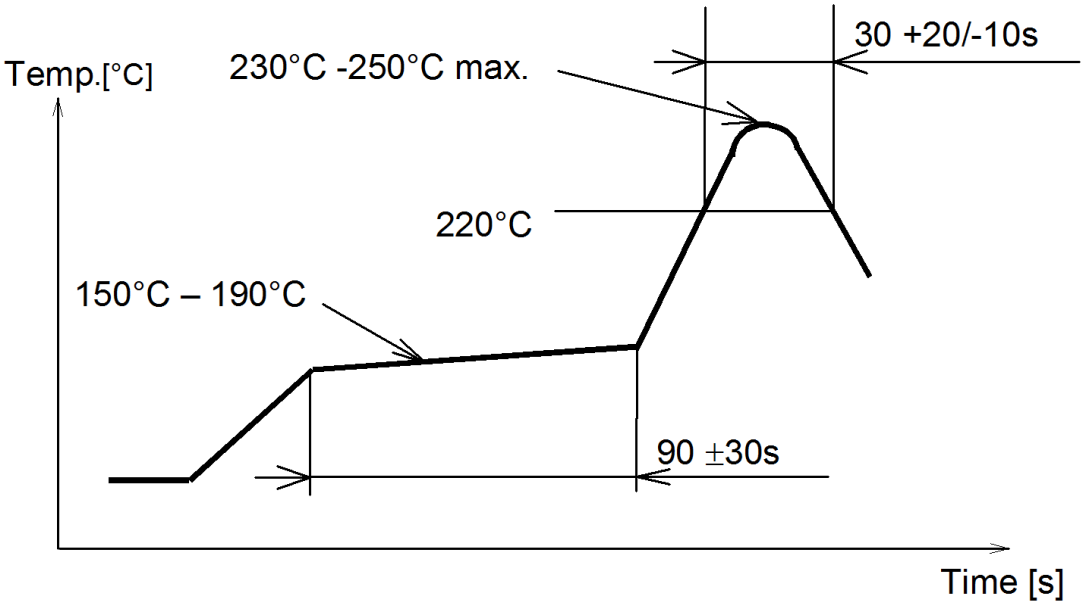
4.10 Reliability Tests

The measurement should be done after the test device has been exposed to room temperature and humidity for one hour.

No.	Item	Limit	Condition
1	Variable Vibration Test (VVT)	Electrical parameter should be in specification	Freq.: 20~2000 Hz, Acc.: 17-50 G, Sweep: 8 min, 2 hours each of XYZ axis
2	Shock Drop Test (DT)	Electrical parameter should be in specification	Drop parts on concrete from a height of 1 m for 3 times
3	Heat-Shock/ Temperature Cycling Test (TC)	Electrical parameter should be in specification	at -40 °C and +85 °C for 1 h/cycle Total = 300 cycles
4	Temperature Humidity Bias Test (THB)	Electrical parameter should be in specification	at +60 °C, 85 °% r.H., 300 h
5	Low Temperature Storage Life Test (LTSL)	Electrical parameter should be in specification	at -40 °C, 300 h
6	High Temperature Storage Life Test (HTSL)	Electrical parameter should be in specification	at +85 °C, 300 h

4.11 Recommended Soldering Profile

- Reflow permissible cycle: 2
- Opposite side reflow is prohibited due to module weight
- More than 75 percent of the soldering area shall be coated by solder
- The soldering profiles should be adhered to in order to prevent electrical or mechanical damage
- Soldering profile assumes lead-free soldering



5 Cautions

Failure to follow the guidelines set forth in this document may result in degrading of the module functions and damage to the module.

5.1 Design Notes

1. Follow the conditions written in this specification, especially the control signals of this module.
2. The supply voltage should abide by the maximum ratings (⇨ 4.2 Absolute Maximum Ratings).
3. The supply voltage must be free of AC ripple voltage (for example from a battery or a low noise regulator output). For noisy supply voltages, provide a decoupling circuit (for example a ferrite in series connection and a bypass capacitor to ground of at least 47 µF directly at the module).
4. This module should not be mechanically stressed when installed.
5. Keep this module away from heat. Heat is the major cause of decreasing the life time of these modules.
6. Avoid assembly and use of the target equipment in conditions where the module temperature may exceed the maximum tolerance.
7. Keep this module away from other high frequency circuits.
8. Refer to the recommended pattern when designing a board.

5.2 Installation Notes

1. Reflow soldering is possible twice based on the conditions set forth in ⇨ 4.11 Recommended Soldering Profile. Set up the temperature at the soldering portion of this module according to this reflow profile.
2. Carefully position the module so that the heat will not burn into printed circuit boards or affect other components that are susceptible to heat.
3. Carefully locate the module, to avoid an increased temperature caused by heat generated by neighboring components.
4. If a vinyl-covered wire comes into contact with the module, the wire cover will melt and generate toxic gas, damaging the insulation. Never allow contact between a vinyl cover and these modules to occur.
5. This module should not be mechanically stressed or vibrated when reflowed.
6. To repair the board by hand soldering, follow the conditions set forth in this chapter.
7. Do not wash this product.
8. Pressing on parts of the metal cover or fastening objects to the metal will cause damage to the module.

5.3 Usage Condition Notes

1. Take measures to protect the module against static electricity.
   If pulses or transient loads (a large load, which is suddenly applied) are applied to the modules, check and evaluate their operation before assembly of the final products.
2. Do not use dropped modules.
3. Do not touch, damage, or soil the pins.
4. Follow the recommended condition ratings about the power supply applied to this module.
5. Electrode peeling strength: Do not apply a force of more than 4.9 N in any direction on the soldered module.
6. Pressing on parts of the metal cover or fastening objects to the metal cover will cause damage.
7. These modules are intended for general purpose and standard use in general electronic equipment, such as home appliances, office equipment, information, and communication equipment.

5.4 Storage Notes

1. The module should not be stressed mechanically during storage.
2. Do not store these modules in the following conditions or the performance characteristics of the module, such as RF performance will be adversely affected:

– Storage in salty air or in an environment with a high concentration of corrosive gas, such as Cl_2, H_2S, NH_3, SO_2, or NO_X,
– Storage in direct sunlight,
– Storage in an environment where the temperature may be outside the range of 5 °C to 35 °C, or where the humidity may be outside the 45 % to 85 % range,
– Storage of the modules for more than one year after the date of delivery storage period: Please check the adhesive strength of the embossed tape and soldering after 6 months of storage.

3. Keep this module away from water, poisonous gas, and corrosive gas.
4. This module should not be stressed or shocked when transported.
5. Follow the specification when stacking packed crates (max. 10).

5.5 Safety Cautions

These specifications are intended to preserve the quality assurance of products and individual components.

Before use, check and evaluate the operation when mounted on your products. Abide by these specifications without deviation when using the products. These products may short-circuit. If electrical shocks, smoke, fire, and/or accidents involving human life are anticipated when a short circuit occurs, provide the following failsafe functions as a minimum:

1. Ensure the safety of the whole system by installing a protection circuit and a protection device.
2. Ensure the safety of the whole system by installing a redundant circuit or another system to prevent a single fault causing an unsafe status.

5.6 Other Cautions

1. Do not use the module for other purposes than those listed in section ⇨ 5.3 Usage Condition Notes.
2. Be sure to provide an appropriate fail-safe function on your product to prevent any additional damage that may be caused by the abnormal function or the failure of the module.
3. This module has been manufactured without any ozone chemical controlled under the Montreal Protocol.
4. These modules are not intended for use under the special conditions shown below. Before using these modules under such special conditions, carefully check their performance and reliability under the said special conditions to determine whether or not they can be used in such a manner:

– In liquid, such as water, salt water, oil, alkali, or organic solvent, or in places where liquid may splash,
– In direct sunlight, outdoors, or in a dusty environment,
– In an environment where condensation occurs,
– In an environment with a high concentration of harmful gas (e. g. salty air, HCl, Cl_2, SO_2, H_2S, NH_3, and NO_X).

5. If an abnormal voltage is applied due to a problem occurring in other components or circuits, replace these modules with new modules, because they may not be able to provide normal performance even if their electronic characteristics and appearances appear satisfactory.
6. When you have any question or uncertainty, contact Panasonic.

5.7 Life Support Policy

This Panasonic Industrial Devices Europe GmbH product is not designed for use in life support appliances, devices, or systems where malfunction can reasonably be expected to result in a significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Panasonic customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Panasonic Industrial Devices Europe GmbH for any damages resulting.

6 Regulatory and Certification Information

6.1 Federal Communications Commission (FCC) for US

Certification is pending.

6.2 Innovation, Science, and Economic Development (ISED) for Canada

Certification is pending.

6.3 European Conformity According to RED (2014/53/EU)

Certification is pending.

6.4 Bluetooth®

Certification is pending.

6.5 RoHS and REACH Declaration

The latest declaration of environmental compatibility (Restriction of Hazardous Substances, RoHS and Registration, Evaluation, Authorisation and Restriction of Chemicals, REACH) for supplied products can be found on the Panasonic website in the “Downloads” section of the respective product ⇨ 7.3.2 Product Information.

7 Appendix

7.1 Ordering Information

Variants and Versions

Order Number	Brand Name	Description	MOQ[51]
ENWC9B01A1EF	PAN4620	IEEE® 802.15.4 and Bluetooth® Low Energy Module	1 500

[51]The default MOQ for mass production is 1 500 pieces, fewer only on customer demand. Samples for evaluation can be delivered at any quantity via the distribution channels.

7.2 List of Acronyms

ADC ..... *Analog-to-digital converter*
AES ..... *Advanced encryption standard*
BLE ..... *Bluetooth® low energy*
BT ..... *Bluetooth®*
CMP ..... *Analog comparator*
CMT ..... *Carrier modulator timer*
DAC ..... *Digital-to-analog converter*
DSPI ..... *DMA Serial peripheral interface*
DT ..... *Shock drop test*
EVM ..... *Error vector magnitude*
GPIO ..... *General purpose Input/Output*
HTSL ..... *High temperature storage life test*
I^2C ..... Inter-integrated circuit
ISM ..... *Industrial, scientific and medical*
LDO ..... *Low drop out*
LE ..... *Low energy*
LLWU ..... *Low-leakage wakeup*
LPO ..... *Low power oscillator*
LPTMR ..... *Low power timer*
LPUART ..... *Low power universal asynchronous receiver transmitter*
LTSL ..... *Low temperature storage life test*
LVD ..... *Low voltage detect*
LVW ..... *Low voltage warning*
MAC ..... *Media access controller*
MBAN ..... *Medical band area network*
MCU ..... *Microcontroller unit*
MOQ ..... *Minimum order quantity*
PIT ..... *Programmable interrupt timer*
POR ..... *Integrated power-on reset*
RAM ..... *Random access memory*
RTC ..... *Real-time clock*
SMAC ..... *Simple media access controller*
SPI ..... *Serial peripheral interface*
SRAM ..... *Static random-access memory*
SWD ..... *Serial wire debug*
TC ..... *Heat-shock/ temperature cycling test*
THB ..... *Temperature humidity bias test*
TPM ..... *Timers module*
TRNG ..... *True random number generator*
TSI ..... *Touch sensing input*
VLPR ..... *Very low power run*
VLPS ..... *Very low power stop*
VVT ..... *Variable vibration test*

7.3 Contact Details

7.3.1 Contact Us

Please contact your local Panasonic Sales office for details on additional product options and services:

For Panasonic Sales assistance in the **EU**, visit

https://eu.industrial.panasonic.com/about-us/contact-us

Email: wireless@eu.panasonic.com

For Panasonic Sales assistance in **North America**, visit the Panasonic Sales & Support Tool to find assistance near you at

https://na.industrial.panasonic.com/distributors

Please visit the **Panasonic Wireless Technical Forum** to submit a question at

https://forum.na.industrial.panasonic.com

7.3.2 Product Information

For further information please also refer to the MKW41Z512CAT4 datasheet and reference manual from NXP®.

Please refer to the Panasonic Wireless Connectivity website for further information on our products and related documents:

For complete Panasonic product details in the **EU**, visit

http://pideu.panasonic.de/products/wireless-modules.html

For complete Panasonic product details in **North America**, visit

http://www.panasonic.com/rfmodules