Ultralow Power 15mA Synchronous Step-Down Switching Regulator

FEATURES

- **High Efficiency: Up to 95%**
- **Maximum Current Output: 15mA**
- **Externally Programmable Frequency Clamp with Internal 50kHz Default Minimizes Audio Noise**
- **18µA I_Q Current**
- **2.9V to 5.5V Input Voltage Range**
- **Low-Battery Detection**
- 0.6V Reference Allows Low Output Voltages
- Shutdown Mode Draws <1µA Supply Current
- 2.8V Undervoltage Lockout
- Unique Low Noise Control Architecture
- Internal Power MOSFETs
- No Schottky Diodes Required
- Internal Soft-Start
- Tiny 2mm × 2mm 8-Lead DFN Package

APPLICATIONS

- Hearing Aids
- Wireless Headsets
- Li-Ion Cell Applications
- Button Cell Replacement

DESCRIPTION

The LTC®3620 is a high efficiency, synchronous buck regulator, suitable for very low power, very small footprint applications powered by a single Li-Ion battery.

The internal synchronous switches increase efficiency and eliminate the need for external Schottky diodes. Low output voltages are easily supported by the 0.6V feedback reference voltage. The LTC3620-1 option is internally programmed to provide a 1.1V output.

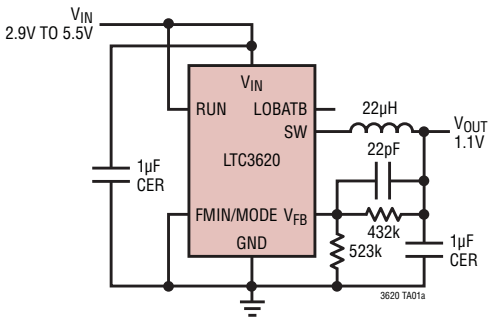
The LTC3620 uses a unique variable frequency architecture to minimize power loss and achieve high efficiency. The switching frequency is proportional to the load current, and an internal frequency clamp forces a minimum switching frequency at light loads to minimize noise in the audio range. The user can program the frequency of this clamp by applying an external clock to the FMIN/MODE pin.

The battery status output, LOBATB, indicates when the input voltage drops below 3V. To help prevent damage to the battery, an undervoltage lockout (UVLO) circuit shuts down the part if the input voltage falls below 2.8V.

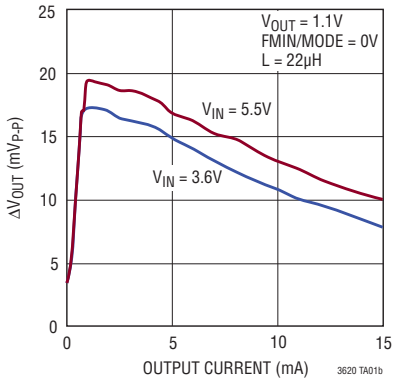
The LTC3620 is available in a low profile, 2mm × 2mm 8-lead DFN package.

TYPICAL APPLICATION

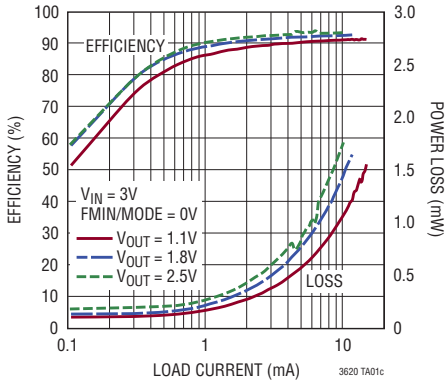
High Efficiency Low Power Step-Down Converter



Output Voltage Ripple vs Load Current



Efficiency vs Load Current

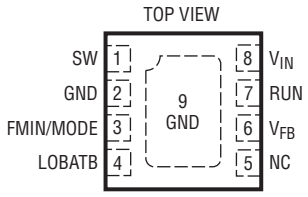


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ..... –0.3V to 6V
RUN Voltage ..... –0.3V to (V_{IN} + 0.3V)
V_{FB} Voltage ..... –0.3V to (V_{IN} + 0.3V)
LOBATB Voltage ..... –0.3V to 6V
FMIN/MODE Voltage ..... –0.3V to (V_{IN} + 0.3V)
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
P-channel Switch Source Current (DC) 50mA
N-channel Switch Sink Current (DC) 50mA
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DC PACKAGE
8-LEAD (2mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 88.5°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3620EDC#PBF	LTC3620EDC#TRPBF	LFJJ	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC3620EDC-1#PBF	LTC3620EDC-1#TRPBF	LFJK	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for T_A = 25°C (Note 2). V_{IN} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		●	2.9		5.5	V
V_{FB}	Regulated Feedback Voltage (Note 3)	LTC3620		0.594	0.6	0.606	V
		LTC3620	●	0.588	0.6	0.612	V
		LTC3620-1		1.089	1.1	1.111	V
		LTC3620-1	●	1.078	1.1	1.122	V
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 3V to 5.5V (Note 3)			0.05	0.15	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 3)				0.5	%
I_Q	Quiescent Current, No Switching	V_{FB} = 0.65V, FMIN/MODE = V_{IN}			18	25	µA
I_{QSD}	Quiescent Current in Shutdown	RUN = 0V			0.01	1	µA
I_{QU}	Quiescent Current in UVLO Condition	RUN = V_{IN}, V_{IN} = 2.5V			0.5		µA
I_{PK}	Peak Inductor Current				35		mA
f_{SW}	Minimum Switching Frequency (Internal)	V_{FB} = 0.65V, FIN/MODE = 0	●	40	50		kHz
V_{RUN}	RUN Input Voltage High			0.8			V
	RUN Input Voltage Low					0.3	V
I_{RUN}	RUN Leakage Current				±0.01	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for T_A = 25°C (Note 2). V_{IN} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FMIN}	FMIN/MODE Input Voltage High			0.9			V
	FMIN/MODE Input Voltage Low					0.7	V
f_{EXT}	FMIN/MODE Input Frequency			20		300	kHz
$I_{FMIN/MODE}$	FMIN/MODE Pin Leakage Current				±0.01	±1	µA
I_{SW}	Switch Leakage Current	V_{RUN} = 0V, V_{SW} = 0V or 5.5V, V_{IN} = 5.5V			±0.01	±1	µA
I_{FB}	V_{FB} Pin Current	LTC3620, V_{FB} = 0.6V LTC3620-1, V_{FB} = 1.1V			0 1.2	±30 2.0	nA µA
V_{UVLO}	Undervoltage Lockout (UVLO)	V_{IN} Decreasing		2.7	2.8	2.9	V
V_{LOBATB}	LOBATB Threshold Voltage	V_{IN} Decreasing		2.93	3.0	3.08	V
R_{LOBATB}	LOBATB Pull-Down On-Resistance				15		Ω
$V_{HLOBATB}$	LOBATB Hysteresis Voltage				100		mV
R_{PFET}	$R_{DS(ON)}$ of P-channel FET (Note 4)	I_{SW} = 50mA, V_{IN} = 3.6V			2.0		Ω
R_{NFET}	$R_{DS(ON)}$ of N-channel FET (Note 4)	I_{SW} = –50mA, V_{IN} = 3.6V			1.0		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3620 is tested under pulsed load conditions such that $T_J \approx T_A$. LTC3620E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

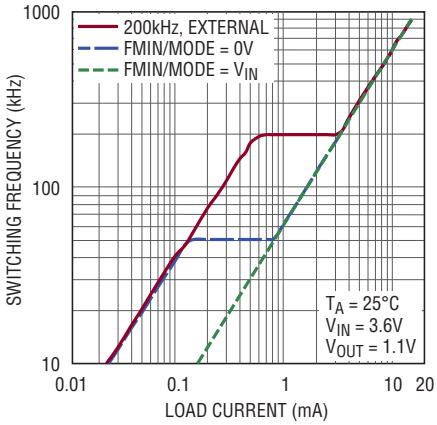
$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: The LTC3620 is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier.

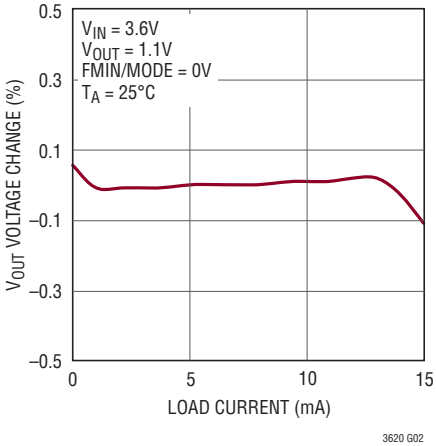
Note 4: The DFN switch-on resistance is guaranteed by correlation to wafer level measurements.

TYPICAL PERFORMANCE CHARACTERISTICS

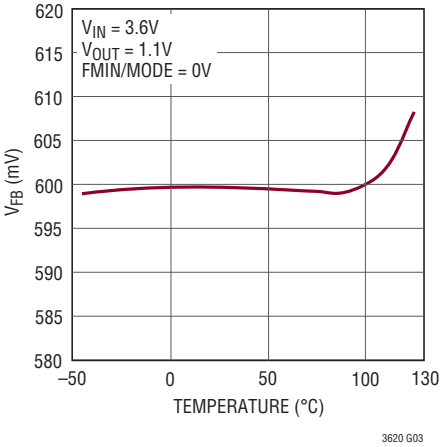
Switching Frequency vs Load Current, FMIN/MODE



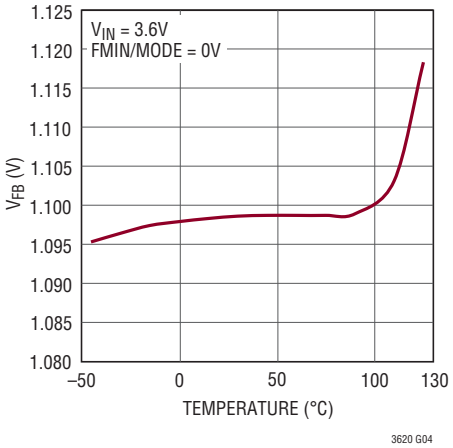
Load Regulation



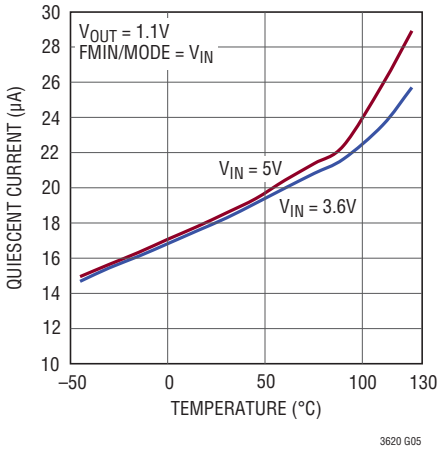
LTC3620 Feedback Voltage vs Temperature



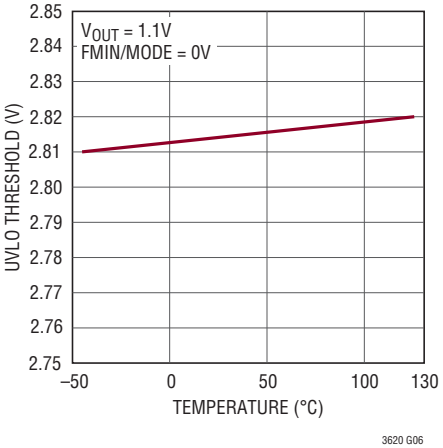
LTC3620-1 Feedback Voltage vs Temperature



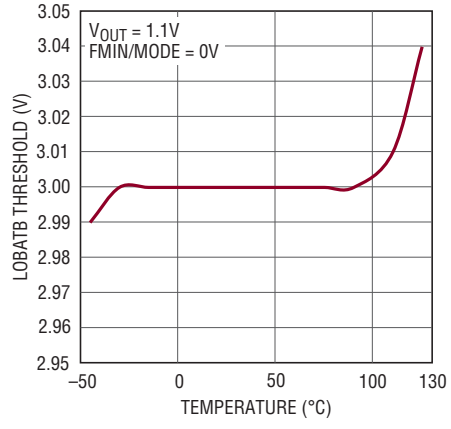
Quiescent Current vs Temperature



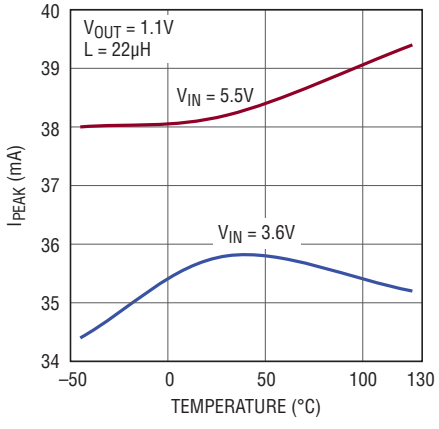
UVLO Threshold vs Temperature



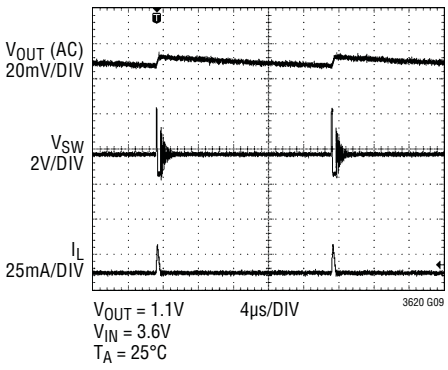
LOBATB Threshold vs Temperature



Peak Inductor Current vs Temperature

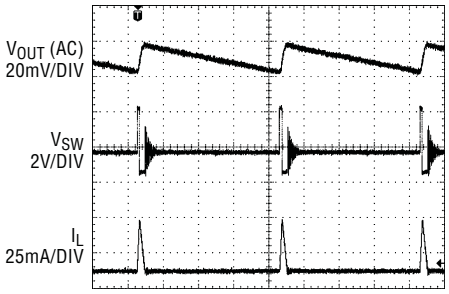


Switching Waveforms at 250µA Load, FMIN/MODE = 0V

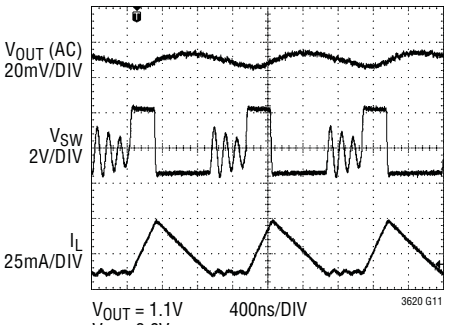


TYPICAL PERFORMANCE CHARACTERISTICS

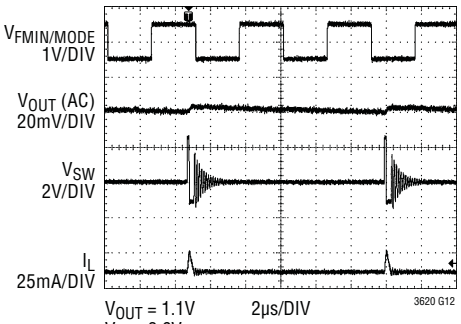
Switching Waveforms at 1mA Load, FMIN/MODE = 0V



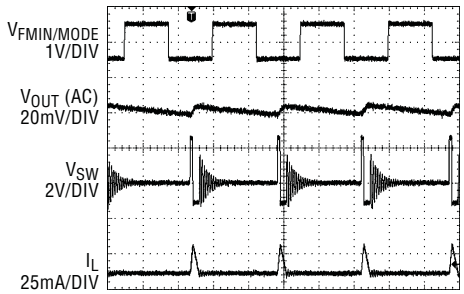
Switching Waveforms at 12mA Load, FMIN/MODE = 0V



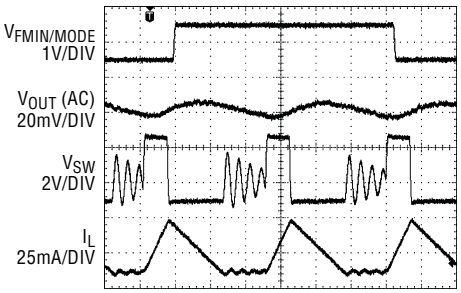
Switching Waveforms at 250µA Load, FMIN/MODE = 200kHz Clock



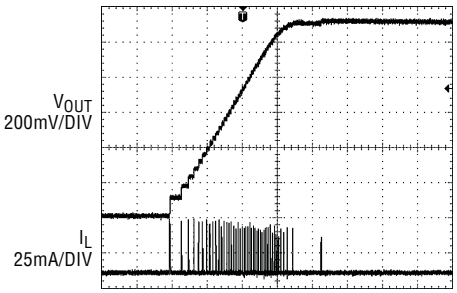
Switching Waveforms at 1mA Load, FMIN/MODE = 200kHz Clock



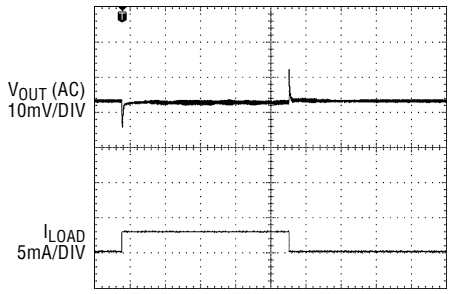
Switching Waveforms at 12mA Load, FMIN/MODE = 200kHz



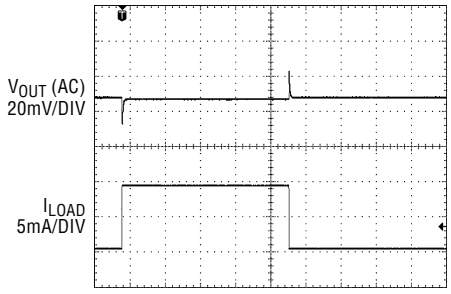
Start-Up Waveforms



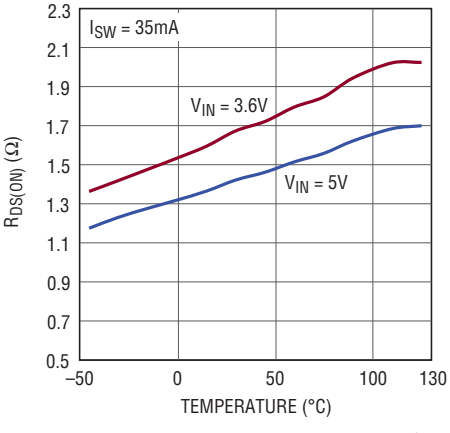
Transient Response, 250µA to 3mA Step, FMIN/MODE = 0V



Transient Response, 1mA to 10mA Step, FMIN/MODE = 0V

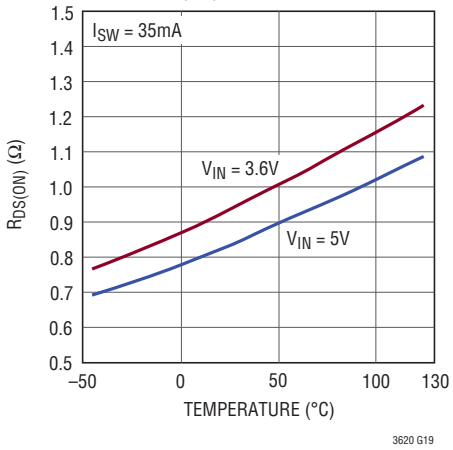


PFET $R_{DS(ON)}$ vs Temperature

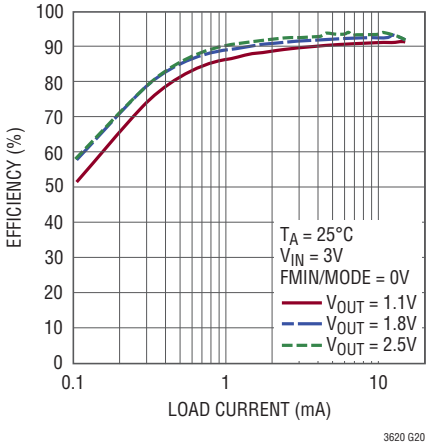


TYPICAL PERFORMANCE CHARACTERISTICS

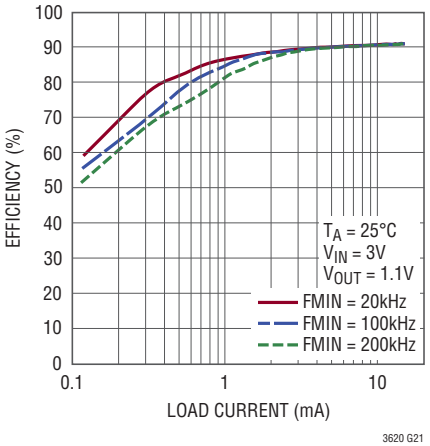
NFET $R_{DS(ON)}$ vs Temperature



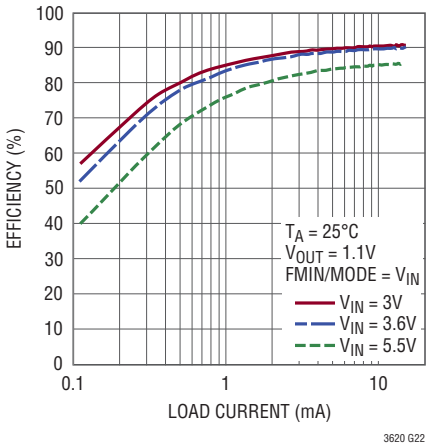
Efficiency vs Load Current, V_{OUT}



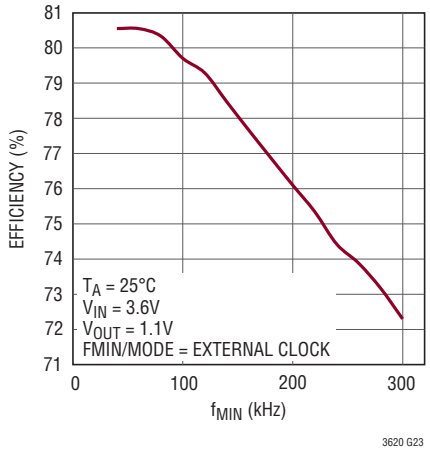
Efficiency vs Load Current, FMIN/MODE Frequency



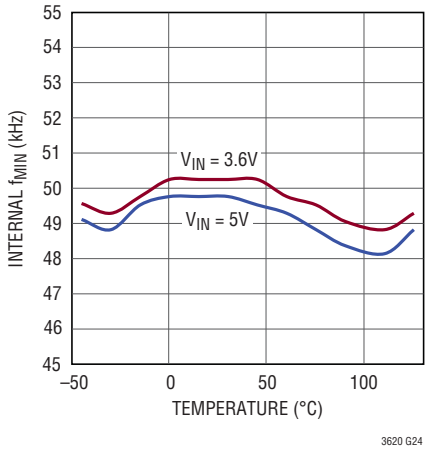
Efficiency vs Load Current, V_{IN}



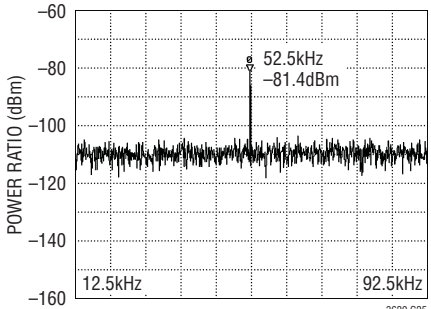
Efficiency vs f_{MIN}, 1mA Load



Internal f_{MIN} vs Temperature

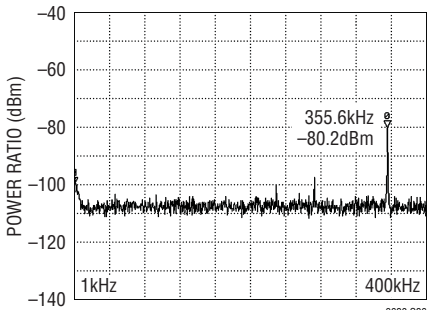


Spectral Content, 500µA Load



VOUT = 1.1V 8kHz/DIV
VIN = 3.6V
FMIN/MODE = 0V
TA = 25°C

Spectral Content, 5mA Load



VOUT = 1.1V 39.9kHz/DIV
VIN = 3.6V
FMIN/MODE = 0V
TA = 25°C

PIN FUNCTIONS

SW (Pin 1): Switch Node Connection to Inductor. This pin connects to the internal power MOSFET Switches.

GND (Pin 2): Ground Connection for Internal Circuitry and Power Path Return. Tie directly to local ground plane.

FMIN/MODE (Pin 3): Frequency Clamp Select Input. Driving this pin with a 20kHz to 300kHz external clock sets the minimum switching frequency. Pulling this pin low sets the minimum switching frequency to the internally set 50kHz. Pulling this pin high defeats the minimum switching frequency and allows the part to switch at arbitrarily low frequencies dependent on the load current.

LOBATB (Pin 4): Low-Battery Status Output. This open-drain output pulls low when V_{IN} falls below 3V.

NC (Pin 5): No Connect.

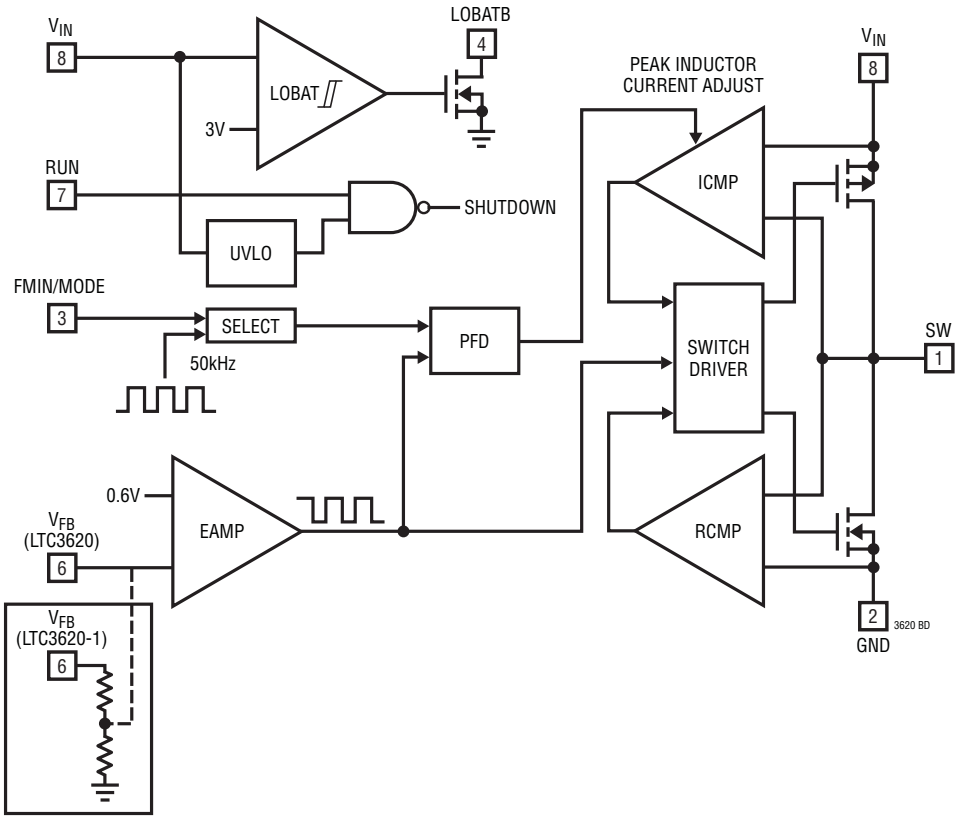
V_{FB} (Pin 6): Regulator Feedback Pin. This pin receives the feedback voltage from the resistive divider across the output. For the LTC3620-1, this pin must be connected directly to V_{OUT}. V_{OUT} is internally divided from V_{OUT} to the reference voltage of 0.6V as seen in the Block Diagram.

RUN (Pin 7): Regulator Enable Pin. Apply a voltage greater than 0.8V to enable the regulator. Do not float this pin.

V_{IN} (Pin 8): Input Supply Pin. Must be locally bypassed.

GND (Exposed Pad Pin 9): Ground. Must be soldered to PCB.

BLOCK DIAGRAM



OPERATION

The LTC3620 is a variable frequency buck switching regulator with a maximum output current of 15mA. At high loads the LTC3620 will supply constant peak current pulses through the output inductor at a frequency dependent on the load current.

A switching cycle is initiated by a pulse from the error amplifier, EAMP. The top FET is turned on and remains on until the peak current threshold is sensed by ICMP (35mA at full loads). When this occurs, the top FET it is turned off and the bottom FET is turned on. The bottom FET remains on until the inductor current drops to 0A, as sensed by the reverse-current comparator, RCMP. The time interval before another switching cycle is initiated is adjusted based on the output voltage error, measured by the EAMP to be the difference between V_{FB} and the 0.6V reference.

As the load current decreases, the EAMP will decrease the switching frequency to match the load, until the minimum switching frequency (internally or externally set) is reached. With the FMIN/MODE pin pulled low, the minimum frequency is internally set to 50kHz. Further decreasing the load will cause the phase frequency detector (PFD) to decrease the peak inductor current in order to maintain the switching frequency at 50kHz.

The minimum switching frequency can be externally set by clocking the FMIN/MODE pin at the desired minimum switching frequency. The load current below which the switching frequency will be clamped is dependent on the externally set frequency and the value of the inductor used. A higher externally set minimum frequency will result in a higher load current threshold below which the part will lock to this minimum frequency. The relationship between load current and minimum frequency is described by the following equation:

$$I_{MAX(LOCK)} = \frac{(V_{IN})(f_{MIN})(L)(35mA)^2}{2V_{OUT}(V_{IN} - V_{OUT})}$$

The LTC3620 will switch at this externally set frequency at load currents below this threshold; though in general, neither this minimum nor this synchronization will be maintained during load transients.

At very light loads, the minimum PFET on time will be reached and the peak inductor current can no longer be reduced. In this situation, the LTC3620 will resume decreasing the regulator switching frequency to prevent the output voltage from climbing uncontrollably.

For those applications which are not sensitive to the spectral content of the output ripple, the minimum frequency clamp can be defeated by pulling the FMIN/MODE pin high. In this mode the inductor current peaks will be held at 35mA and the switching frequency will decrease without limit.

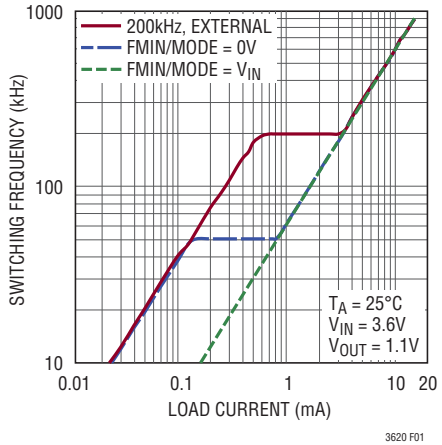


Figure 1. Switching Frequency vs Load Current, FMIN/MODE

APPLICATIONS INFORMATION

Choosing an Inductor

There are a number of different values, sizes and brands of inductors that will work well with this part. Table 1 has a number of recommended inductors, though there are many other manufacturers and devices that may also be suitable. Consult each manufacturer for more detailed information and for their entire selection of related parts.

Table 1: Representative Surface Mount Inductors

VENDOR	PART NUMBER	VALUE (µH)	DCR (Ω)	MAX DC CURRENT (mA)	W × L × H (mm^3)
Taiyo Yuden	CBMF1608T	22 ±10%	1.3 Max	70	0.8 × 1.6 × 0.8
Murata	LQH2MC_02	18 ±20% 22 ±20%	1.8 ±30% 2.1 ±30%	190 185	1.6 × 2 × 0.9
Würth Electronics	744028220	22 ±30%	1.48 Max	270	2.8 × 2.8 × 1.1
Coilcraft	LPS3010	18 ±20% 22 ±20%	1.0 Max 1.2 Max	380 320	2.95 × 2.95 × 0.9

There is a trade-off between physical size and efficiency; The inductors in Table 1 are shown because of their small footprints, choose larger sized inductors with less core loss and lower DCR to maximize efficiency.

The ideal inductor value will vary depending on which characteristics are most critical to the designer. Use the equations and recommendations in the next sections to help you find the correct inductance value for your design.

Avoiding Audio Range Switching

In order to best avoid switching in the audio range at the lowest possible load current, the minimum frequency should be set as low as is acceptable, and the inductor value should be minimized. For a 1.1V output the smallest recommended inductor value is 15µH.

Adjusting for V_{OUT}

The inductor current peak and zero crossing are dependent on the dI/dt. The equations for the rising and falling slopes are as follows:

Rising $dI/dt = (V_{IN}-V_{OUT})/L$

Falling $dI/dt = V_{OUT}/L$

The part is optimized to get 35mA peaks for V_{IN} = 3.6V and V_{OUT} = 1.1V with an 18µH inductor. If the falling slope is too steep the NFET will continue to conduct shortly after the inductor current reaches zero, causing a small reverse current. This means the net power delivered with every pulse will decrease. To mitigate this problem the inductor can be resized. Table 2 shows recommended inductors and output capacitors for commonly used output voltages.

Table 2. Recommended Inductor and Output Capacitor Sizes for Different V_{OUT}

V_{OUT} (V)	L (µH)	C_{OUT} (µF)
0.9	15	2.2
1.1	22	1
1.1 (LTC3620-1)	22	2.2
1.8	33	2.2
2.5	47	4.7

Because the rising dI/dt decreases for increased V_{OUT} and increased L, the inductor current peaks will decrease, causing the maximum load current to decrease as well. Figure 2 shows typical maximum load current versus output voltage.

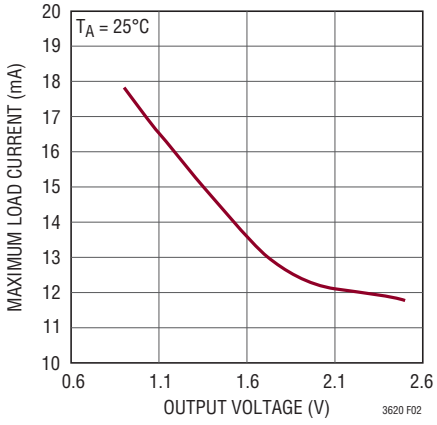


Figure 2. Maximum Output Current vs V_{OUT}, V_{IN} = 3.6V

Output Voltage Ripple

The quantity of charge transferred from V_{IN} to V_{OUT} per switching cycle is directly proportional to the inductor value. Consequently, the output voltage ripple is directly proportional to the inductor value, and the switching frequency for a given load is inversely proportional to the inductor value. For a given load current, higher switching frequency will typically lower the efficiency because of the

APPLICATIONS INFORMATION

increase in switching losses internal to the part. This can be partially offset by using inductors with lower loss.

The peak-to-peak output voltage ripple can be approximated by:

$$\Delta V = \frac{\left(I_{PK}^{2}\right)(L)(V_{IN})}{2(C_{OUT})(V_{OUT})(V_{IN} - V_{OUT})}$$

The output ripple is a strong function of the peak inductor current, I_{PK}. When the LTC3620 is locked to the minimum switching frequency, I_{PK} is decreased to maintain regulation. Consequently, ΔV_{OUT} is reduced in and below the lock range.

Efficiency

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in the LTC3620's circuits: V_{IN} quiescent current and I^2R losses. V_{IN} quiescent current loss dominates the efficiency loss at low load currents, whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of little consequence, as illustrated on the front page of this data sheet.

The quiescent current is due to two components: the DC bias current, I_Q, as given in the Electrical Characteristics, and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current and proportional to frequency. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. The I^2R losses per pulse will be proportional to the peak current squared times the sum of the switch resistance and the inductor resistance:

$$I^2R\frac{Loss}{Pulse} = \frac{I_{PK}^{2}}{3}R_{EFF}$$

where $R_{EFF} = R_L + R_{PFET}\,D + R_{NFET}\,(1 - D)$, and D is the ratio of the top switch on-time to the total time of the pulse. Additional losses incurred from the inductor DC resistance and core loss may be significant in smaller inductors.

Capacitor Selection

Higher value, lower cost, ceramic capacitors are now widely available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3620's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

The output voltage ripple is inversely proportional to the output capacitor. The larger the capacitor, the smaller the ripple, and vice versa. However, the transient response time is directly proportional to C_{OUT}, so a larger C_{OUT} means slower response time.

To maintain stability and an acceptable output voltage ripple, values for C_{OUT} should range from 1µF to 5µF.

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Setting Output Voltage

The output voltage is set by tying V_{FB} to a resistive divider using the following formula (refer to Figure 3):

$$V_{OUT} = \frac{0.6V(R1+R2)}{R2}$$

R1 and R2 should be large to minimize standing load current and improve efficiency.

The fixed output version, the LTC3620-1, includes an internal resistive divider, eliminating the need for external resistors. The resistor divider is chosen such that the V_{FB} input current is approximately 1µA. For this version, the V_{FB} pin should be connected directly to V_{OUT}.

Maximum Load Current and Maximum Frequency

The maximum current that the LTC3620 can provide is calculated to be just slightly less than half the maximum peak current.

The inductor value will determine how much energy is delivered to the output for each switching cycle, and thus the duration of each pulse and the maximum frequency. Larger inductors will have slower ramp rates, longer pulses, and thus lower maximum frequencies. Conversely, smaller inductors will result in higher maximum frequencies.

When using a frequency clamp, large abrupt increasing load steps from levels below the locking range to levels near the maximum output may result in a large drop in the output voltage. This is due to the low bandwidth of the frequency clamp loop in returning the peak inductor current to its maximum.

Thermal Considerations

The LTC3620 requires the package backplane metal to be soldered to the PC board. This gives the DFN package exceptional thermal properties, making it difficult in normal operation to exceed the maximum junction temperature of the part. In most applications the LTC3620 does not dissipate much heat due to its high efficiency and low current. In applications where the LTC3620 is running at high ambient temperatures and high load currents, the heat dissipated may exceed the maximum junction temperature of the part if it is not well thermally grounded.

Design Example

This example designs a 1.1V output using a Li-Ion battery input with voltages between 2.8V to 4.2V, and an average of 3.6V. The internally provided 50kHz clock will be used for the minimum switching frequency, so the FMIN/MODE pin will be pulled low. For a 1.1V output, an 18µH inductor should be used (refer to Table 2).

C_{OUT} can be chosen from Table 2 or can be based on a desired maximum output voltage ripple, ΔV_{OUT}. For this case let's use a maximum ΔV_{OUT} equal to 1% of V_{OUT}, or 11mV.

$$C_{OUT} = \frac{\left(35mA^2\right)(22\mu H)(3.6V)}{2\Delta V_{OUT}(1.1V)(3.6V-1.1V)} = 1.6\mu F \approx 1.5\mu F$$

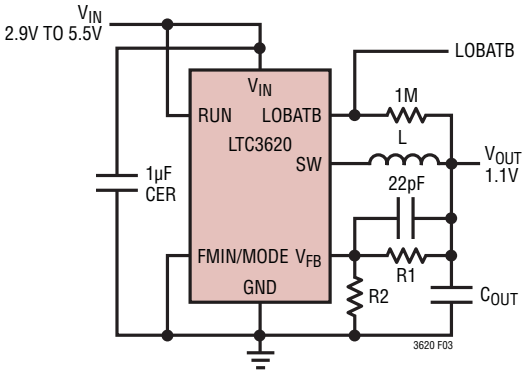


Figure 3. Design Example Schematic

APPLICATIONS INFORMATION

A larger capacitor could be used to reduce this number. Keep in mind that while a larger output capacitor will decrease voltage ripple, it will also increase the transient settling time. The optimal range for C_{OUT} should be between 1µF and 5µF.

The best way to select the feedback resistors is to select a target combined resistance, and try different standard 1% resistor sizes to see which combination will give the least error. For this example a target combined resistance of around 1M will be used. By checking R1 values between 422k and 475k, and calculating R2 using the formula:

$$R2 = \frac{(0.6V)R1}{V_{OUT} - 0.6V}$$

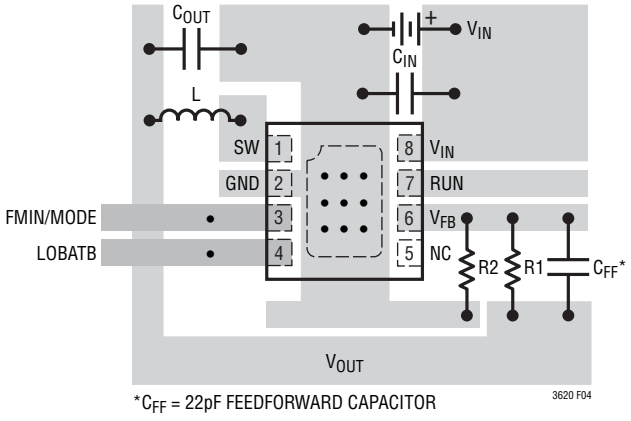
it can be found that a value of R2 = 523k and R1 = 432k minimizes the error in this range.

The error can be checked by solving for V_{OUT} and finding the percent error from the desired 1.1V. Using these resistor values will result in V_{OUT} = 1.096V, and an error of around 0.4%. Using different target resistor sums is acceptable, but a smaller sum will decrease efficiency at lower loads, and a larger sum will increase noise sensitivity at the V_{FB} pin.

Board Layout Checklist

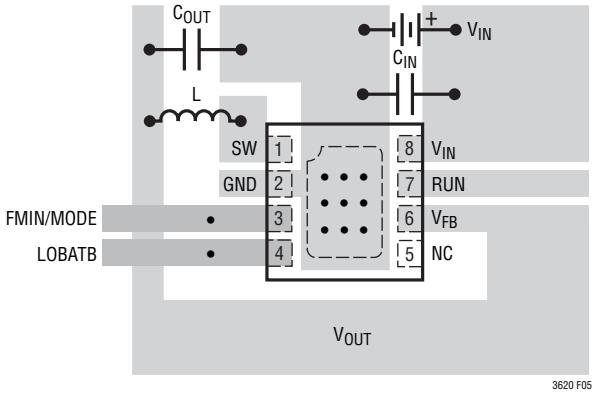
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3620:

1. The power traces consisting of GND, SW and V_{IN} should be kept short, direct and wide.
2. The V_{FB} pin should connect directly to the respective feedback resistors, which should also have short, direct paths to V_{OUT} and GND respectively.
3. Keep C_{OUT} and C_{IN} as close to the LTC3620 as possible.
4. All parts connecting to ground should have their ground terminals in close proximity to the LTC3620 GND connection.
5. Keep the SW node and external clock, if used, away from the sensitive V_{FB} node. Also, minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.



*C_{FF} = 22pF FEEDFORWARD CAPACITOR

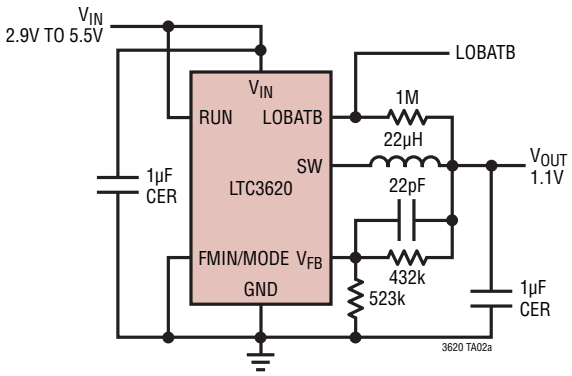
LTC3620 Layout Diagram



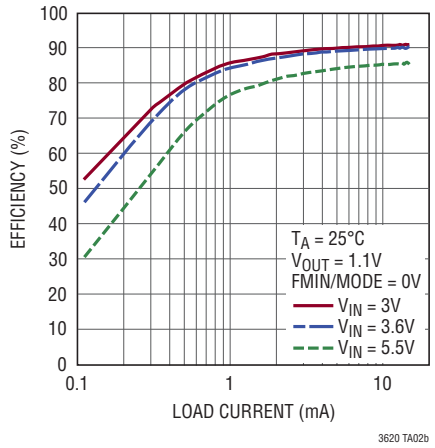
LTC3620-1 Layout Diagram

TYPICAL APPLICATIONS

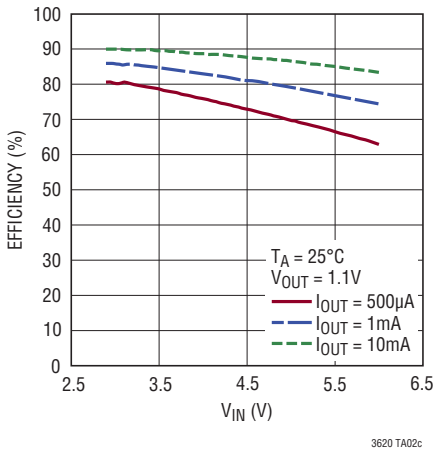
High Efficiency Low Power Step-Down Converter, FMIN/MODE = 0



Efficiency vs Load Current

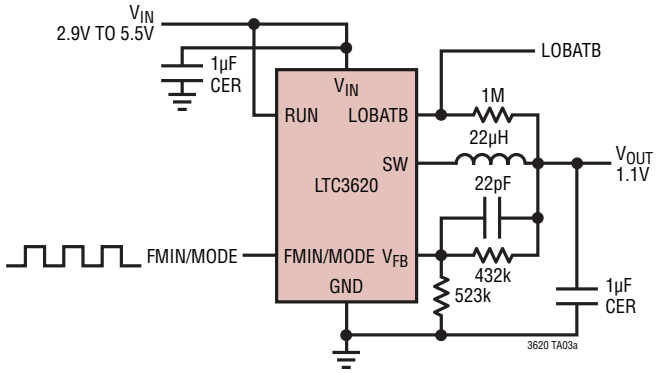


Efficiency vs V_{IN}

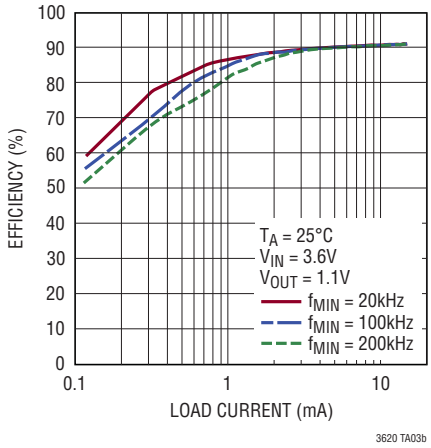


TYPICAL APPLICATIONS

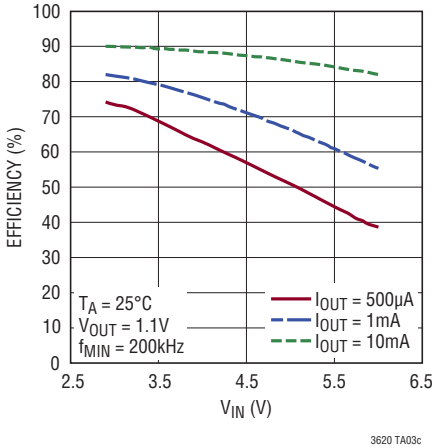
High Efficiency Low Power Step-Down Converter, Externally Programmed f_{MIN}



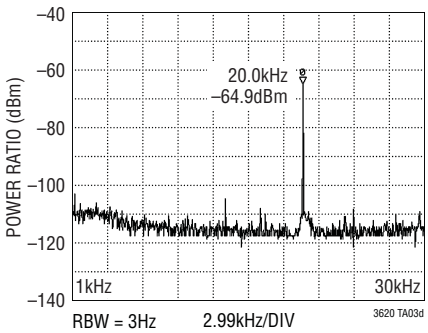
Efficiency vs Load Current



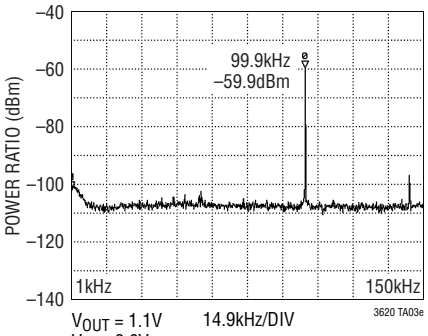
Efficiency vs V_{IN}



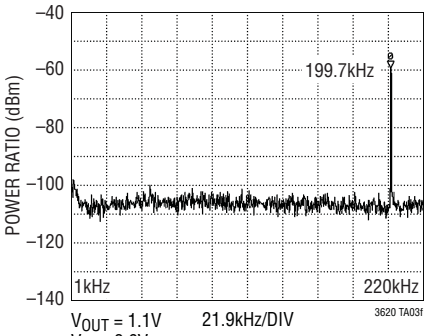
Spectral Content, FMIN/MODE = 20kHz Clock



Spectral Content, FMIN/MODE = 100kHz Clock

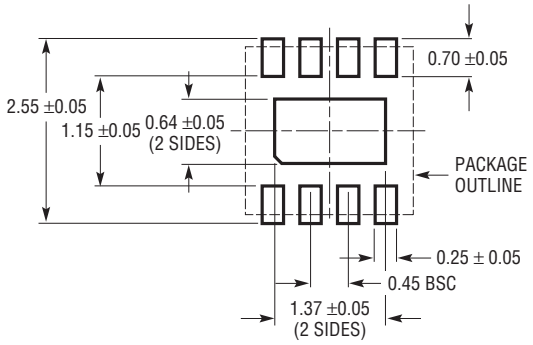


Spectral Content, FMIN/MODE = 200kHz Clock

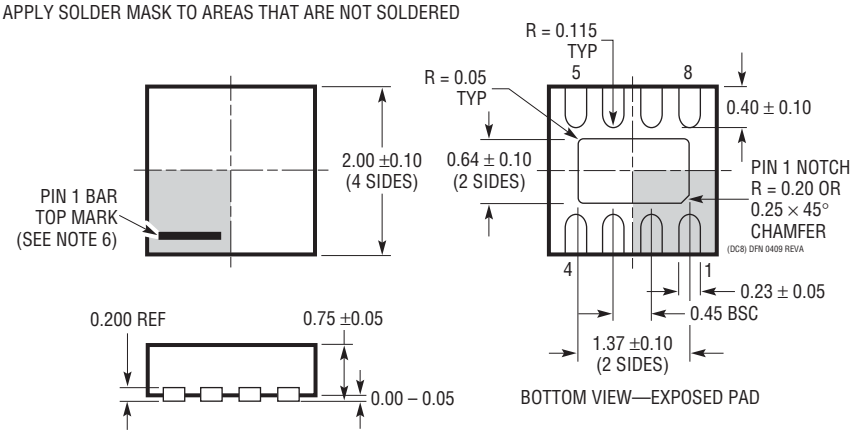


PACKAGE DESCRIPTION

DC Package
8-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1719 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

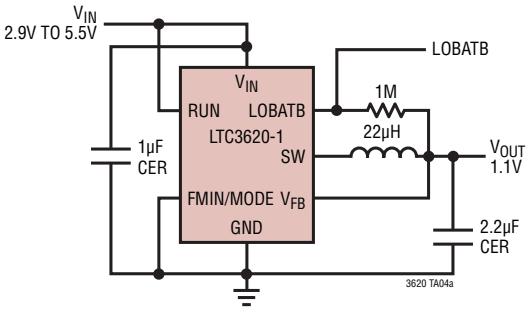
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

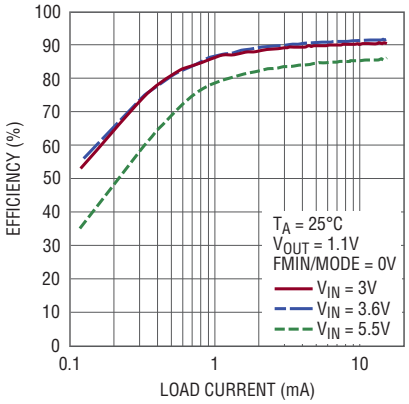
REV	DATE	DESCRIPTION	PAGE NUMBER
A	8/10	Added (Note 2) to Electrical Characteristics header	2, 3
		$V_{LOADREG}$ value of 0.5% moved from TYP to MAX	2
		Note 2 updated, Note 4 deleted and note numbers corrected	3
		V_{SW} value updated on graph G10	5
		Pin 9 text updated in Pin Functions section	7

TYPICAL APPLICATIONS

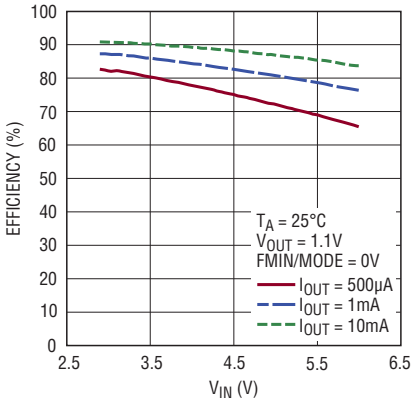
High Efficiency Low Power Step-Down Converter, LTC3620-1 Internally Programmed, 1.1V_{OUT}



Efficiency vs Load Current



Efficiency vs V_{IN}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3631/LTC3631-3.3/ LTC3631-5	45V, 100mA (I_{OUT}), Ultralow Quiescent Current Synchronous Step-Down DC/DC Converter	V_{IN}: 4.5V to 45V (60V_{MAX}), $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 1µA, 3mm × 3mm DFN Package, MSOP-8E
LTC3632	50V, 20mA (I_{OUT}), Ultralow Quiescent Current Synchronous Step-Down DC/DC Converter	V_{IN}: 4.5V to 50V (60V_{MAX}), $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 1µA, 3mm × 3mm DFN Package, MSOP-8E
LTC3642/LTC3642-3.3/ LTC3642-5	45V, 50mA (I_{OUT}), Ultralow Quiescent Current Synchronous Step-Down DC/DC Converter	V_{IN}: 4.5V to 45V (60V_{MAX}), $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 1µA, 3mm × 3mm DFN Package, MSOP-8E
LTC3405A/LTC3405AB	300mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3406A/LTC3406AB	600mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3407A/LTC3407A-2	Dual 600mA/800mA I_{OUT}, 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E, DFN Packages
LTC3409	600mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65µA, I_{SD} < 1µA, DFN Package
LTC3410/LTC3410B	300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA, I_{SD} < 1µA, SC70 Package
LTC3411A	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS10, DFN Packages
LTC3548	Dual 400mA/800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10, DFN Packages
LTC3561A	1A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 240µA, I_{SD} < 1µA, 3mm × 3mm DFN Package

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