GaAs, pHEMT, MMIC, 1 W, Power Amplifier with Power Detector, 37 GHz to 40 GHz

Data Sheet **HMC7229LS6**

FEATURES

- 32 dBm typical saturated output power (P_{SAT}) at 18% power added efficiency (PAE) at 39 GHz
- P1dB compression output power: 31.5 dBm typical
- High output third-order intercept (IP3): 40 dBm typical
- High gain: 24 dB typical
- 50 Ω matched input/output
- Ceramic, 6 mm × 6 mm, high frequency, air cavity package

APPLICATIONS

- Point to point radios
- Point to multipoint radios
- Very small aperture terminal (VSAT) and satellite communications (SATCOM)

FUNCTIONAL BLOCK DIAGRAM

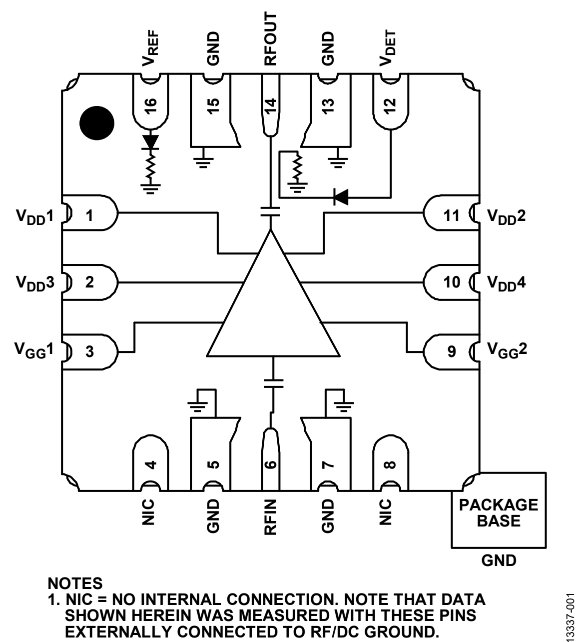

Figure 1.

GENERAL DESCRIPTION

The HMC7229LS6 is a four stage, gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), 1 W power amplifier, with an integrated temperature compensated on-chip power detector that operates between 37 GHz to 40 GHz. The HMC7229LS6 provides 24 dB of gain and 32 dBm of saturated output power at 18% PAE at 39 GHz from a 6 V supply. With an excellent IP3 of 40 dBm, the HMC7229LS6 is ideal for linear applications such as high capacity, point to point or multipoint radios or VSAT/SATCOM applications demanding 32 dBm of efficient saturated output power. The radio frequency (RF) input/outputs are internally matched and dc blocked for ease of integration into higher level assemblies. The HMC7229LS6 is housed in a ceramic, 6 mm × 6 mm, high frequency, air cavity package that exhibits low thermal resistance and is compatible with surface-mount manufacturing techniques.

Rev. E Document Feedback

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REVISION HISTORY

8/2020—Rev. D to Rev. E

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12/2017—Rev. C to Rev. D

Changes to Figure 33 ... 11

9/2017—Rev. B to Rev. C

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Changes to Ordering Guide ... 15

6/2016—Rev. v01.0514 to Rev. B

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.
Updated Format ... Universal
Changes to General Description Section ... 1
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Added Theory of Operation Section ... 11
Added Applications Information Section and Recommended Bias Sequence Section ... 12
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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, $V_{DD}1$ to $V_{DD}4$ ($V_{DD}x$) = 6 V, I_{DD} = 1200 mA (adjust $V_{GG}1$/$V_{GG}2$, $V_{GG}x$, between −2 V to 0 V to achieve an I_{DD} = 1200 mA typical), unless otherwise stated.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		37		40	GHz
GAIN		21	24		dB
Gain Variation over Temperature			0.058		dB/°C
RETURN LOSS					
Input			16		dB
Output			14		dB
OUTPUT POWER					
For P1dB Compression		28.5	31.5		dBm
Saturated (P_{SAT})	With 18% PAE at 39 GHz		32		dBm
OUTPUT THIRD-ORDER INTERCEPT (IP3)	Measurement taken at P_{OUT}/tone = 20 dBm		40		dBm
TOTAL SUPPLY CURRENT (I_{DD})[1]	V_{DD} = 5 V, V_{DD} = 5.5 V, and V_{DD} = 6 V		1200		mA

[1] Adjust $V_{GG}x$ to achieve I_{DD} = 1200 mA.

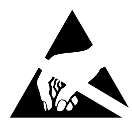
ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (V_{DD}x)	7 V
Minimum Gate Voltage (V_{GG1}, V_{GG2})	−3 V
RF Input Power (RFIN)	21 dBm
Channel Temperature	175°C
Continuous Power Dissipation, P_{DISS} (T = 85°C, Derates 95 mW/°C Above 85°C)	9.0 W
Thermal Resistance (Channel to Ground Paddle)	10°C/W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity (Human Body Model)	Class 0, passed 150 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

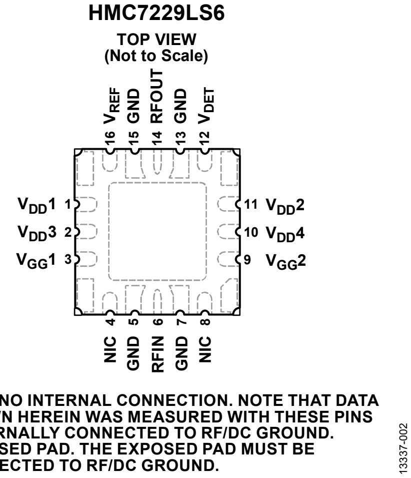


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 10, 11	$V_{DD}1$ to $V_{DD}4$	Drain Bias Voltages. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required for each of these pins. See Figure 3.
3, 9	$V_{GG}1$, $V_{GG}2$	Gate Controls for the Power Amplifier. Adjust $V_{GG}x$ to achieve the recommended bias current. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required for each of these pins. Apply $V_{GG}x$ bias to either Pin 3 or Pin 9. See Figure 4.
4, 8	NIC	No Internal Connection. Note that data shown herein was measured with these pins externally connected to RF/dc ground.
5, 7, 13, 15	GND	Ground Pins. Connect these pins and the exposed ground pad to RF/dc ground. See Figure 5.
6	RFIN	RF Input. This pin is ac-coupled and matched to 50 Ω. See Figure 6.
12	V_{DET}	Detector Voltage. This pin is the dc voltage that represents the RF output power rectified by the diode that is biased through an external resistor. See Figure 8.
14	RFOUT	RF Output. This pin is ac-coupled and matched to 50 Ω. See Figure 9.
16	V_{REF}	Detector Reference Voltage. This pin is the dc voltage of the diode biased through an external resistor used for the temperature compensation of V_{DET}. See Figure 7.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

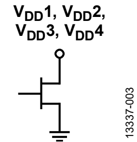


Figure 3. $V_{DD}1$, $V_{DD}2$, $V_{DD}3$, and $V_{DD}4$ Interface Schematic

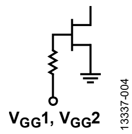


Figure 4. $V_{GG}1$ and $V_{GG}2$ Interface Schematic

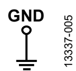


Figure 5. GND Interface Schematic

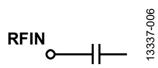


Figure 6. RFIN Interface Schematic

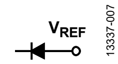


Figure 7. V_{REF} Interface Schematic

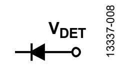


Figure 8. V_{DET} Interface Schematic

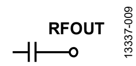


Figure 9. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

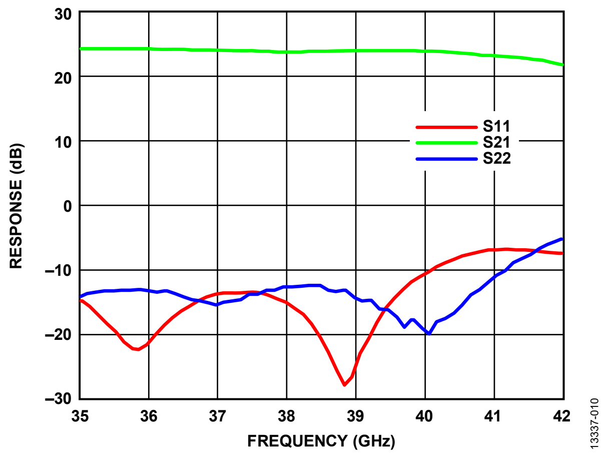


Figure 10. Gain and Return Loss (S11, S21, and S22) vs. Frequency

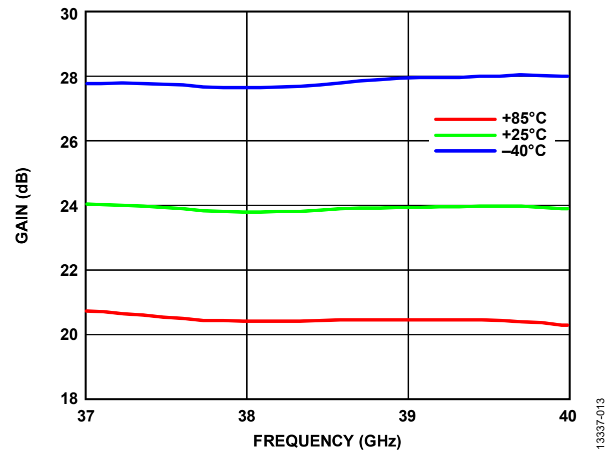


Figure 13. Gain vs. Frequency for Various Temperatures

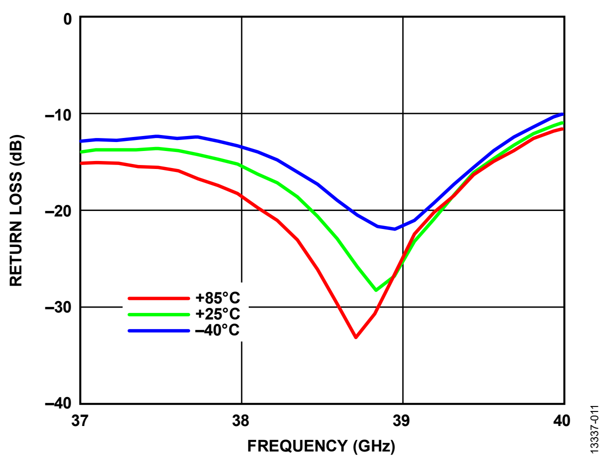


Figure 11. Input Return Loss vs. Frequency for Various Temperatures

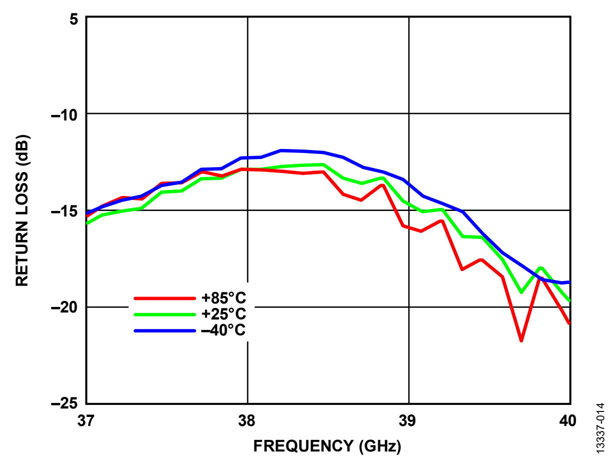


Figure 14. Output Return Loss vs. Frequency for Various Temperatures

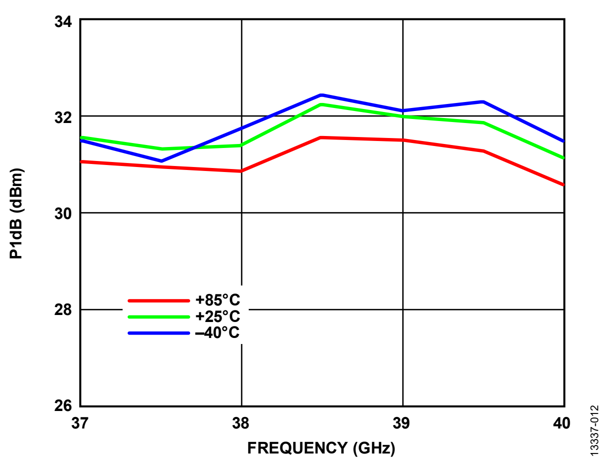


Figure 12. P1dB vs. Frequency for Various Temperatures

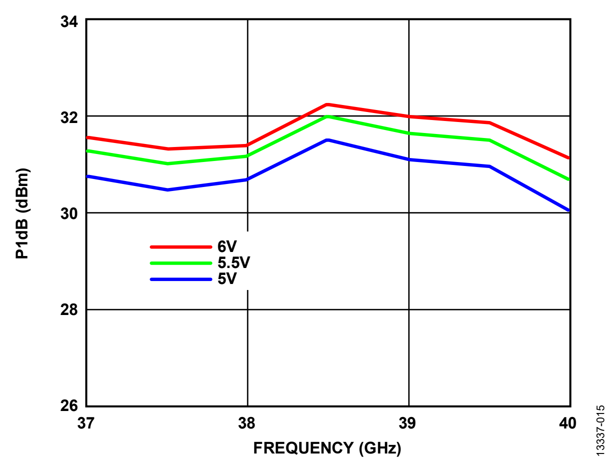


Figure 15. P1dB vs. Frequency for Various Supply Voltages

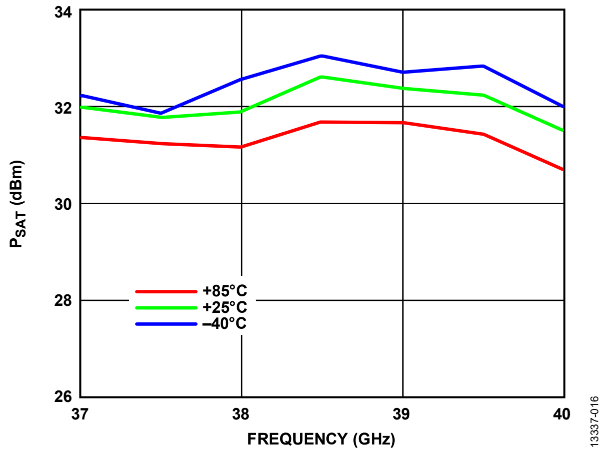


Figure 16. P_{SAT} vs. Frequency for Various Temperatures

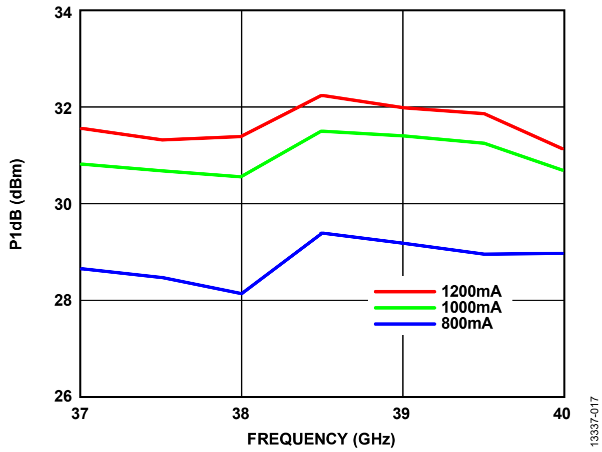


Figure 17. P1dB vs. Frequency for Various Supply Voltages

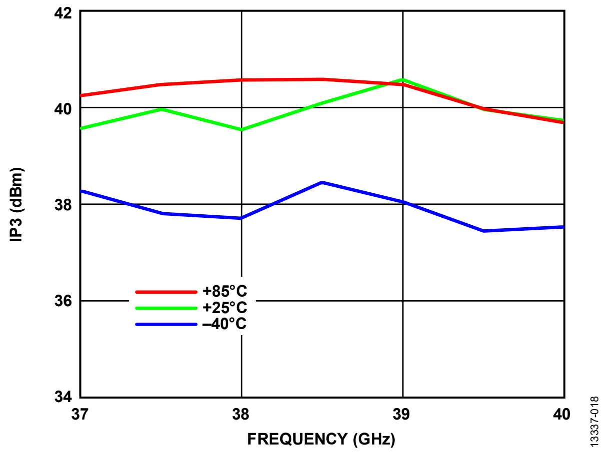


Figure 18. Output IP3 vs. Frequency for Various Temperatures, P_{OUT}/Tone = 20 dBm

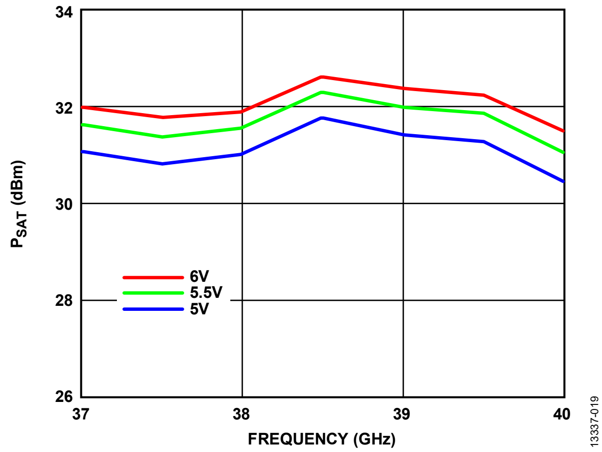


Figure 19. P_{SAT} vs. Frequency for Various Supply Voltages

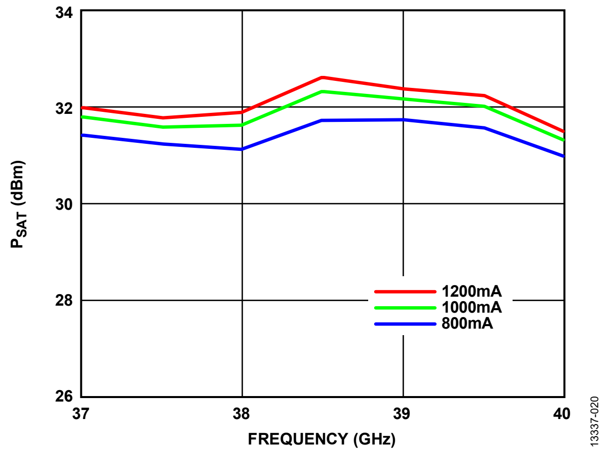


Figure 20. P_{SAT} vs. Frequency for Various Supply Currents

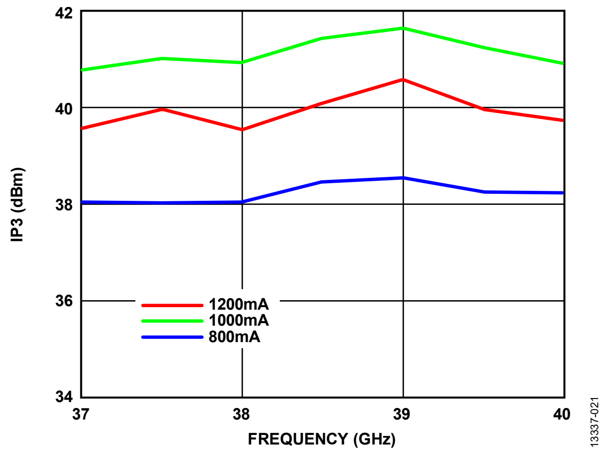


Figure 21. Output IP3 vs. Frequency for Various Supply Currents, P_{OUT}/Tone = 20 dBm

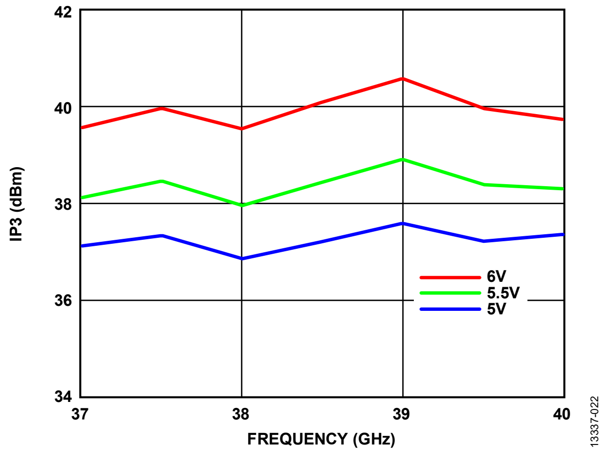


Figure 22. Output IP3 vs. Frequency for Various Supply Voltages P_{OUT}/Tone = 20 dBm

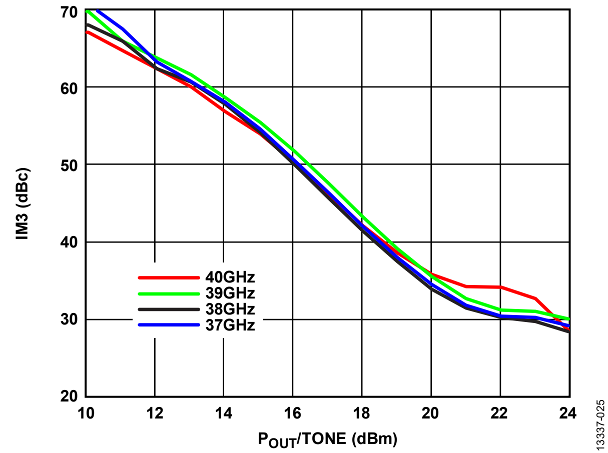


Figure 25. Output IM3 at V_{DD} = 5 V vs. P_{OUT}/Tone

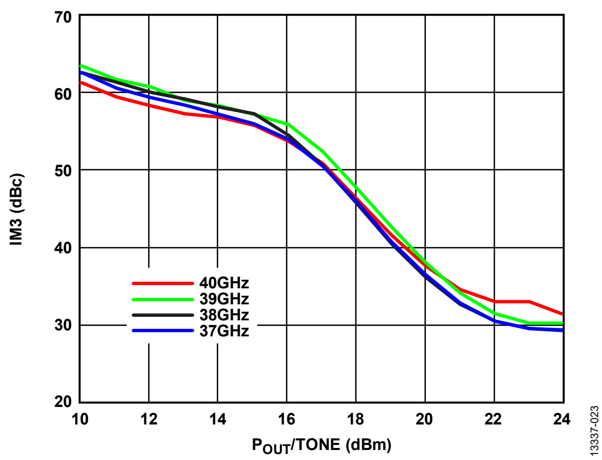


Figure 23. Output IM3 at V_{DD} = 5.5 V vs. P_{OUT}/Tone

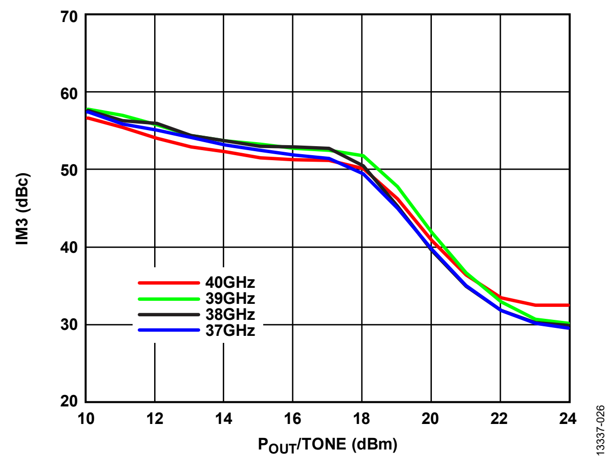


Figure 26. Output IM3 at V_{DD} = 6 V vs. P_{OUT}/Tone

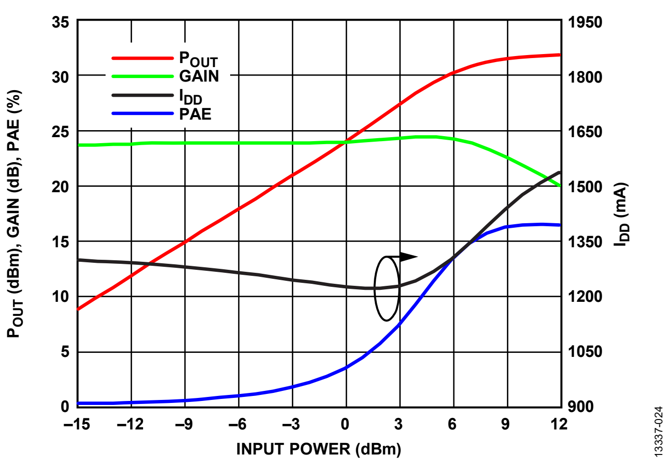


Figure 24. Power Compression (P_{OUT}, Gain, PAE, and I_{DD}) at 38 GHz vs. Input Power

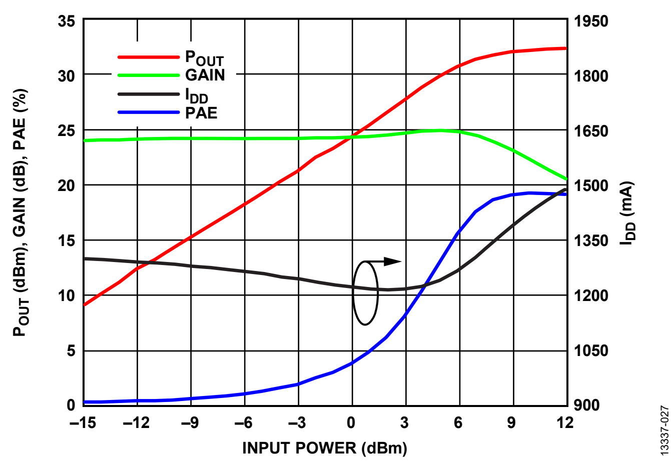


Figure 27. Power Compression (P_{OUT}, Gain, PAE, and I_{DD}) at 39 GHz vs. Input Power

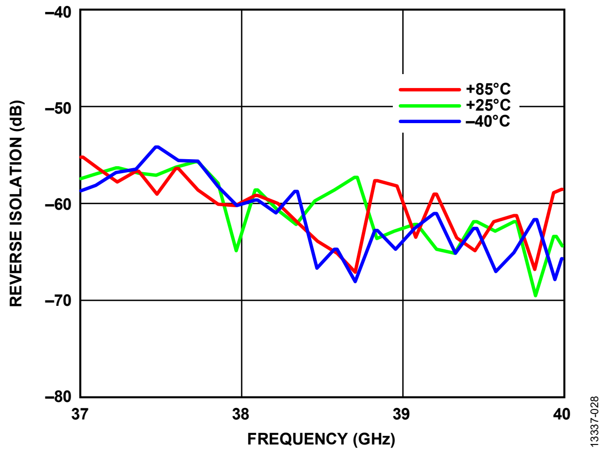


Figure 28. Reverse Isolation vs. Frequency for Various Temperatures

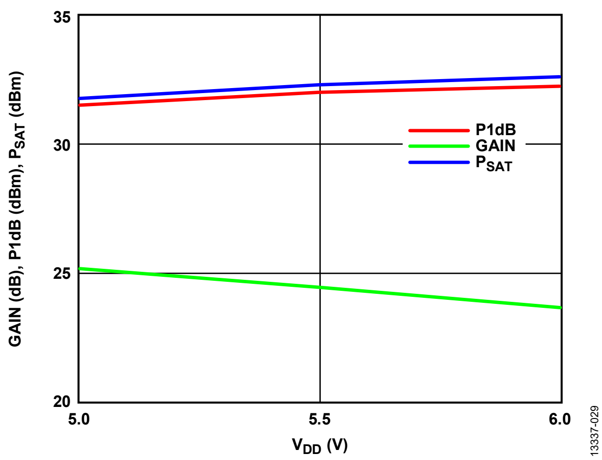


Figure 29. Gain, P1dB, and P_{SAT} vs. Supply Voltage (V_{DD}) at 38.5 GHz

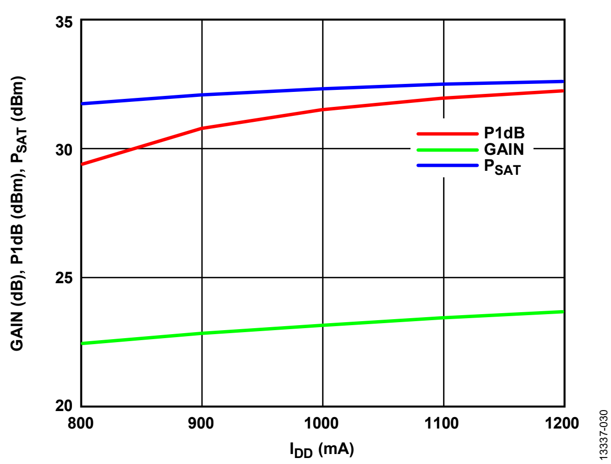


Figure 30. Gain, P1dB, and P_{SAT} vs. Supply Current (I_{DD}) at 38.5 GHz

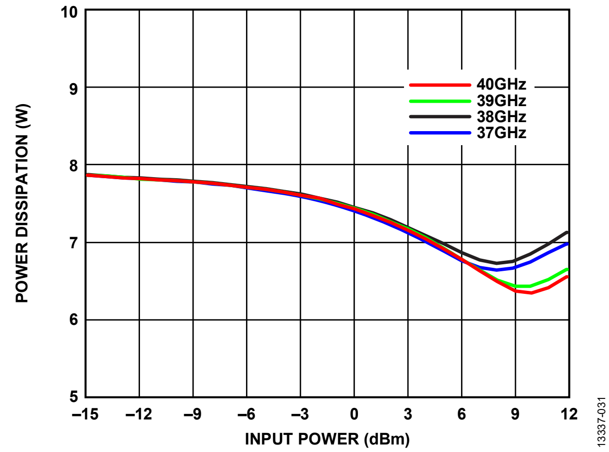


Figure 31. Power Dissipation vs. Input Power

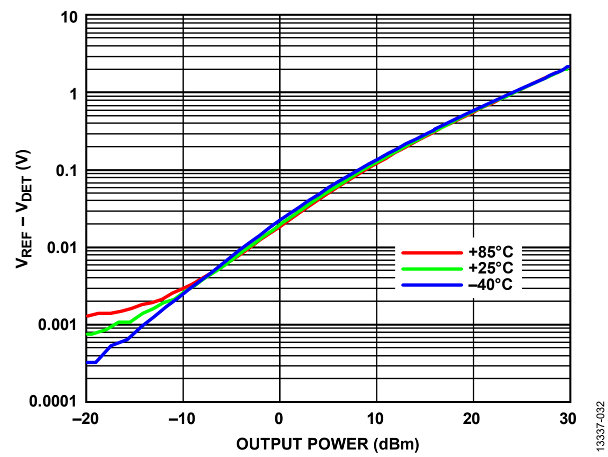


Figure 32. Detector Voltage (V_{REF} – V_{DET}) vs. Output Power for Various Temperatures at 38.5 GHz

THEORY OF OPERATION

The HMC7229LS6 is gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), 1 W power amplifier consisting of four gain stages that are in series. Figure 33 shows the simplified block diagram.

The input signal is divided evenly into two, each of these paths are amplified through four independent gain stages, and the amplified signals are then combined at the output. A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, it rectifies the RF power and makes it available for measurement as a dc voltage at VDET. To allow for temperature compensation of VDET, a identical and symmetrically located circuit, minus the coupled RF power, is available via VREF. Taking the difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output. (See Figure 32.)

The HMC7229LS6 has single-ended input and output ports whose impedances are nominally matched to 50 Ω internally over the 37 GHz to 40 GHz frequency range. Consequently, the HMC7229LS6 can directly insert into a 50 Ω system with no impedance matching circuitry required. In addition, multiple HMC7229LS6 devices can be cascaded back to back without requiring external matching circuitry. Similarly, multiple HMC7229LS6 devices can be used with power dividers at the input and power combiners at the output to obtain higher output power levels.

Because the input and output impedances are sufficiently stable vs. the variations in temperature and supply voltage, no impedance matching compensation is required.

To achieve the best performance and not damage the HMC7229LS6, do not exceed the absolute maximum ratings.

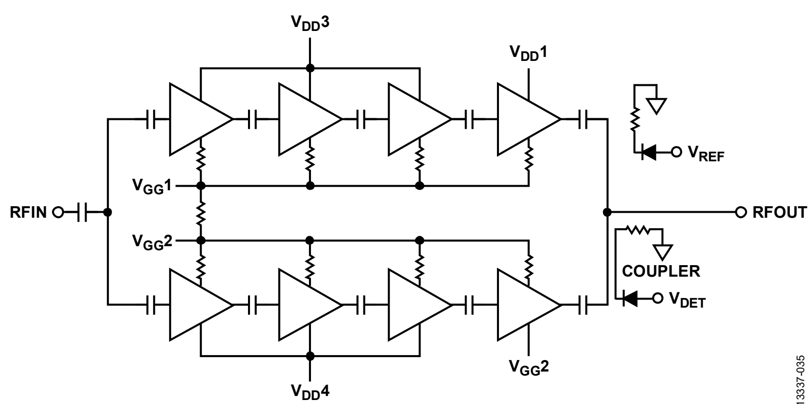


Figure 33. GaAs, pHEMT, 1 W MMIC Power Amplifier Block Diagram

APPLICATIONS INFORMATION

Figure 35 shows the basic connections for operating the HMC7229LS6 and see the Theory of Operation section for additional details. The RF input and RF output are ac-coupled by the internal dc block capacitors. To avoid damaging the HMC7229LS6, follow the recommended bias sequencing during power-up and power-down.

The gate bias of the HMC7229LS6 is supplied by using either the $V_{GG}1$ pin or the $V_{GG}2$ pin. While applying drain bias to the HMC7229LS6, all of the $V_{DD}1$, $V_{DD}2$, $V_{DD}3$, and $V_{DD}4$ pins must be used.

RECOMMENDED BIAS SEQUENCE

During Power-Up

The recommended bias sequence during power-up is the following:

1. Connect the GND pin to ground.
2. Set $V_{GG}x$ to −2 V.
3. Set $V_{DD}x$ to 6 V.
4. Increase $V_{GG}x$ to achieve a typical I_{DD} = 1200 mA.
5. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down is the following:

1. Turn the RF signal off.
2. Decrease $V_{GG}x$ to −2 V to achieve a typical I_{DD} = 0 mA.
3. Decrease $V_{DD}x$ to 0 V.
4. Increase $V_{GG}x$ to 0 V.

The bias conditions previously listed (V_{DDx} = 6 V, I_{DD} = 1200 mA), are the recommended operating point to get optimum performance. The data used in this data sheet was taken with the recommended bias condition. When using the HMC7229LS6 with different bias conditions, different performance may result than what is shown in the Typical Performance Characteristics section.

The V_{DET} and V_{REF} pins are the output pins for the internal power detector. The V_{DET} pin is the dc voltage output pin that represents the RF output power rectified by the internal diode, which is biased through an external resistor.

The V_{REF} pin is the dc voltage output pin that represents the reference diode voltage, which is biased through an external resistor. This voltage then compensates for the temperature variation effects on both diodes. A typical circuit is shown in the Typical Application Circuit section that reads out the output voltage and represents the RF output power shown in Figure 35.

EVALUATION PRINTED CIRCUIT BOARD (PCB)

Use RF circuit design techniques to create the circuit board for this application. Ensure that signal lines have 50 Ω impedance, and connect the package ground leads and exposed paddle directly to the ground plane similar to that shown in Figure 35. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 34 is available from Analog Devices, Inc., upon request.

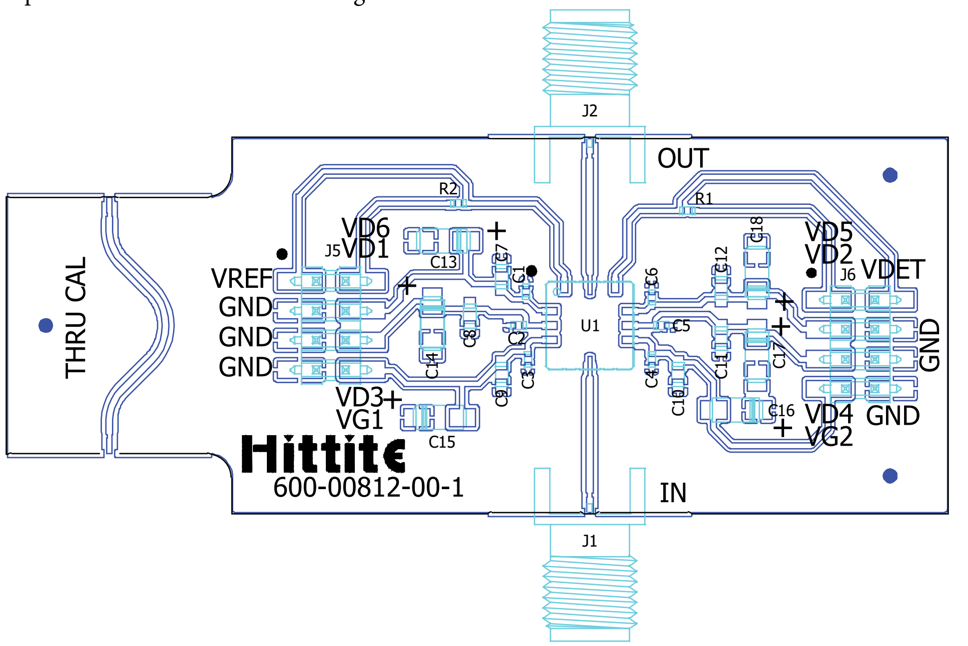


Figure 34. 600-00812-00-1 Evaluation Board PCB

Table 4. List of Materials for Evaluation PCB

Item	Description
J1, J2	K connector, SRI
J5, J6	DC pin
C1 to C6	100 pF capacitors, 0402 package
C7 to C12	10 nF capacitors, 0603 package
C13 to C18	4.7 µF capacitors, Case A package
R1, R2	40.2 kΩ resistors, 0402 package
U1	HMC7229LS6 amplifier
PCB	600-00812-00-1 evaluation board PCB, circuit board material is Rogers 4350 or Arlon 25FR

TYPICAL APPLICATION CIRCUIT

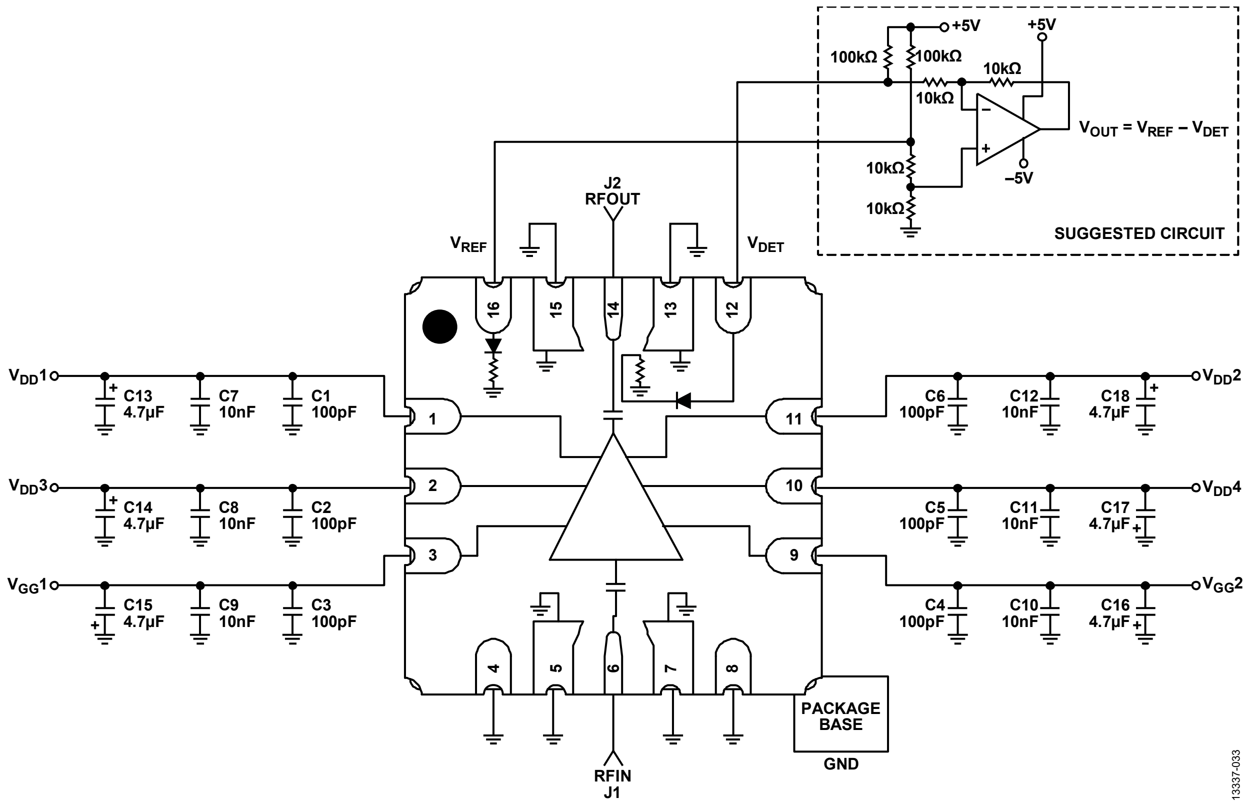


Figure 35. Typical Application Circuit

OUTLINE DIMENSIONS

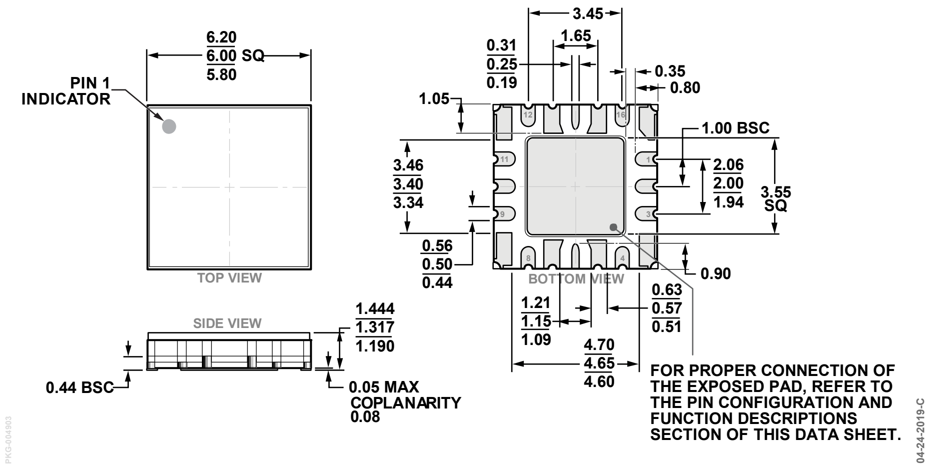


Figure 36. 16-Terminal Ceramic Leadless Chip with Heat Sink [LCC_HS]
(EH-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Package Body Material	Lead Finish	Temperature Range	Package Description	Package Option
HMC7229LS6	Alumina White	Gold over Nickel	−40°C to +85°C	16-Terminal LCC_HS	EH-16-1
HMC7229LS6TR	Alumina White	Gold over Nickel	−40°C to +85°C	16-Terminal LCC_HS	EH-16-1
EVAL01-HMC7229LS6				Evaluation Board	

[1] All Models are RoHS-Compliant.