EVAL-1CH2CHSOICEBZ User Guide
UG-937

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Using the EVAL-1CH2CHSOICEBZ *i*Coupler Standard Data Isolator Evaluation Board

FEATURES

Access to 2 data channels
Multiple connection options
Support for active probes
Provisions for cable terminations
Support for printed circuit board (PCB) edge mounted coaxial connectors
Easy configuration

SUPPORTED *i*Coupler DEVICES

Sample *i*Coupler digital isolators must be ordered separately; supported *i*Coupler devices are as follows:

ADuM110N
ADuM120N/ADuM121N
ADuM210N
ADuM225N/ADuM226N
ADuM7240/ADuM7241
ADuM1200/ADuM1201
ADuM1210
ADuM3200/ADuM3201
ADuM3210/ADuM3211
ADuM1280/ADuM1281

GENERAL DESCRIPTION

The EVAL-1CH2CHSOICEBZ supports single- and dual-channel *i*Coupler® standard data isolators in 8-lead SOIC packages. The evaluation board provides a JEDEC standard, 8-lead SOIC_N and 8-lead SOIC_W pad layout. This layout supports signal distribution, loopback, and loads referenced to the VDDx or GNDx planes, as well as optimal bypass capacitance. Signal sources can be conducted to the board through header pins or through edge mounted SMA connectors (SMA connectors must be ordered separately). Screw terminal blocks on the board provide power connections. The board includes 0.2 inch header positions for compatibility with active probes (probe header pins must be ordered separately).

The evaluation board follows best PCB design practices for 4-layer boards, including a full power and ground plane on each side of the isolation barrier. No other electromagnetic interference (EMI) or noise mitigation design features are included on this board. In cases of high speed operation, or when ultralow emissions are required, refer to the AN-1109 Application Note for additional board layout techniques.

PHOTOGRAPH OF THE EVALUATION BOARD

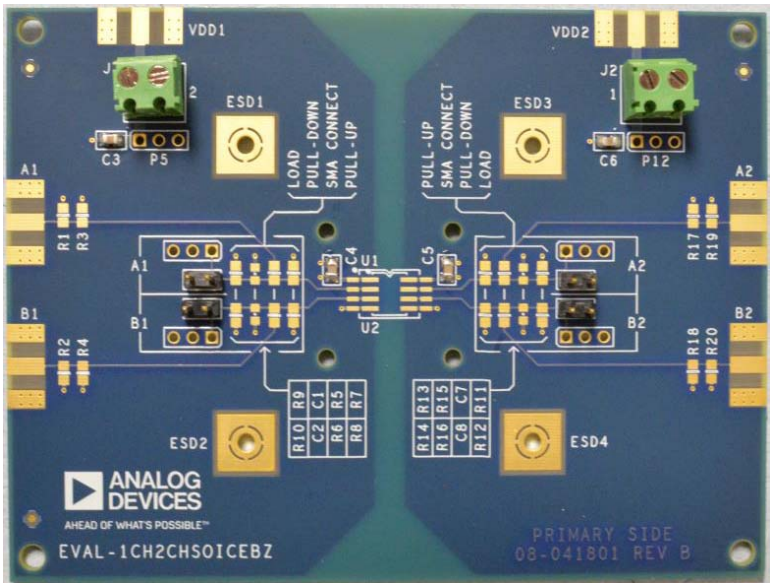

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

4/16—Revision 0: Initial Version

EVALUATION BOARD CIRCUITRY

PCB EVALUATION GOALS

The EVAL-1CH2CHSOICEBZ board is intended to achieve the following goals:

- Evaluate the full range of *i*Coupler data transfer functions.
- Independently power each side of an *i*Coupler isolator.
- Allow high differential voltage to be applied between the two sides of an *i*Coupler isolator. Note that this board is intended for evaluation of the components, but has not been safety certified for high voltage operation. If differential voltages above 60 V are applied, external safety measures appropriate for the voltage must be in place.
- Allow easy connection to power supplies, data channels, and instrumentation.

The evaluation board comes installed with power terminals, bypass capacitors, and header pins. Note that the EVAL-ADuM226N0EBZ is available with the ADuM226N0 device, which is installed on the EVAL-1CH2CHSOICEBZ evaluation board. All other compatible *i*Coupler digital isolators must be ordered and installed separately on the EVAL-1CH2CHSOICEBZ evaluation board.

The board is compatible with single- and dual-channel devices, such as the ADuM110N, ADuM120N/ADuM121N, ADuM210N, and ADuM225N/ADuM226N, as well as other 8-lead SOIC_N and 8-lead SOIC_W iCoupler devices that share the package and pin configuration examples shown in Figure 2, Figure 3, and Figure 4.

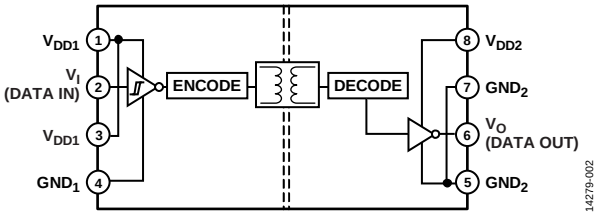

Figure 2. ADuM110N/ADuM210N Functional Block Diagram

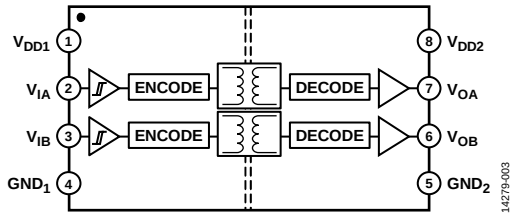

Figure 3. ADuM120N/ADuM225N Functional Block Diagram

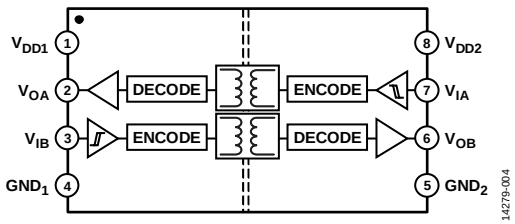

Figure 4. ADuM121N/ADuM226N Functional Block Diagram

CONNECTORS

The PCB provides support for three types of interconnections:

- SMA edge mounted connectors
- Through hole signal ground pairs
- Terminal blocks for power connections

With these three options, both temporary and permanent connections to the board can be made.

When coaxial connections are required, SMA connector positions are available for digital input/output signals and the VDD1/VDD2 power supplies. The SMA connector positions are unpopulated as shipped and must be ordered from a distributor separately. Figure 5 shows examples of installed SMA connectors; these connectors were chosen because they are not only low profile and provide excellent mechanical connections to the PCB, but also support 50 Ω coaxial cabling.

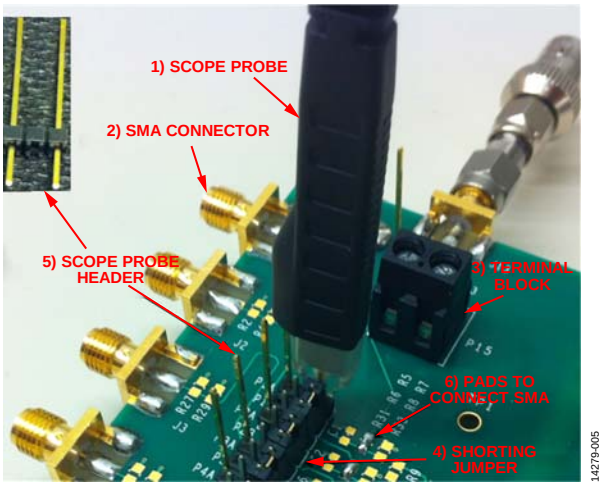

Figure 5. Optional Components

Power can be connected through the J1 and J2 terminal blocks or through the optional VDD1 and VDD2 SMA connectors. Signals can be routed in or out with the provided header pins or the optional SMA connectors. The pin spacing of each through-hole connector is 0.1 inch between the centers. There are additional signal test points with 0.2 inch spacing provided for active scope probes. These header pins must be added separately. The installed probe points are shown in Figure 5.

INPUT POWER

Each side of an *i*Coupler standard data isolator requires its own off-board power source. On the silkscreen, the J1 and J2 screw terminals are marked 1 for VDDx and 2 for GNDx.

Divided power and ground planes are present on Layer 2 and Layer 3 of the PCB on each side of the isolation barrier. This configuration is shown in Figure 9 and Figure 10, respectively.

DATA INPUT/OUTPUT (I/O) STRUCTURES

Each data channel has a variety of structures to help configure, load, and monitor both the input and output. Figure 6 shows an example of the routing from an external connection to the pin of the device under test (DUT). Each data channel has similar connections.

Starting at the external connection, the signal path is constructed in the following order (see Figure 6 for the locations of these components):

1. A pad layout for a PCB board edge mounted SMA connector.
2. Two 0805 pads are provided where 100 Ω resistors to ground can be installed. The combined resistance is 50 Ω to provide a termination for a standard coaxial cable.
3. A standard 0805 pad layout that allows the coaxial and termination structures to be connected to the rest of the signal path.
4. A 0603 pad layout between the signal path and VDDx for a pull-up resistor, if required.
5. A populated 2-pin header to provide a signal ground pair for use with clip leads or for temporarily shorting a channel to ground.
6. Groupings of three open through holes, consisting of a signal and two ground connections. These holes can be used for hardwiring signal wires into the PCB, installing a header to accept an active probe, or installing a 2-pin header to allow adjacent channels to temporarily be shorted together.
7. A 0805 pad layout between the signal and GNDx where a load capacitor or pull-down resistor can be installed.

Figure 5 shows many of the optional components installed, as well as how the jumpers can be used to temporarily connect channels. Figure 5 also shows a signal connected to the first channel SMA, which is then fanned out to the top three channels and monitored by an active scope probe.

BYPASS CAPACITANCE ON THE PCB

Several positions and structures are provided to allow optimal bypass capacitance for the DUT on the evaluation board. Provisions are made for optional surface-mount bulk capacitors to be installed near the power connectors to compensate for long cables to the power supply. Bypass capacitors are installed near the *i*Coupler data isolator and consist of a 0.1 µF capacitor for each DUT V_{DDx} pin on the top side of the board.

The PCB also implements a distributed capacitive bypass. This bypass consists of power and ground planes closely spaced on the inner layers of the PCB, which reduces noise and the transmission of EMI without using complex design features.

HIGH VOLTAGE CAPABILITY

This PCB is designed in adherence with 2500 V basic insulation practices. High voltage testing beyond 2500 V is not recommended. Do not rely on the evaluation board for safety functions.

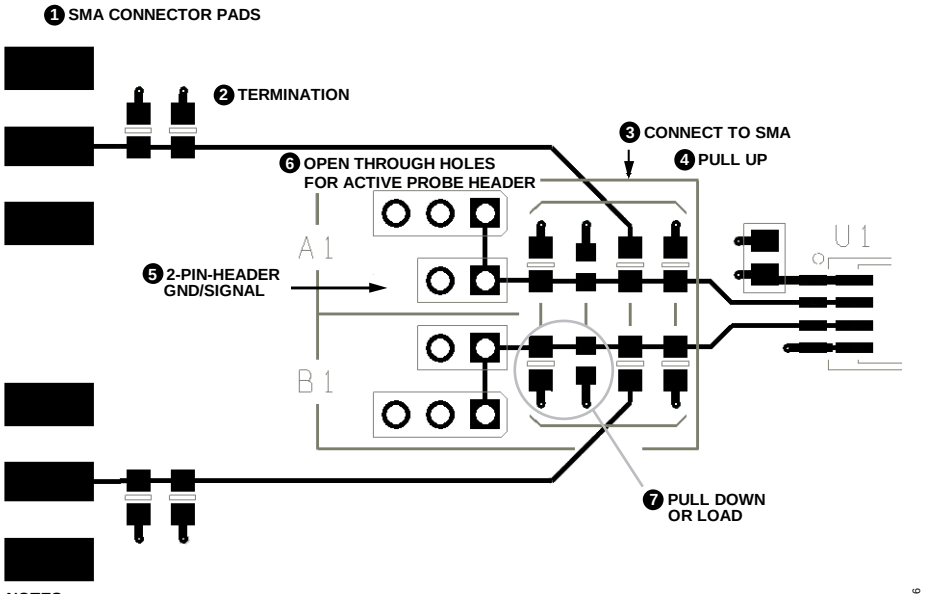

Figure 6. Configuration and Monitoring Structures

EVALUATION BOARD SCHEMATICS AND ARTWORK

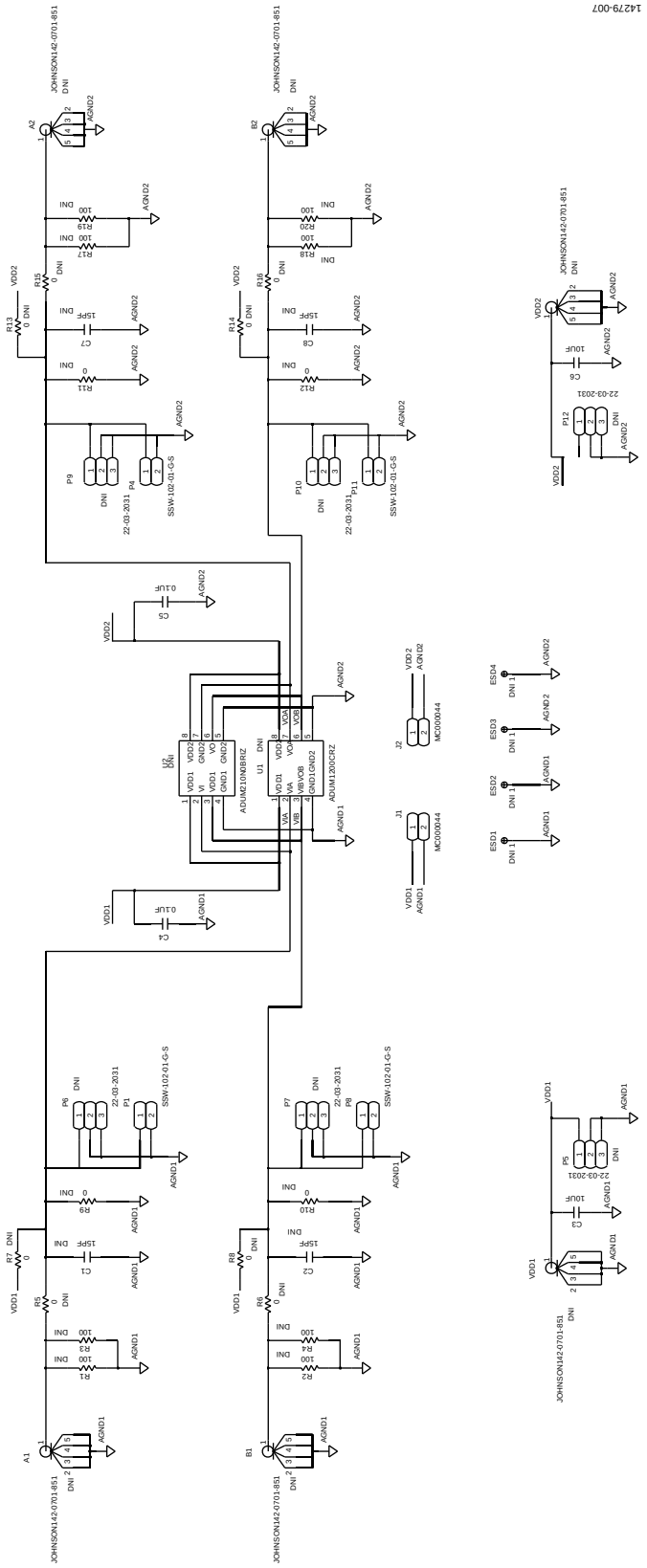

Figure 7. EVAL-1CH2CHSOICEBZ Schematic

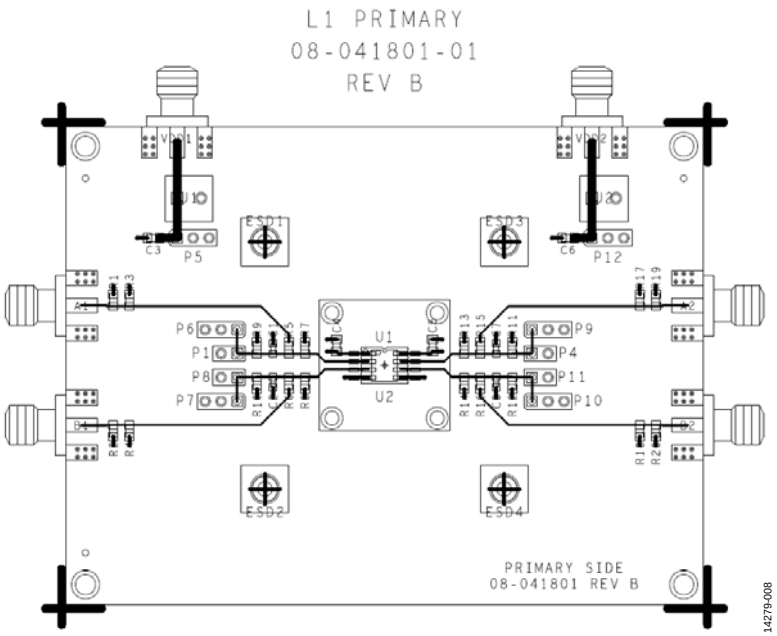

Figure 8. Top Level Signal Routing and Assembly (Layer 1)

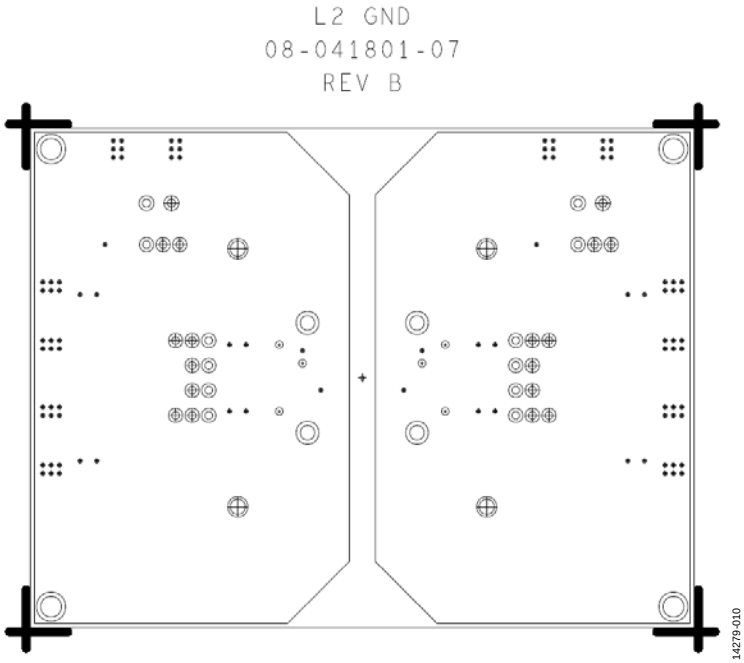

Figure 9. GND1 and GND2 Planes (Layer 2)

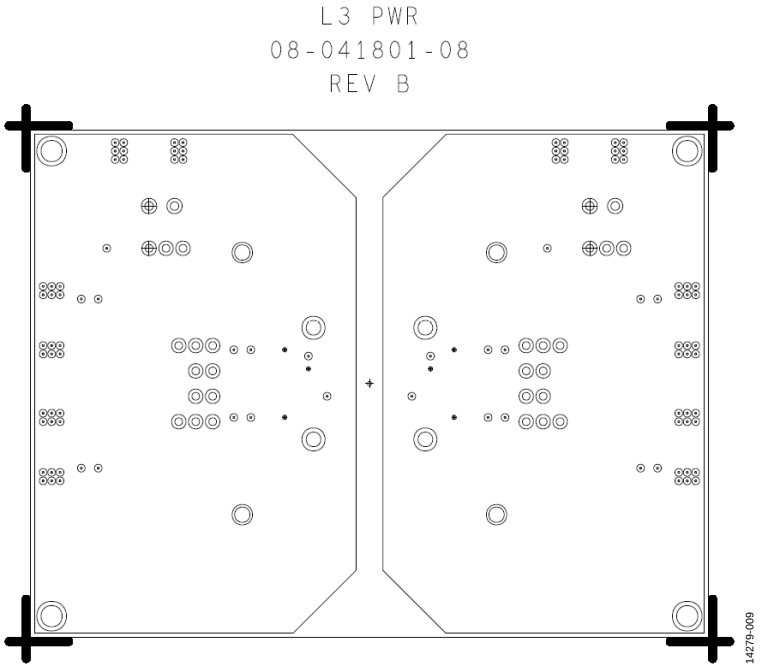

Figure 10. VDD1 and VDD2 Power Plane (Layer 3)

BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Manufacturer/Part Number
1	U1	DUT	Analog Devices, Inc./ADuM226N0BRIZ[1]
2	C3, C6	0805, 10 µF capacitor, CER monolithic	Not applicable
2	C4, C5	0805, 0.1 µF capacitor, chip X7R	Not applicable
2	J1, J2	PCB screw terminal	Multicomp/MC000044
4	P1, P4, P8, P11	2-pin header, 100 mil spacing	Not applicable
6	A1, A2, B1, B2, VDD1, VDD2	SMA edge connector (not installed)	Johnson/142-0701-851
6	P5 to P7, P9, P10, P12	2-pin header, 200 mil spacing (not installed)	Not applicable
4	C1, C2, C7, C8	0603 signal load (not installed)	Not applicable
8	R1 to R4, R17 to R20	0805, 100 Ω resistors (not installed)	Not applicable
12	R5 to R16	0805, 0 Ω resistors (not installed)	Not applicable

[1] This is the DUT installed on the EVAL-ADuM226N0EBZ; otherwise, this location is unpopulated.