Dual 12-/14-/16-Bit, 1 GSPS, Digital-to-Analog Converters

AD9776/AD9778/AD9779

FEATURES

Low power: 1.0 W @ 1 GSPS, 600 mW @ 500 MSPS, full operating conditions
SFDR = 78 dBc to f_{OUT} = 100 MHz
Single carrier WCDMA ACLR = 79 dBc @ 80 MHz IF
Analog output: adjustable 8.7 mA to 31.7 mA, R_L = 25 Ω to 50 Ω
Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth
Auxiliary DACs allow control of external VGA and offset control
Multiple chip synchronization interface
High performance, low noise PLL clock multiplier
Digital inverse sinc filter
100-lead, exposed paddle TQFP package

APPLICATIONS

Wireless infrastructure
WCDMA, CDMA2000, TD-SCDMA, WiMax, GSM
Digital high or low IF synthesis
Internal digital upconversion capability
Transmit diversity
Wideband communications: LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9776/AD9778/AD9779 are dual, 12-/14-/16-bit, high dynamic range, digital-to-analog converters (DACs) that provide a sample rate of 1 GSPS, permitting multicarrier generation up to the Nyquist frequency. They include features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators such as the AD8349. A serial peripheral interface (SPI®) provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 10 mA to 30 mA. The devices are manufactured on an advanced 0.18 μm CMOS process and operate on 1.8 V and 3.3 V supplies for a total power consumption of 1.0 W. They are enclosed in 100-lead TQFP packages.

PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.
2. A proprietary DAC output switching technique enhances dynamic performance.
3. The current outputs are easily configured for various single-ended or differential circuit topologies.
4. CMOS data input interface with adjustable set up and hold.
5. Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth.

TYPICAL SIGNAL CHAIN

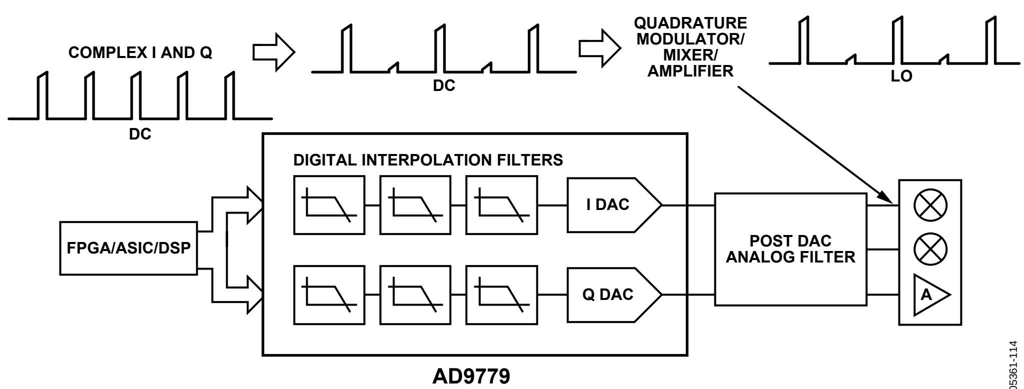

Figure 1.

Rev. A

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TABLE OF CONTENTS

REVISION HISTORY

3/07—Rev. 0 to Rev. A

Changes to Features ... 1
Changes to Applications ... 1
Changes to General Product Highlights ... 1
Added Figure 1, Renumbered Figures Sequentially ... 1
Changes to Table 1 ... 4
Changes to Table 2 ... 5
Changes to Table 3 ... 5
Changes to Figure 53 and Figure 54 ... 26
Changes to Table 12 ... 29
Changes to Power Dissipation Section ... 39
Added Table 19, Renumbered Tables Sequentially ... 41
Changes to Figure 92 and Figure 93 ... 42
Changes to Figure 94 ... 42
Added New Figure 95, Renumbered Figures Sequentially ... 42
Changes to Synchronization of Input Data to the REFCLK Input (Pin 5 and Pin 6) with PLL Enabled or Disabled Section ... 43
Added New Figure 96, Renumbered Figures Sequentially ... 43
Changes to Figure 106 ... 51

7/05—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

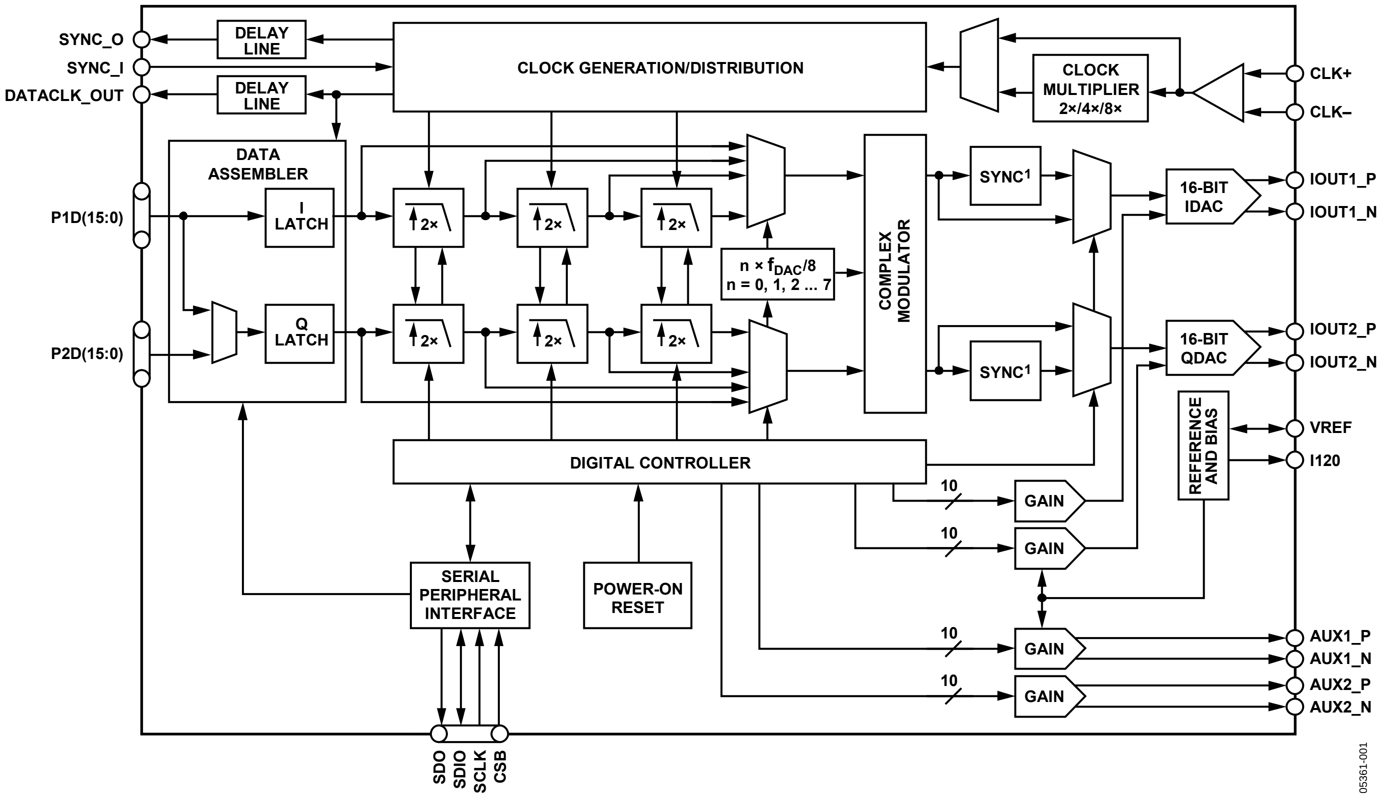


Figure 2. Functional Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 =1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1. AD9776, AD9778, and AD9779 DC Specifications

	AD9776			AD9778			AD9779			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.1			±0.65			±2.1		LSB
Integral Nonlinearity (INL)		±0.6			±1			±3.7		LSB
MAIN DAC OUTPUTS										
Offset Error	−0.001	0	+0.001	−0.001	0	+0.001	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)		±2			±2			±2		% FSR
Full-Scale Output Current[1]	8.66	20.2	31.66	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
Gain DAC Monotonicity		Guaranteed			Guaranteed			Guaranteed		
MAIN DAC TEMPERATURE DRIFT										
Offset		0.04			0.04			0.04		ppm/°C
Gain		100			100			100		ppm/°C
Reference Voltage		30			30			30		ppm/°C
AUX DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current[1]	−1.998		+1.998	−1.998		+1.998	−1.998		+1.998	mA
Output Compliance Range (Source)	0		1.6	0		1.6	0		1.6	V
Output Compliance Range (Sink)	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Resistance		1			1			1		MΩ
Aux DAC Monotonicity Guaranteed										
REFERENCE										
Internal Reference Voltage		1.2			1.2			1.2		V
Output Resistance		5			5			5		kΩ
ANALOG SUPPLY VOLTAGES										
AVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
CVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES										
DVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
DVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
POWER CONSUMPTION										
1× Mode, f_{DAC} = 100 MSPS, IF = 1 MHz		250	300		250	300		250	300	mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL Off		498			498			498		mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL On		588			588			588		mW
4× Mode, f_{DAC}/4 Modulation, f_{DAC} = 500 MSPS, IF = 137.5 MHz, Q DAC Off		572			572			572		mW

Parameter	AD9776 Min	AD9776 Typ	AD9776 Max	AD9778 Min	AD9778 Typ	AD9778 Max	AD9779 Min	AD9779 Typ	AD9779 Max	Unit
8× Mode, f_{DAC}/4 Modulation, f_{DAC} = 1 GSPS, IF = 262.5 MHz		980			980			980		mW
Power-Down Mode		2	3.7		2	3.7		2	3.7	mW
Power Supply Rejection Ratio, AVDD33	−0.3		+0.3	−0.3		+0.3	−0.3		+0.3	% FSR/V
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted. LVDS driver and receiver are compliant to the IEEE-1596 reduced range link, unless otherwise noted.

Table 2. AD9776, AD9778, and AD9779 Digital Specifications

Parameter	Conditions	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High		2.0			V
Input V_{IN} Logic Low				0.8	V
Maximum Input Data Rate at Interpolation					
1×		300			MSPS
2×		250			MSPS
4×		200			MSPS
8×		125			MSPS
CMOS OUTPUT LOGIC LEVEL (DATACLK, PIN 37)[1]					
Output V_{OUT} Logic High		2.4			V
Output V_{OUT} Logic Low				0.4	V
LVDS RECEIVER INPUTS (SYNC_I+, SYNC_I−)	SYNC_I+ = V_{IA}, SYNC_I− = V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}		825		1575	mV
Input Differential Threshold, V_{IDTH}		−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$			20		mV
Receiver Differential Input Impedance, R_{IN}[2]		80		120	Ω
LVDS Input Rate				125	MSPS
Set-Up Time, SYNC_I to DAC Clock		−0.2			ns
Hold Time, SYNC_I to DAC Clock		1			ns
LVDS DRIVER OUTPUTS (SYNC_O+, SYNC_O−)	SYNC_O+ = V_{OA}, SYNC_O− = V_{OB}, 100 Ω termination				
Output Voltage High, V_{OA} or V_{OB}		825		1575	mV
Output Voltage Low, V_{OA} or V_{OB}		1025			mV
Output Differential Voltage, $\|V_{OD}\|$		150	200	250	mV
Output Offset Voltage, V_{OS}		1150		1250	mV
Output Impedance, R_O	Single-ended	80	100	120	Ω
Maximum Clock Rate		1			GHz
DAC CLOCK INPUT (CLK+, CLK−)					
Differential Peak-to-Peak Voltage (CLK+, CLK−)[3]		400	800	2000	mV
Common-Mode Voltage		300	400	500	mV
Maximum Clock Rate[4]		1			GSPS
SERIAL PERIPHERAL INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High				12.5	ns
Minimum Pulse Width Low				12.5	ns

[1] Specification is at a DATACLK frequency of 100 MHz into a 1 kΩ load; maximum drive capability of 8 mA. At higher speeds or greater loads, best practice suggests using an external buffer for this signal.
[2] Guaranteed at 25°C. Can drift above 120 Ω at temperatures above 25°C.
[3] When using the PLL, a differential swing of 2 V p-p is recommended.
[4] Typical maximum clock rate when DVDD18 = CVDD18 = 1.9 V.

DIGITAL INPUT DATA TIMING SPECIFICATIONS

Table 3. AD9776, AD9778, and AD9779 Digital Input Data Timing Specifications

Parameter	Min	Typ	Max	Unit
INPUT DATA (ALL MODES, −40°C to +85°C)[1]				
Set-Up Time, Input Data to DATACLK	+2.5			ns
Hold Time, Input Data to DATACLK	−0.4			ns
Set-Up Time, Input Data to REFCLK	−0.8			ns
Hold Time, Input Data to REFCLK	+2.9			ns

[1] Timing vs. temperature and data valid keep out windows are delineated in Table 19.

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 4. AD9776, AD9778, and AD9779 AC Specifications

	AD9776			AD9778			AD9779			
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		82			82			82		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		81			81			82		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		85			85			87		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)										
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		87			87			91		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		80			85			85		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		75			81			81		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		75			80			81		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING										
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		−152			−155			−158		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		−155			−159			−160		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		−157.5			−160			−161		dBm/Hz
WCDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		76			78			79		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		69			73			74		dBc
WCDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		77.5			80			81		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		76			78			78		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

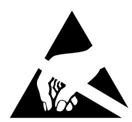
Parameter	With Respect To	Rating
AVDD33, DVDD33	AGND, DGND, CGND	−0.3 V to +3.6 V
DVDD18, CVDD18	AGND, DGND, CGND	−0.3 V to +1.98 V
AGND	DGND, CGND	−0.3 V to +0.3 V
DGND	AGND, CGND	−0.3 V to +0.3 V
CGND	AGND, DGND	−0.3 V to +0.3 V
I120, VREF, IPTAT	AGND	−0.3 V to AVDD33 + 0.3 V
I_{OUT1-P}, I_{OUT1-N}, I_{OUT2-P}, I_{OUT2-N}, Aux_{1-P}, Aux_{1-N}, Aux_{2-P}, Aux_{2-N}	AGND	−1.0 V to AVDD33 + 0.3 V
P1D15 to P1D0, P2D15 to P2D0	DGND	−0.3 V to DVDD33 + 0.3 V
DATACLK, TXENABLE	DGND	−0.3 V to DVDD33 + 0.3 V
CLK+, CLK−	CGND	−0.3 V to CVDD18 + 0.3 V
RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I−, CSB, SCLK, SDIO, SDO	DGND	−0.3 V to DVDD33 + 0.3 V
Junction Temperature		+125°C
Storage Temperature Range		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

100-lead, thermally enhanced TQFP_EP package, θ_{JA} = 19.1°C/W with the bottom EPAD soldered to the PCB. With the bottom EPAD not soldered to the PCB, θ_{JA} = 27.4°C/W. These specifications are valid with no airflow movement.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

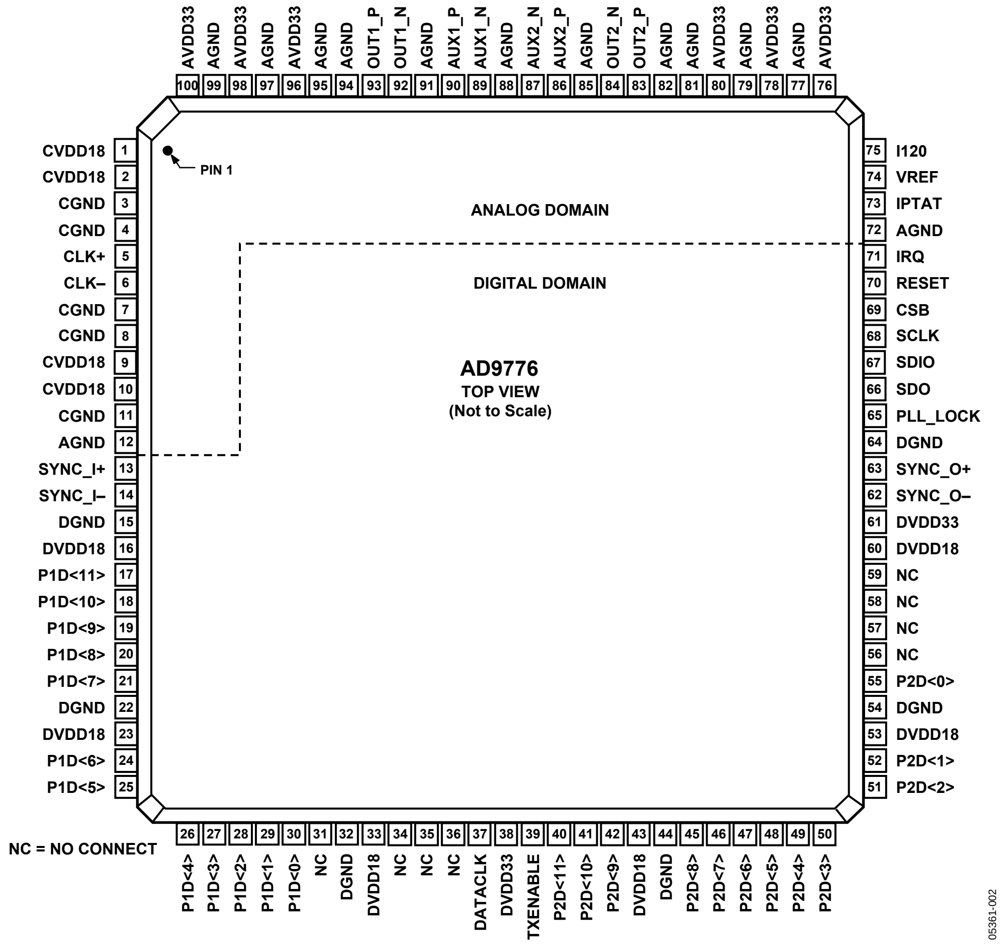


Figure 3. AD9776 Pin Configuration

Table 6. AD9776 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Common.
4	CGND	Clock Common.
5	CLK+[1]	Differential Clock Input.
6	CLK–[1]	Differential Clock Input.
7	CGND	Clock Common.
8	CGND	Clock Common.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Common.
12	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Common.
16	DVDD18	1.8 V Digital Supply.
17	P1D<11>	Port 1, Data Input D11 (MSB).
18	P1D<10>	Port 1, Data Input D10.
19	P1D<9>	Port 1, Data Input D9.
20	P1D<8>	Port 1, Data Input D8.
21	P1D<7>	Port 1, Data Input D7.
22	DGND	Digital Common.
23	DVDD18	1.8 V Digital Supply.
24	P1D<6>	Port 1, Data Input D6.
25	P1D<5>	Port 1, Data Input D5.
26	P1D<4>	Port 1, Data Input D4.
27	P1D<3>	Port 1, Data Input D3.
28	P1D<2>	Port 1, Data Input D2.
29	P1D<1>	Port 1, Data Input D1.
30	P1D<0>	Port 1, Data Input D0 (LSB).
31	NC	No Connect.
32	DGND	Digital Common.
33	DVDD18	1.8 V Digital Supply.
34	NC	No Connect.
35	NC	No Connect.
36	NC	No Connect.
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.

Pin No.	Mnemonic	Description
39	TXENABLE	Transmit Enable.
40	P2D<11>	Port 2, Data Input D11 (MSB).
41	P2D<10>	Port 2, Data Input D10.
42	P2D<9>	Port 2, Data Input D9.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Common.
45	P2D<8>	Port 2, Data Input D8.
46	P2D<7>	Port 2, Data Input D7.
47	P2D<6>	Port 2, Data Input D6.
48	P2D<5>	Port 2, Data Input D5.
49	P2D<4>	Port 2, Data Input D4.
50	P2D<3>	Port 2, Data Input D3.
51	P2D<2>	Port 2, Data Input D2.
52	P2D<1>	Port 2, Data Input D1.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Common.
55	P2D<0>	Port 2, Data Input D0 (LSB).
56	NC	No Connect.
57	NC	No Connect.
58	NC	No Connect.
59	NC	No Connect.
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O–	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output
64	DGND	Digital Common
65	PLL_LOCK	PLL Lock Indicator
66	SDO	SPI Port Data Output
67	SDIO	SPI Port Data Input/Output
68	SCLK	SPI Port Clock
69	CSB	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
72	AGND	Analog Common.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 μA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.
74	VREF	Voltage Reference Output.
75	I120	120 μA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Common.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Common.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Common.
82	AGND	Analog Common.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Common.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Common.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Common.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Common.
95	AGND	Analog Common.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Common.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Common.
100	AVDD33	3.3 V Analog Supply.

[1] The combined differential clock input at the CLK+ and CLK– pins are referred to as REFCLK.

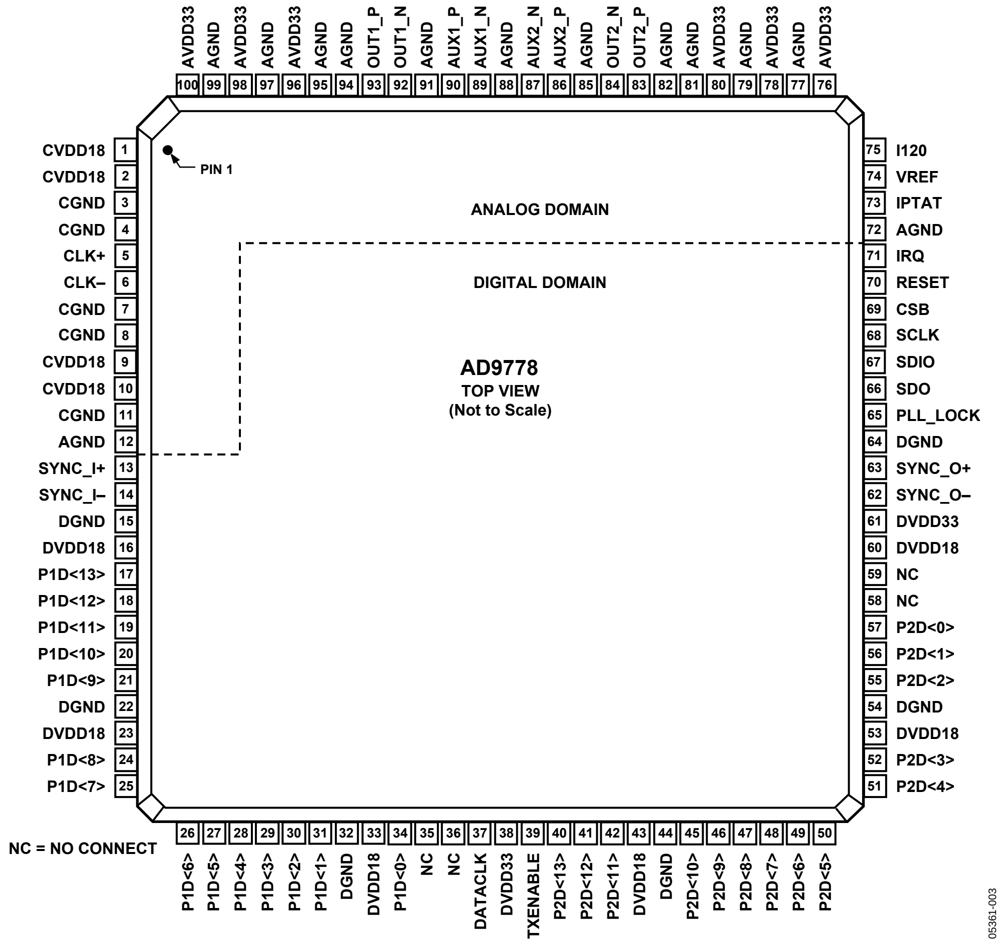


Figure 4. AD9778 Pin Configuration

Table 7. AD9778 Pin Function Description

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Common.
4	CGND	Clock Common.
5	CLK+[1]	Differential Clock Input.
6	CLK–[1]	Differential Clock Input.
7	CGND	Clock Common.
8	CGND	Clock Common.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Common.
12	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Common.
16	DVDD18	1.8 V Digital Supply.
17	P1D<13>	Port 1, Data Input D13 (MSB).
18	P1D<12>	Port 1, Data Input D12.
19	P1D<11>	Port 1, Data Input D11.
20	P1D<10>	Port 1, Data Input D10.
21	P1D<9>	Port 1, Data Input D9.
22	DGND	Digital Common.
23	DVDD18	1.8 V Digital Supply.
24	P1D<8>	Port 1, Data Input D8.
25	P1D<7>	Port 1, Data Input D7.
26	P1D<6>	Port 1, Data Input D6.
27	P1D<5>	Port 1, Data Input D5.
28	P1D<4>	Port 1, Data Input D4.
29	P1D<3>	Port 1, Data Input D3.
30	P1D<2>	Port 1, Data Input D2.
31	P1D<1>	Port 1, Data Input D1.
32	DGND	Digital Common.
33	DVDD18	1.8 V Digital Supply.
34	P1D<0>	Port 1, Data Input D0 (LSB).
35	NC	No Connect.
36	NC	No Connect.
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D<13>	Port 2, Data Input D13 (MSB).

Pin No.	Mnemonic	Description
41	P2D<12>	Port 2, Data Input D12.
42	P2D<11>	Port 2, Data Input D11.
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Common.
45	P2D<10>	Port 2, Data Input D10.
46	P2D<9>	Port 2, Data Input D9.
47	P2D<8>	Port 2, Data Input D8.
48	P2D<7>	Port 2, Data Input D7.
49	P2D<6>	Port 2, Data Input D6.
50	P2D<5>	Port 2, Data Input D5.
51	P2D<4>	Port 2, Data Input D4.
52	P2D<3>	Port 2, Data Input D3.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Common.
55	P2D<2>	Port 2, Data Input D2.
56	P2D<1>	Port 2, Data Input D1.
57	P2D<0>	Port 2, Data Input D0 (LSB).
58	NC	No Connect.
59	NC	No Connect.
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O−	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Common.
65	PLL_LOCK	PLL Lock Indicator.
66	SDO	SPI Port Data Output.
67	SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	CSB	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
72	AGND	Analog Common.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 μA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.

Pin No.	Mnemonic	Description
74	VREF	Voltage Reference Output.
75	I120	120 μA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Common.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Common.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Common.
82	AGND	Analog Common.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Common.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Common.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Common.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Common.
95	AGND	Analog Common.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Common.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Common.
100	AVDD33	3.3 V Analog Supply.

[1] The combined differential clock input at the CLK+ and CLK− pins are referred to as REFCLK.

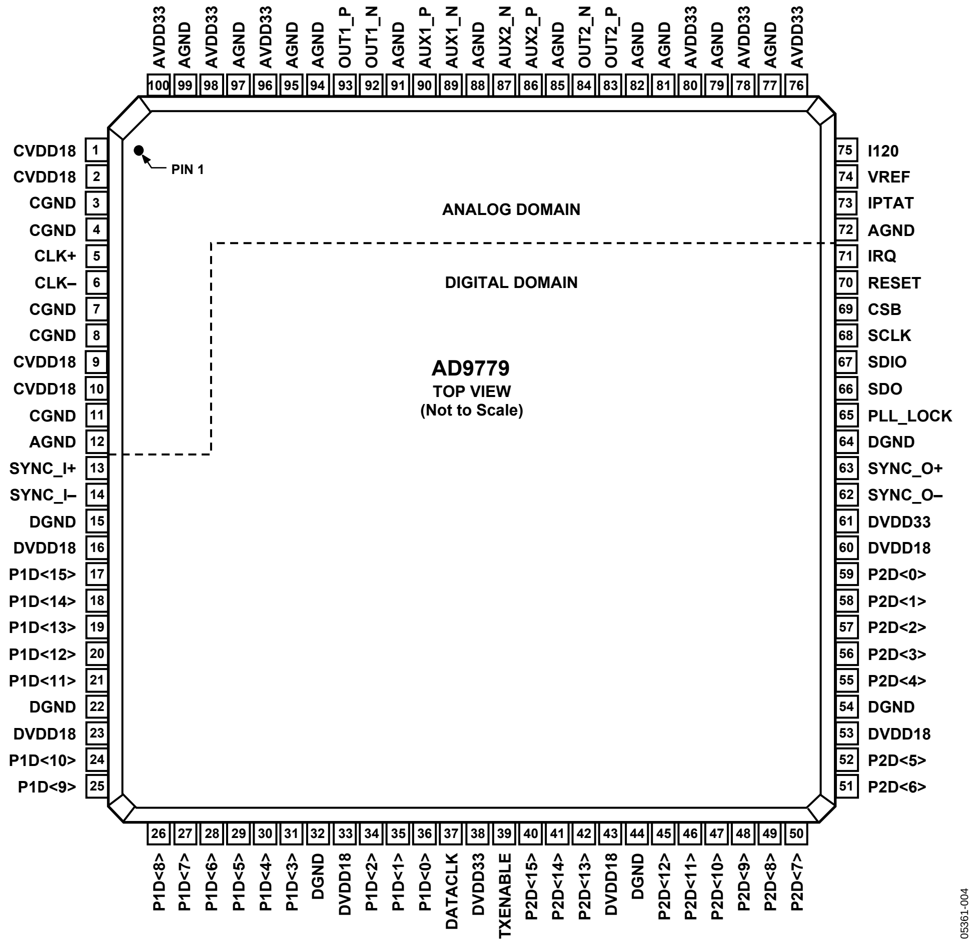


Figure 5. AD9779 Pin Configuration

Table 8. AD9779 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply.
2	CVDD18	1.8 V Clock Supply.
3	CGND	Clock Common.
4	CGND	Clock Common.
5	CLK+[1]	Differential Clock Input.
6	CLK–[1]	Differential Clock Input.
7	CGND	Clock Common.
8	CGND	Clock Common.
9	CVDD18	1.8 V Clock Supply.
10	CVDD18	1.8 V Clock Supply.
11	CGND	Clock Common.
12	AGND	Analog Common.
13	SYNC_I+	Differential Synchronization Input.
14	SYNC_I–	Differential Synchronization Input.
15	DGND	Digital Common.
16	DVDD18	1.8 V Digital Supply.
17	P1D<15>	Port 1, Data Input D15 (MSB).
18	P1D<14>	Port 1, Data Input D14.
19	P1D<13>	Port 1, Data Input D13.
20	P1D<12>	Port 1, Data Input D12.
21	P1D<11>	Port 1, Data Input D11.
22	DGND	Digital Common.
23	DVDD18	1.8 V Digital Supply.
24	P1D<10>	Port 1, Data Input D10.
25	P1D<9>	Port 1, Data Input D9.
26	P1D<8>	Port 1, Data Input D8.
27	P1D<7>	Port 1, Data Input D7.
28	P1D<6>	Port 1, Data Input D6.
29	P1D<5>	Port 1, Data Input D5.
30	P1D<4>	Port 1, Data Input D4.
31	P1D<3>	Port 1, Data Input D3.
32	DGND	Digital Common.
33	DVDD18	1.8 V Digital Supply.
34	P1D<2>	Port 1, Data Input D2.
35	P1D<1>	Port 1, Data Input D1.
36	P1D<0>	Port 1, Data Input D0 (LSB).
37	DATACLK	Data Clock Output.
38	DVDD33	3.3 V Digital Supply.
39	TXENABLE	Transmit Enable.
40	P2D<15>	Port 2, Data Input D15 (MSB).
41	P2D<14>	Port 2, Data Input D14.
42	P2D<13>	Port 2, Data Input D13.

Pin No.	Mnemonic	Description
43	DVDD18	1.8 V Digital Supply.
44	DGND	Digital Common.
45	P2D<12>	Port 2, Data Input D12.
46	P2D<11>	Port 2, Data Input D11.
47	P2D<10>	Port 2, Data Input D10.
48	P2D<9>	Port 2, Data Input D9.
49	P2D<8>	Port 2, Data Input D8.
50	P2D<7>	Port 2, Data Input D7.
51	P2D<6>	Port 2, Data Input D6.
52	P2D<5>	Port 2, Data Input D5.
53	DVDD18	1.8 V Digital Supply.
54	DGND	Digital Common.
55	P2D<4>	Port 2, Data Input D4.
56	P2D<3>	Port 2, Data Input D3.
57	P2D<2>	Port 2, Data Input D2.
58	P2D<1>	Port 2, Data Input D1.
59	P2D<0>	Port 2, Data Input D0 (LSB).
60	DVDD18	1.8 V Digital Supply.
61	DVDD33	3.3 V Digital Supply.
62	SYNC_O−	Differential Synchronization Output.
63	SYNC_O+	Differential Synchronization Output.
64	DGND	Digital Common.
65	PLL_LOCK	PLL Lock Indicator.
66	SPI_SDO	SPI Port Data Output.
67	SPI_SDIO	SPI Port Data Input/Output.
68	SCLK	SPI Port Clock.
69	SPI_CSB	SPI Port Chip Select Bar.
70	RESET	Reset, Active High.
71	IRQ	Interrupt Request.
72	AGND	Analog Common.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 10 μA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.

Pin No.	Mnemonic	Description
74	VREF	Voltage Reference Output.
75	I120	120 μA Reference Current.
76	AVDD33	3.3 V Analog Supply.
77	AGND	Analog Common.
78	AVDD33	3.3 V Analog Supply.
79	AGND	Analog Common.
80	AVDD33	3.3 V Analog Supply.
81	AGND	Analog Common.
82	AGND	Analog Common.
83	OUT2_P	Differential DAC Current Output, Channel 2.
84	OUT2_N	Differential DAC Current Output, Channel 2.
85	AGND	Analog Common.
86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
88	AGND	Analog Common.
89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
91	AGND	Analog Common.
92	OUT1_N	Differential DAC Current Output, Channel 1.
93	OUT1_P	Differential DAC Current Output, Channel 1.
94	AGND	Analog Common.
95	AGND	Analog Common.
96	AVDD33	3.3 V Analog Supply.
97	AGND	Analog Common.
98	AVDD33	3.3 V Analog Supply.
99	AGND	Analog Common.
100	AVDD33	3.3 V Analog Supply.

[1] The combined differential clock input at the CLK+ and CLK− pins are referred to as REFCLK.

TYPICAL PERFORMANCE CHARACTERISTICS

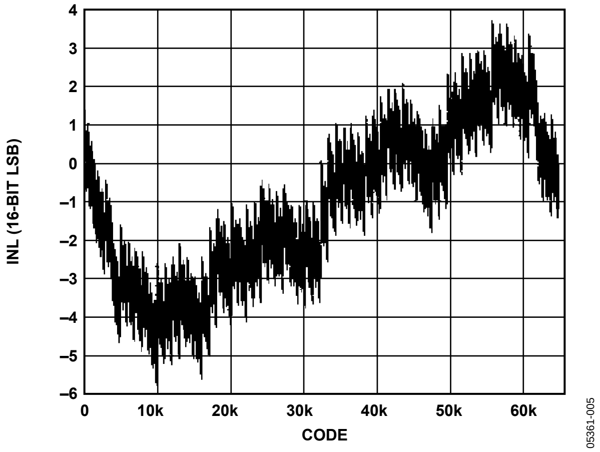


Figure 6. AD9779 Typical INL

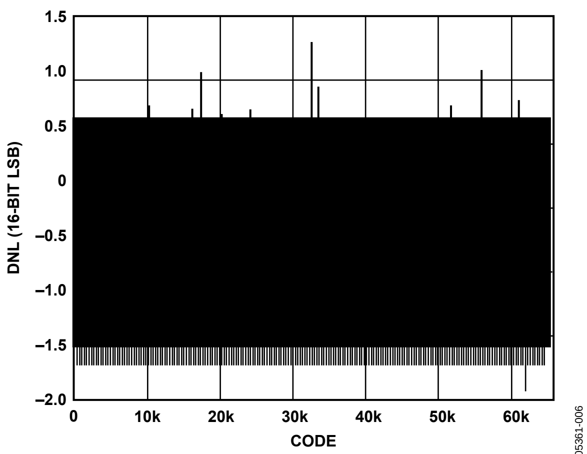


Figure 7. AD9779 Typical DNL

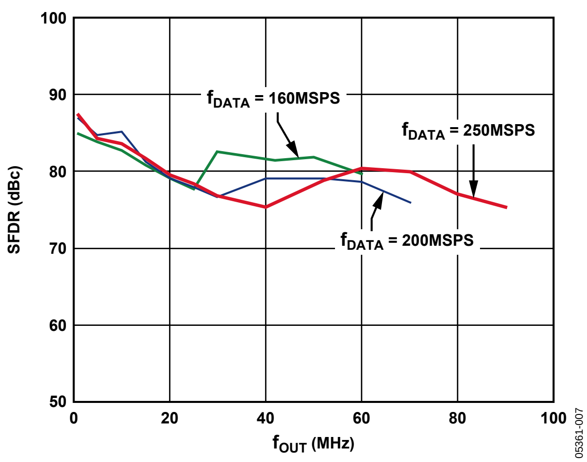


Figure 8. AD9779 In-Band SFDR vs. f_{OUT}, 1x Interpolation

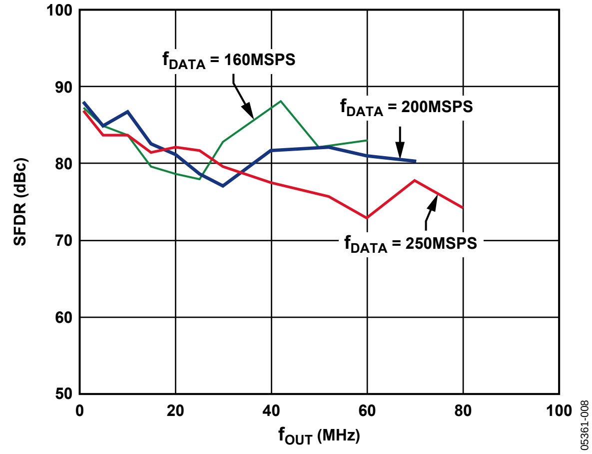


Figure 9. AD9779 In-Band SFDR vs. f_{OUT}, 2× Interpolation

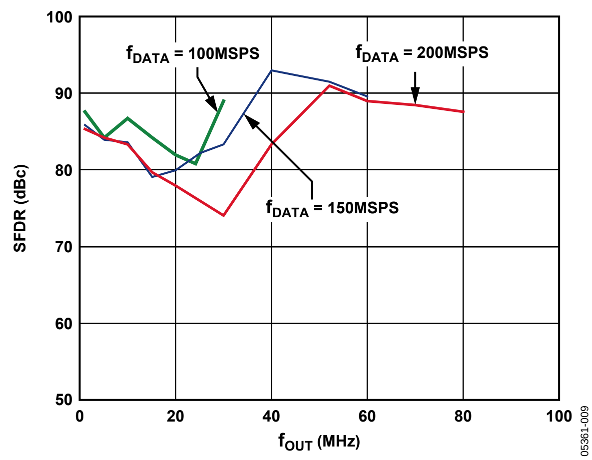


Figure 10. AD9779 In-Band SFDR vs. f_{OUT}, 4× Interpolation

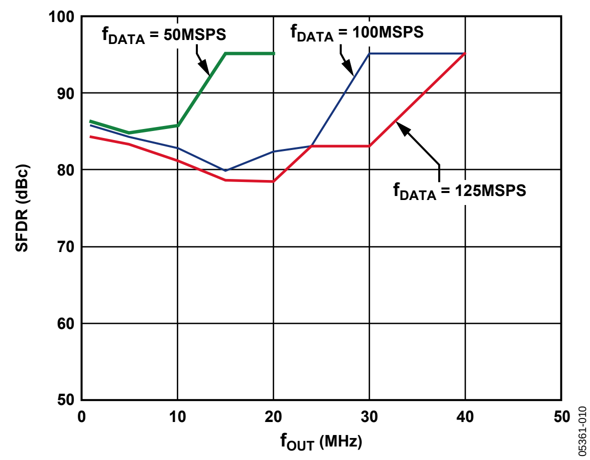


Figure 11. AD9779 In-Band SFDR vs. f_{OUT}, 8× Interpolation

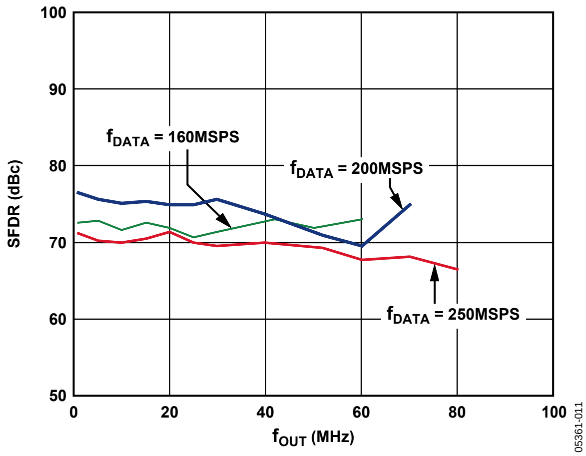


Figure 12. AD9779 Out-of-Band SFDR vs. f_{OUT}, 2× Interpolation

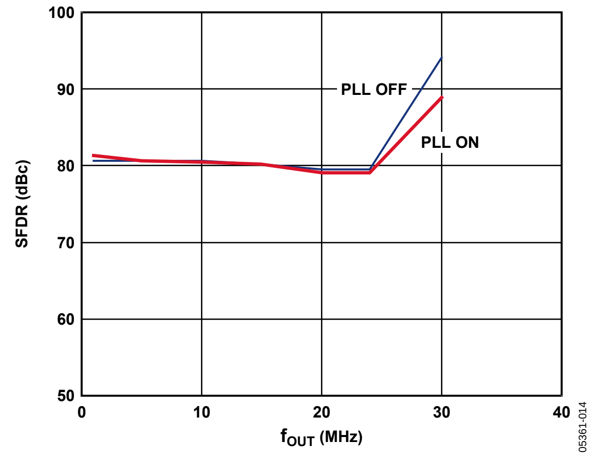


Figure 15. AD9779 In-Band SFDR, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/Off

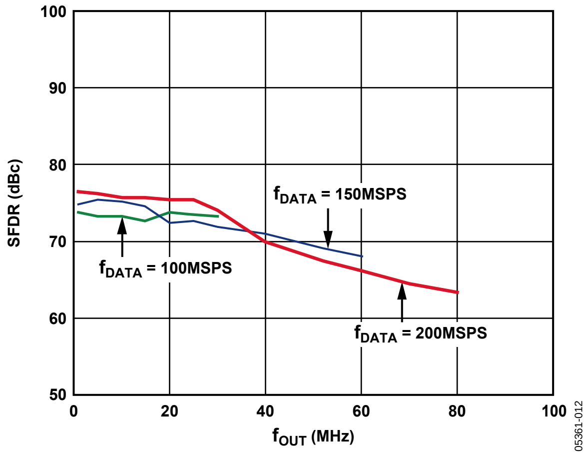


Figure 13. AD9779 Out-of-Band SFDR vs. f_{OUT}, 4× Interpolation

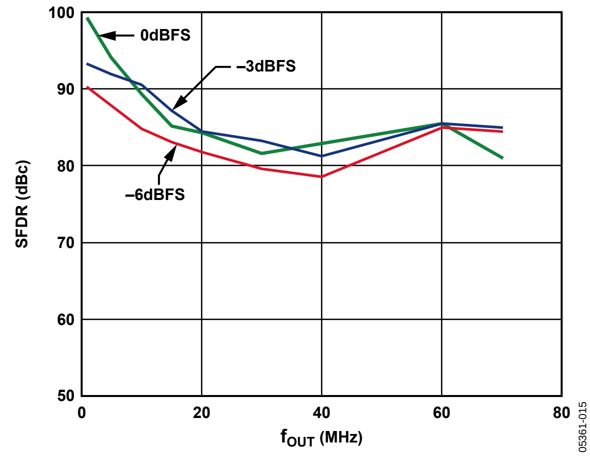


Figure 16. AD9779 In-Band SFDR vs. Digital Full-Scale Input

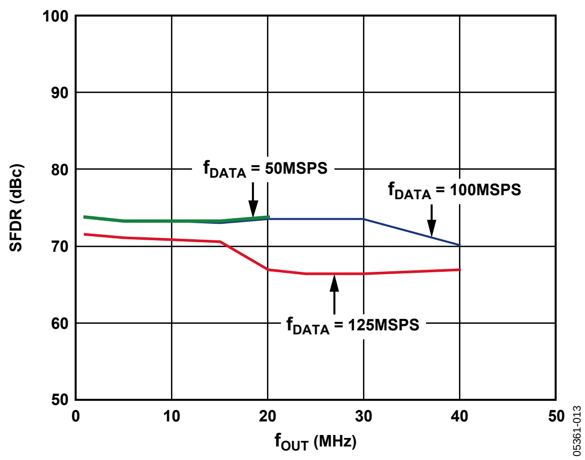


Figure 14. AD9779 Out-of-Band SFDR vs. f_{OUT}, 8× Interpolation

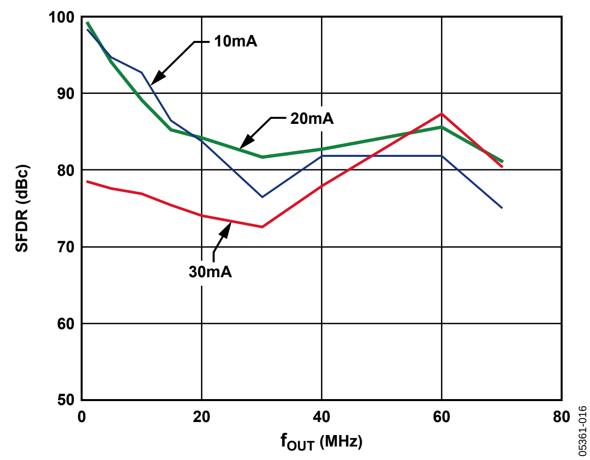


Figure 17. AD9779 In-Band SFDR vs. Output Full-Scale Current

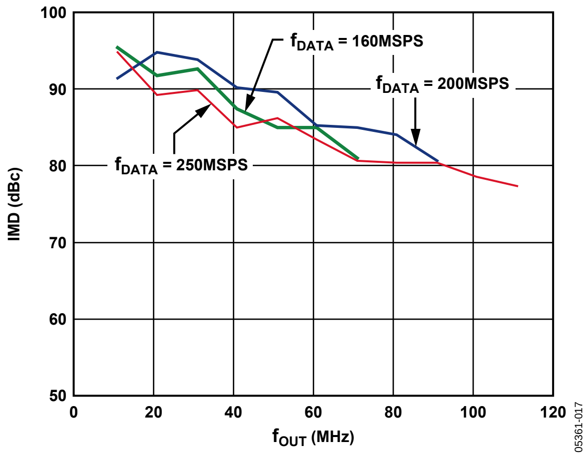


Figure 18. AD9779 Third-Order IMD vs. f_{OUT}, 1× Interpolation

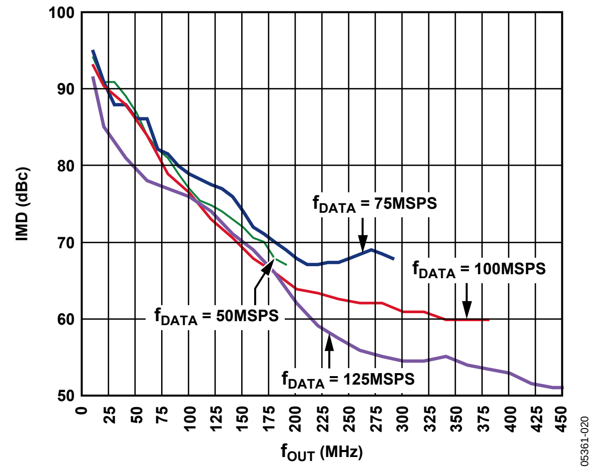


Figure 21. AD9779 Third-Order IMD vs. f_{OUT}, 8× Interpolation

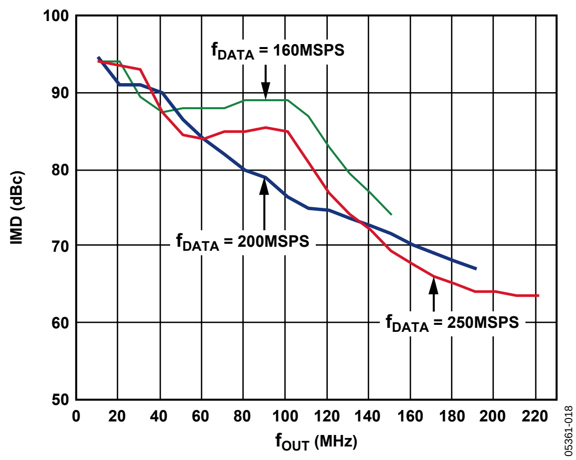


Figure 19. AD9779 Third-Order IMD vs. f_{OUT}, 2× Interpolation

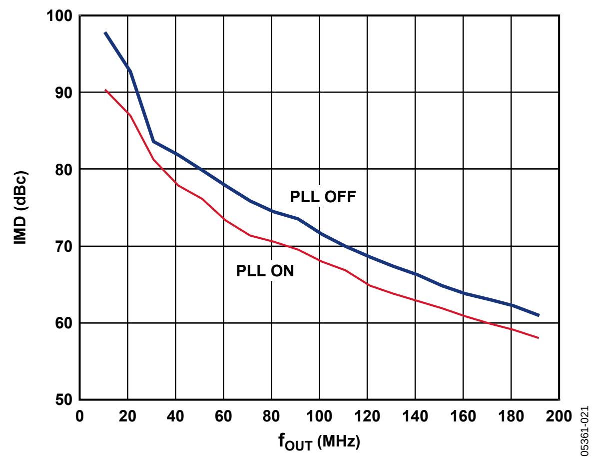


Figure 22. AD9779 Third-Order IMD vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On vs. PLL Off

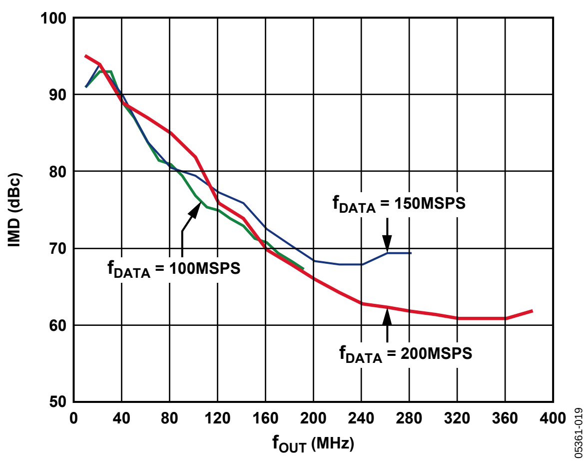


Figure 20. AD9779 Third-Order IMD vs. f_{OUT}, 4× Interpolation

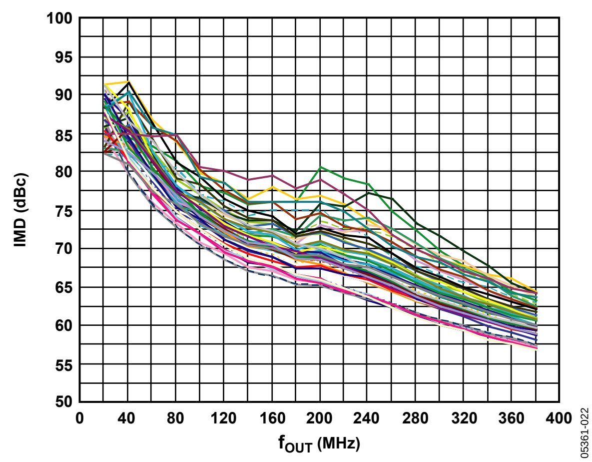


Figure 23. AD9779 Third-Order IMD vs. f_{OUT}, over 50 Parts,4× Interpolation, f_{DATA} = 200 MSPS

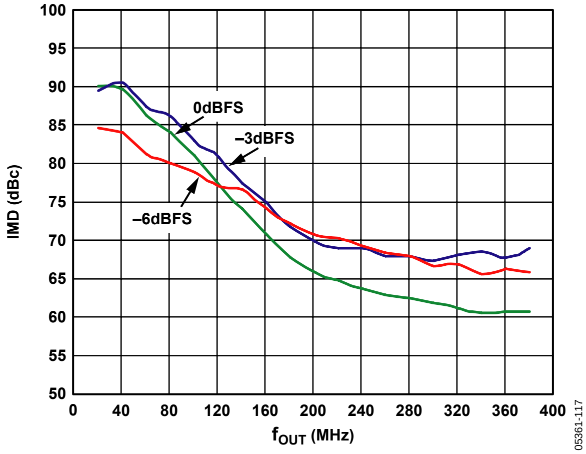


Figure 24. IMD Performance vs. Digital Full-Scale Input, 4× Interpolation, f_{DATA} = 200 MSPS

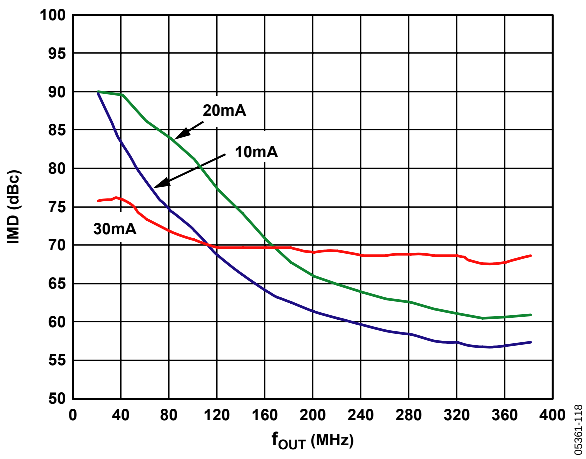


Figure 25. IMD Performance vs. Full-Scale Output Current, 4× Interpolation, f_{DATA} = 200 MSPS

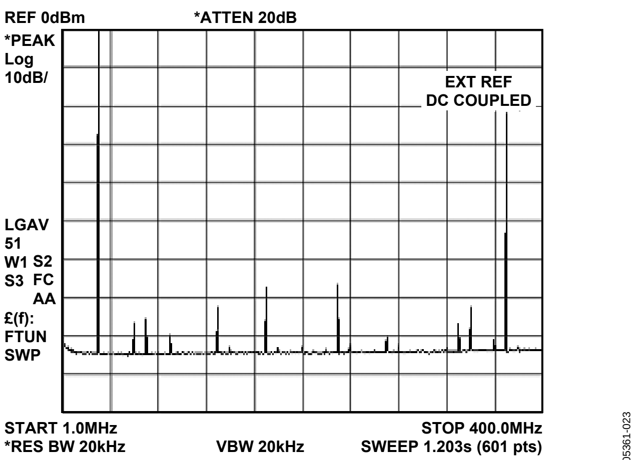


Figure 26. AD9779 Single Tone, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz

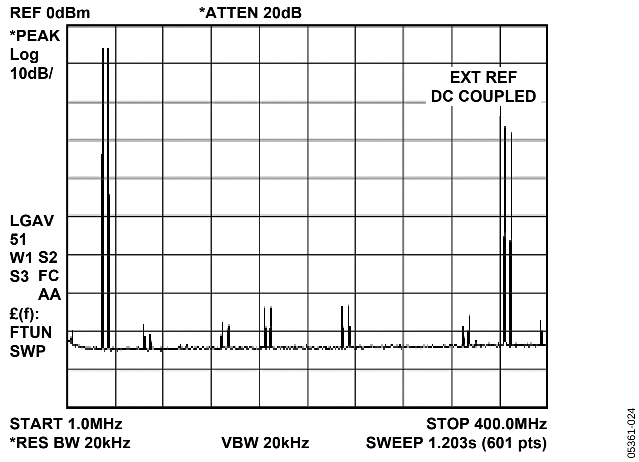


Figure 27. AD9779 Two-Tone Spectrum, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz, 35 MHz

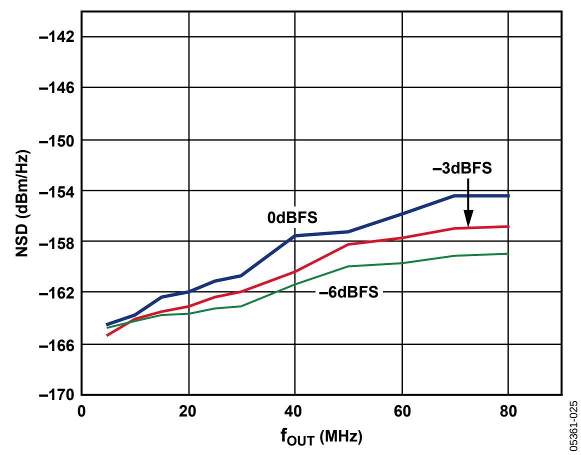


Figure 28. AD9779 Noise Spectral Density vs. Digital Full-Scale of Single-Tone Input, f_{DATA} = 200 MSPS, 2× Interpolation

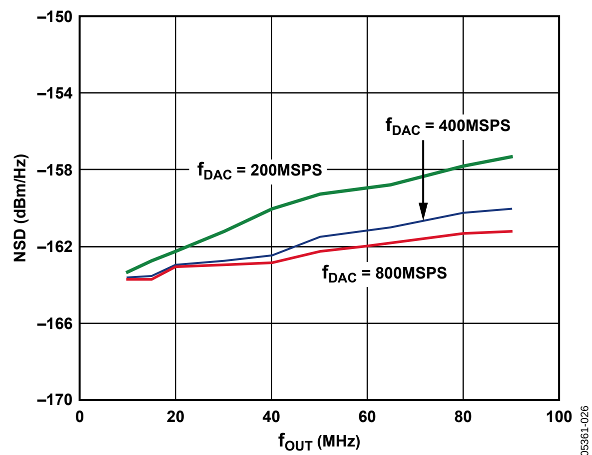


Figure 29. AD9779 Noise Spectral Density vs. f_{DAC}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

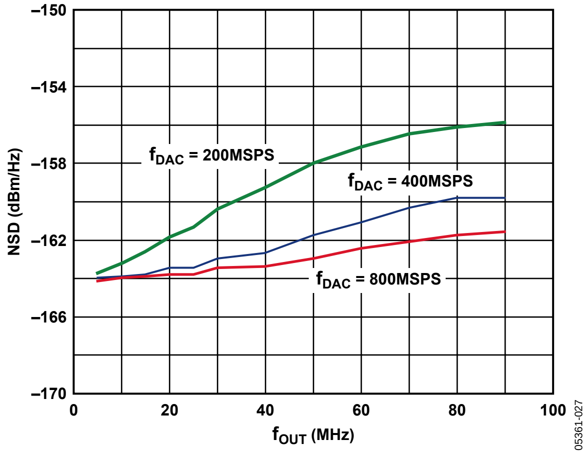


Figure 30. AD9779 Noise Spectral Density vs. f_{DAC}, Single-Tone Input at −6 dBFS

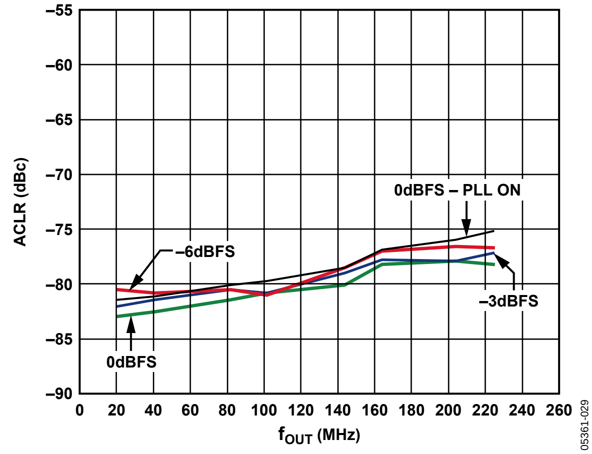


Figure 32. AD9779 ACLR for Second Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS. On-Chip Modulation Translates Baseband Signal to IF

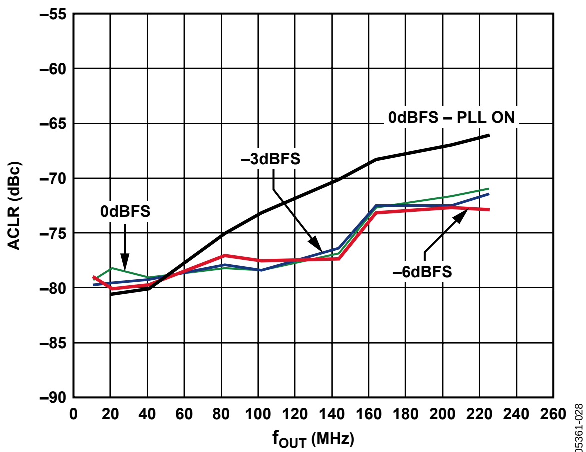


Figure 31. AD9779 ACLR for First Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

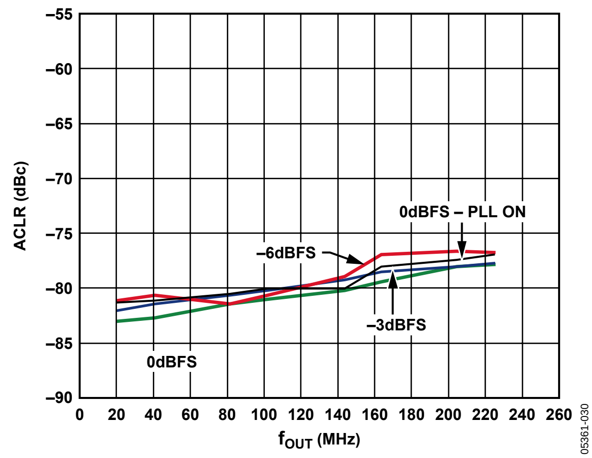


Figure 33. AD9779 ACLR for Third Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

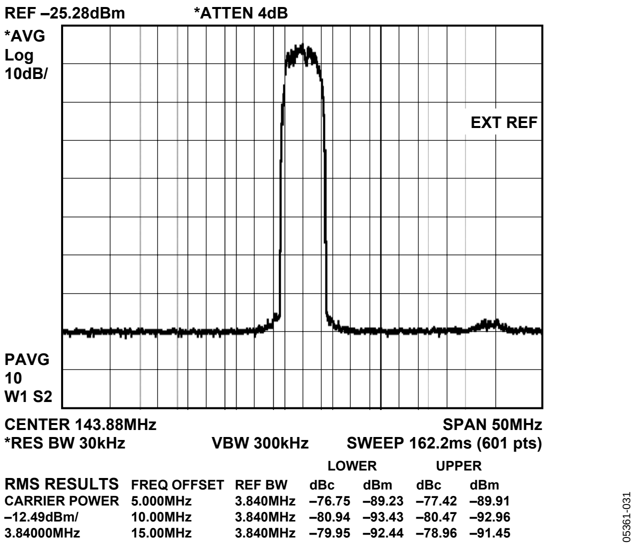


Figure 34. AD9779 WCDMA Signal, 4× Interpolation, f_{DATA} =122.88 MSPS, f_{DAC}/4 Modulation

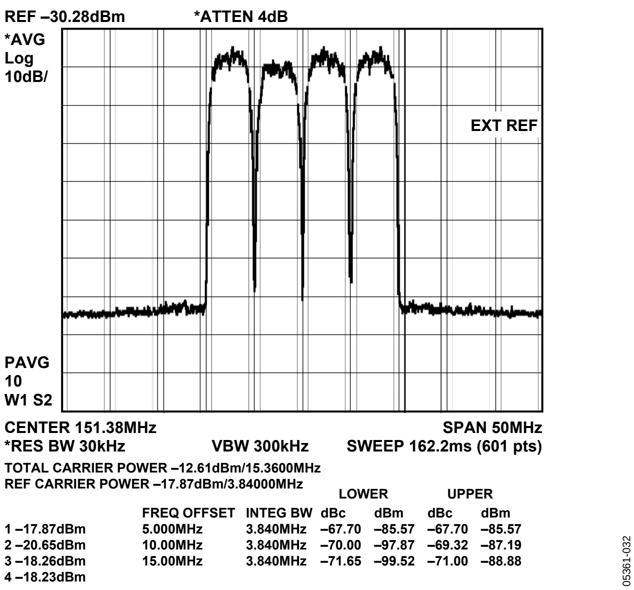


Figure 35. AD9779 Multicarrier WCDMA Signal, 4× Interpolation, f_{DAC} =122.88 MSPS, f_{DAC}/4 Modulation

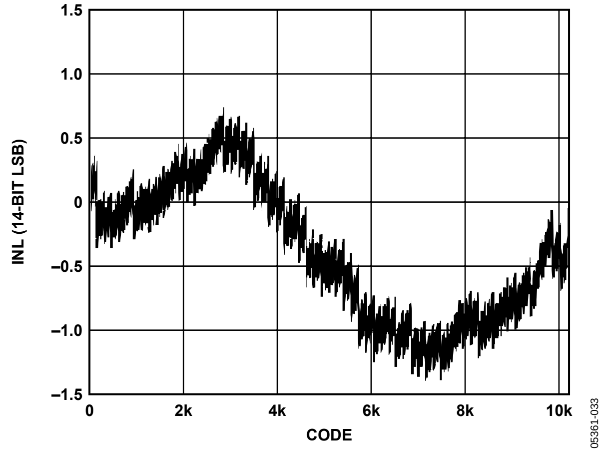


Figure 36. AD9778 Typical INL

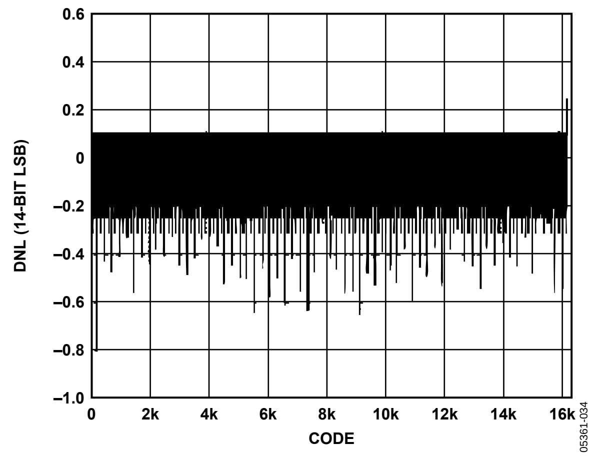


Figure 37. AD9778 Typical DNL

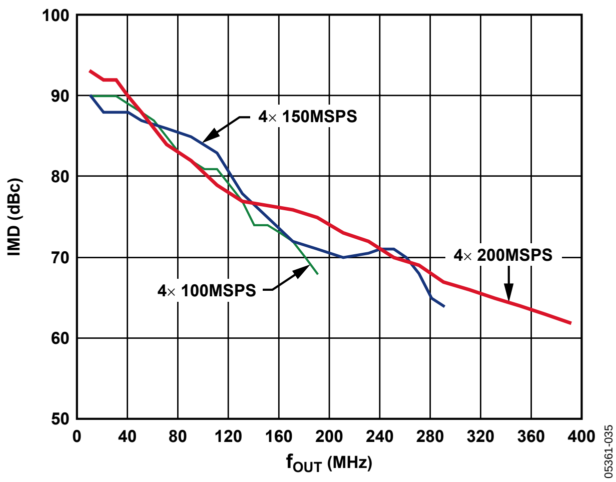


Figure 38. AD9778 IMD, 4× Interpolation

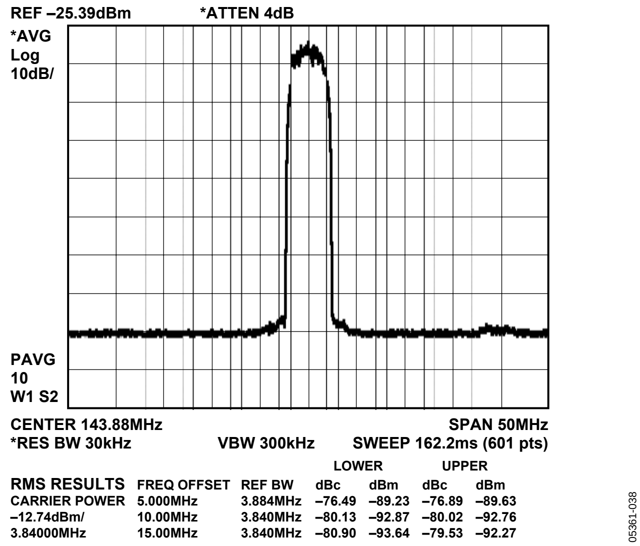


Figure 41. AD9778 ACLR, f_{DATA} = 122.88 MSPS, 4× Interpolation, f_{DAC}/4 Modulation

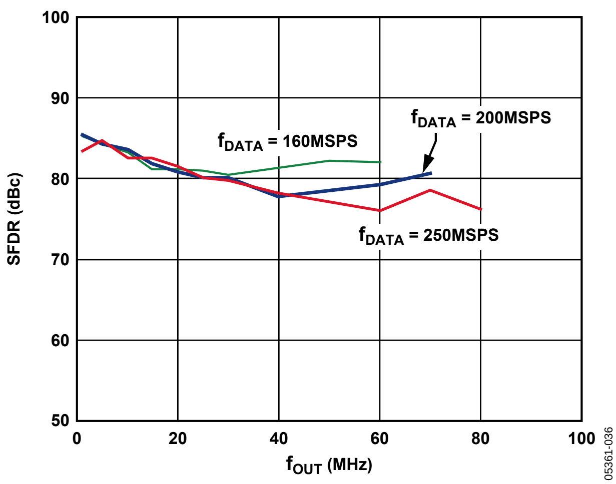


Figure 39. AD9778 In-Band SFDR, 2× Interpolation

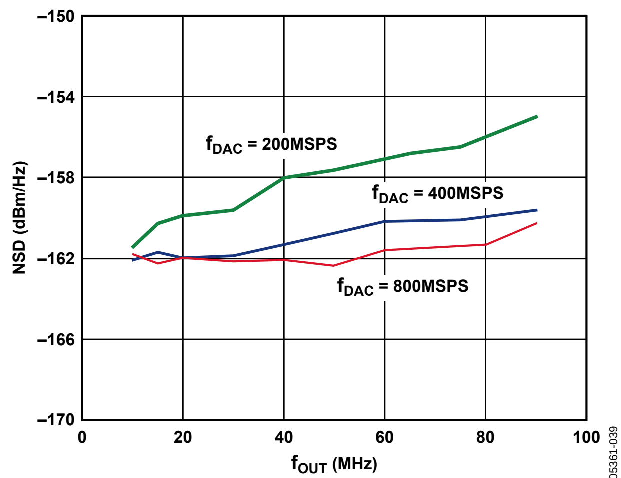


Figure 42. AD9778 Noise Spectral Density vs. f_{DAC} Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

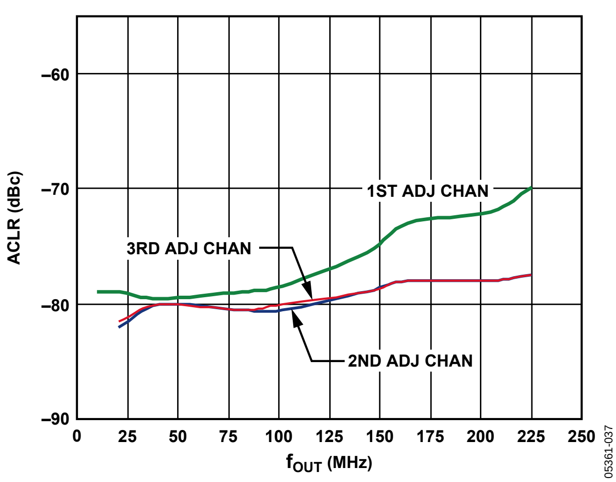


Figure 40. AD9778 ACLR, Single-Carrier WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS

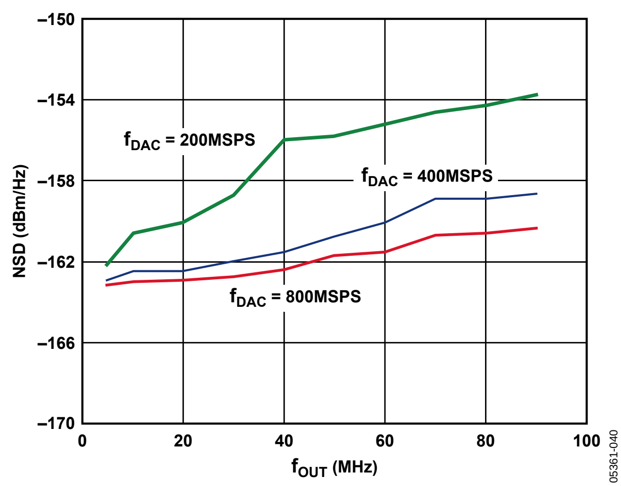


Figure 43. AD9778 Noise Spectral Density vs. f_{DAC} Single-Tone Input at –6 dBFS, f_{DATA} = 200 MSPS

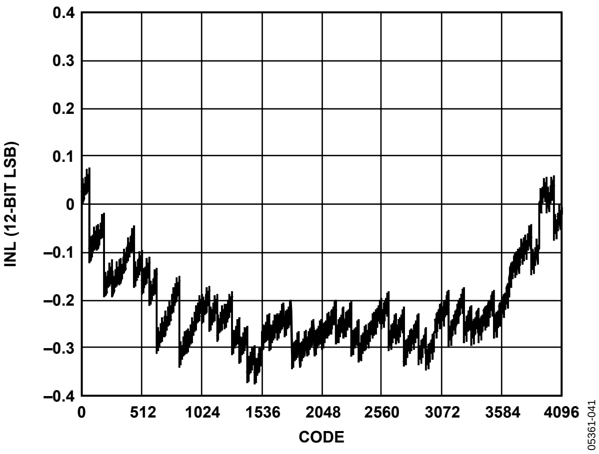


Figure 44. AD9776 Typical INL

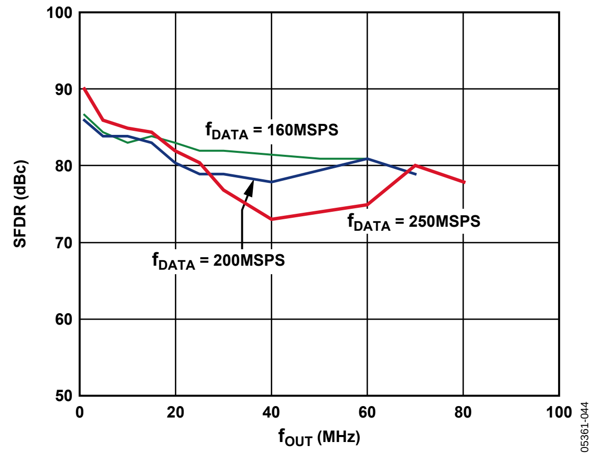


Figure 47. AD9776 In-Band SFDR, 2× Interpolation

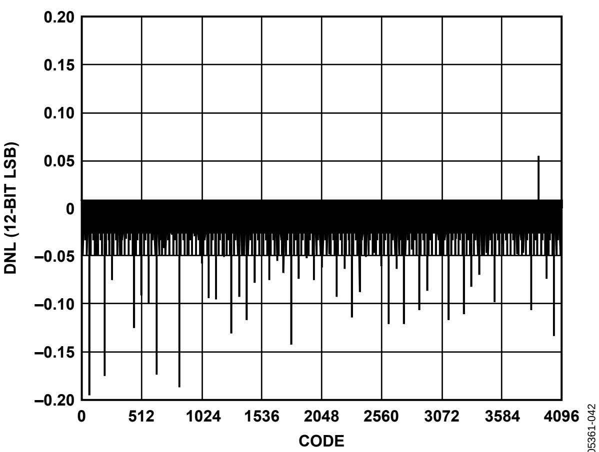


Figure 45. AD9776 Typical DNL

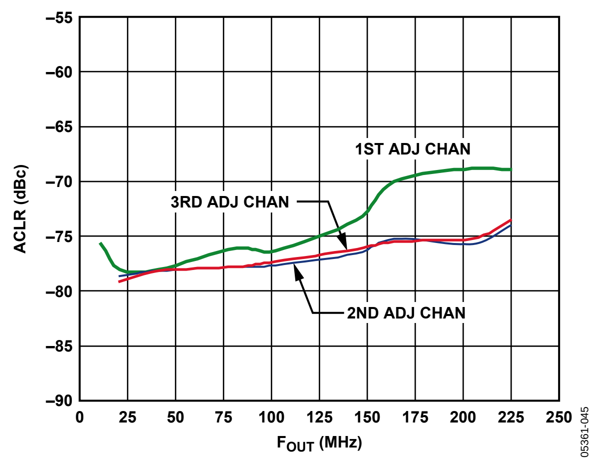


Figure 48. AD9776 ACLR, f_{DATA} = 122.88 MSPS, 4× Interpolation, f_{DAC}/4 Modulation

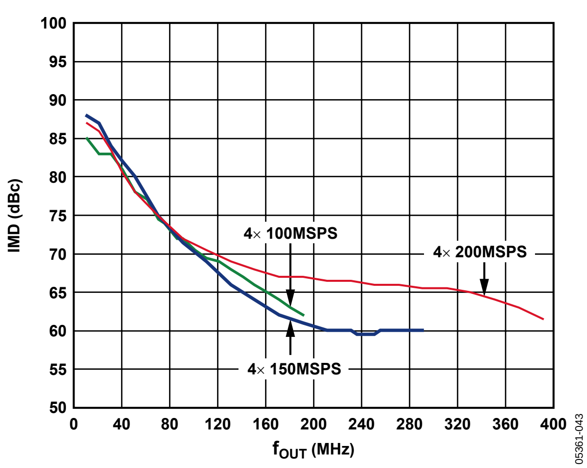


Figure 46. AD9776 IMD, 4× Interpolation

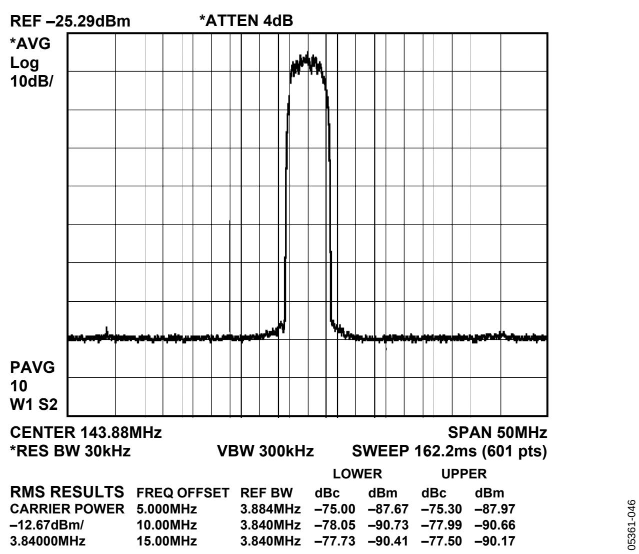


Figure 49. AD9776, Single Carrier WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS

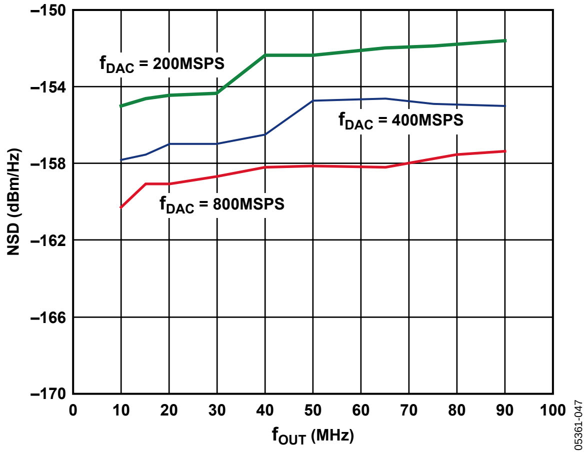


Figure 50. AD9776 Noise Spectral Density vs. f_{DAC}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

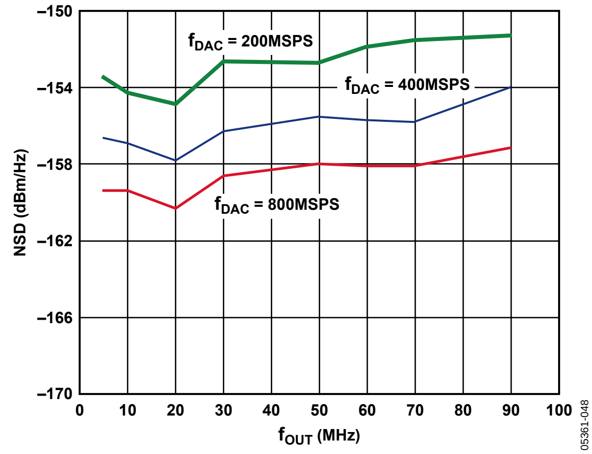


Figure 51. AD9776 Noise Spectral Density vs. f_{DAC}, Single-Tone Input at –6 dBFS, f_{DATA} = 200 MSPS

TERMINOLOGY

Integral Nonlinearity (INL)

INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error

The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1.

Gain Error

The difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range

The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)

The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time

The time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

In-Band Spurious Free Dynamic Range (SFDR)

The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Out-of-Band Spurious Free Dynamic Range (SFDR)

The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the band that starts at the frequency of the input data rate and ends at the Nyquist frequency of the DAC output sample rate. Normally, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths to the DAC output.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter

If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)

The ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection

In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9776/AD9778/AD9779 combine many features that make them very attractive DACs for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface with common quadrature modulators when designing single sideband transmitters. The speed and performance of the parts allow wider bandwidths and more carriers to be synthesized than in previously available DACs. The digital engine uses a breakthrough filter architecture that combines the interpolation with a digital quadrature modulator. This allows the parts to conduct digital quadrature frequency upconversion. They also have features that allow simplified synchronization with incoming data and between multiple parts.

The serial port configuration is controlled by Register 0x00, Bits<6:7>. It is important to note that the configuration changes immediately upon writing to the last bit of the byte. For multibyte transfers, writing to this register can occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the software reset, RESET (Register 0x00, Bit 5) or pulling the RESET pin (Pin 70) high. All registers are set to their default values, except Register 0x00 and Register 0x04, which remain unchanged.

Use of only single-byte transfers when changing serial port configurations or initiating a software reset is recommended to prevent unexpected device behavior.

As described in this section, all serial port data is transferred to/from the device in synchronization to the SCLK pin. If synchronization is lost, the device has the ability to asynchronously terminate an I/O operation, putting the serial port controller into a known state and, thereby, regaining synchronization.

SERIAL PERIPHERAL INTERFACE

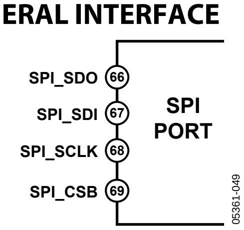


Figure 52. SPI Port

The serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9776/AD9778/AD9779. Single or multiple byte transfers are supported, as well as MSB-first or LSB-first transfer formats. The serial interface ports can be configured as a single pin I/O (SDIO) or two unidirectional pins for input/output (SDIO/SDO).

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD977x. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A logic high on the CSB pin followed by a logic low resets the SPI port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation, regardless of the state of the internal registers or the other signal levels at the inputs to the SPI port. If the SPI port is in an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one, two, three, or four data bytes as determined by the instruction byte. Using one multibyte transfer is preferred. Single-byte data transfers are useful in reducing CPU overhead when register access requires only one byte. Registers change immediately upon writing to the last bit of each transfer byte.

Instruction Byte

The instruction byte contains the information shown in Table 9.

Table 9. SPI Instruction Byte

MSB **LSB**

I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation.

N1 and N0, Bit 6 and Bit 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are listed in Table 10.

A4, A3, A2, A1, and A0—Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0, respectively, of the instruction byte determine the register that is accessed during the data transfer portion of the communication cycle.

For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the device based on the LSB-first bit (Register 0x00, Bit 6).

Table 10. Byte Transfer Count

N1	N0	Description
0	0	Transfer one byte
0	1	Transfer three bytes
1	0	Transfer two bytes
1	1	Transfer four bytes

Serial Interface Port Pin Descriptions

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and to run the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select (CSB)

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

Serial Data I/O (SDIO)

Data is always written into the device on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, configuring the SDIO pin as unidirectional.

Serial Data Out (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the device operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB TRANSFERS

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by Register Bit LSB_FIRST (Register 0x00, Bit 6). The default is MSB-first (LSB-first = 0).

When LSB-first = 0 (MSB-first) the instruction and data bit must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow from high address to low address. In MSB-first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSB-first = 1 (LSB-first) the instruction and data bit must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB-first mode is active. The serial port controller address increments from the data address written toward 0x1F for multibyte I/O operations if the LSB-first mode is active.

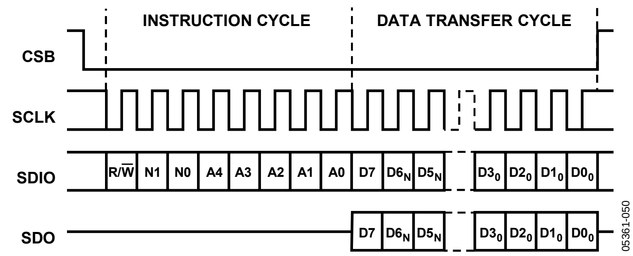


Figure 53. Serial Register Interface Timing MSB-First

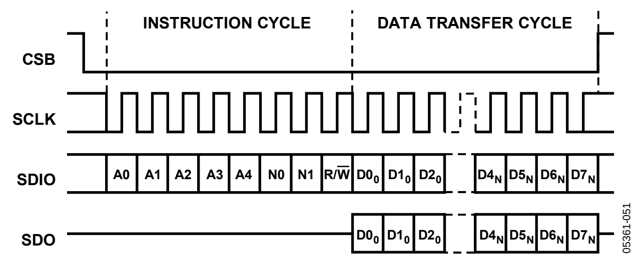


Figure 54. Serial Register Interface Timing LSB-First

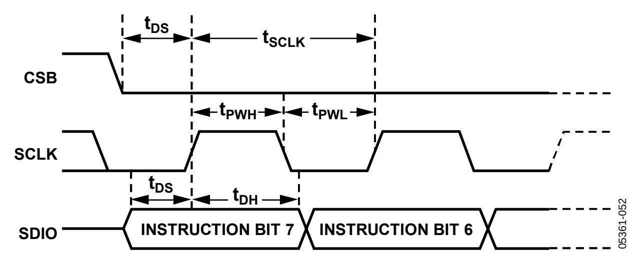


Figure 55. Timing Diagram for SPI Register Write

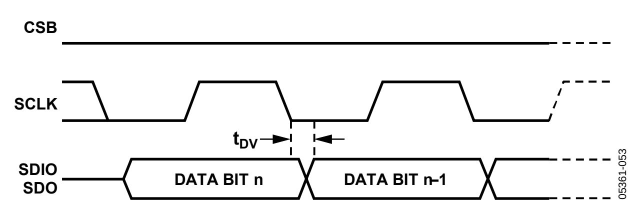


Figure 56. Timing Diagram for SPI Register Read

SPI REGISTER MAP

Table 11.

Register Name	Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Comm	0x00	00	SDIO Bidirectional	LSB/MSB First	Software Reset	Power-Down Mode	Auto Power-Down Enable		PLL Lock Indicator (Read Only)		0x00
Digital Control	0x01	01	Filter Interpolation Factor<1:0>		Filter Modulation Mode<3:0>					Zero Stuffing Enable	0x00
	0x02	02	Data Format	Dual/Interleaved Data Bus Mode	Real Mode	Data Clock Delay Enable	Inverse Sinc Enable	DATACLK Invert	TxEnable Invert	Q First	0x00
Sync Control	0x03	03	Data Clock Delay Mode<1:0>		Data Clock Divide Ratio<1:0>		Reserved				0x00
	0x04	04	Data Clock Delay<3:0>				Output Sync Pulse Divide<2:0>			Sync Out Delay<4>	0x00
	0x05	05	Sync Out Delay<3:0>				Input Sync Pulse Frequency Ratio<2:0>			Sync Input Delay<4>	0x00
	0x06	06	Sync Input Delay<3:0>				Input Sync Pulse Timing Error Tolerance<3:0>				0x00
	0x07	07	Sync Receiver Enable	Sync Driver Enable	Sync Triggering Edge	DAC Clock Offset<4:0>					0x00
PLL Control	0x08	08	PLL Band Select<5:0>						PLL VCO AGC Gain<1:0>		0xCF
	0x09	09	PLL Enable	PLL VCO Divider Ratio<1:0>		PLL Loop Divide Ratio<1:0>		PLL Bias Setting<2:0>			0x37
Misc Control	0x0A	10	PLL Control Voltage Range<2:0> (Read Only)			PLL Loop Bandwidth Adjustment<4:0>					0x38
I DAC Control Register	0x0B	11	I DAC Gain Adjustment<7:0>								0xF9
	0x0C	12	I DAC Sleep	I DAC Power Down					I DAC Gain Adjustment<9:8>		0x01
Aux DAC1 Control Register	0x0D	13	Auxiliary DAC1 Data<7:0>								0x00
	0x0E	14	Auxiliary DAC1 Sign	Auxiliary DAC1 Current Direction	Auxiliary DAC1 Power-Down				Auxiliary DAC1 Data<9:8>		0x00
Q DAC Control Register	0x0F	15	Q DAC Gain Adjustment<7:0>								0xF9
	0x10	16	Q DAC Sleep	Q DAC Power-Down					Q DAC Gain Adjustment<9:8>		0x01
Aux DAC2 Control Register	0x11	17	Auxiliary DAC2 Data<7:0>								0x00
	0x12	18	Auxiliary DAC2 Sign	Auxiliary DAC2 Current Direction	Auxiliary DAC2 Power-Down				Auxiliary DAC2 Data<9:8>		0x00
	0x13 to 0x18	19 to 24	Reserved								
Interrupt Register	0x19	25		Sync Delay IRQ				Sync Delay IRQ Enable		Internal Sync Loopback	0x00
	0x1A to 0x1F	26 to 31	Reserved								

Table 12. SPI Register Description

	Address				
Register Name	**Reg. No.**	**Bits**	**Description**	**Function**	**Default**
Comm Register	00	7	SDIO bidirectional	0: use SDIO pin as input data only	0
				1: use SDIO as both input and output data	
	00	6	LSB/MSB first	0: first bit of serial data is MSB of data byte	0
				1: first bit of serial data is LSB of data byte	
	00	5	Software reset	Bit must be written with a 1, then 0 to soft reset SPI register map	0
	00	4	Power-down mode	0: all circuitry is active	
				1: disable all digital and analog circuitry, only SPI port is active	
	00	3	Auto power-down enable	Controls auto power-down mode, see the Power-Down and Sleep Modes section	0
	00	1	PLL lock (read only)	0: PLL is not locked	
				1: PLL is locked	0
Digital Control Register	01	7:6	Filter interpolation factor	00: 1× interpolation	00
				01: 2× interpolation	
				10: 4× interpolation	
				11: 8× interpolation	
	01	5:2	Filter modulation mode	See Table 21 for filter modes	0000
	01	0	Zero stuffing	0: zero stuffing off	0
				1: zero stuffing on	
	02	7	Data format	0: signed binary	0
				1: unsigned binary	
	02	6	Dual/interleaved data bus mode	0: both input data ports receive data	0
				1: Data Port 1 only receives data	
	02	5	Real mode	0: enable Q path for signal processing	0
				1: disable Q path data (internal Q channel clocks disabled, I and Q modulators disabled)	
	02	4	DATACLK delay enable	See the Using Data Delay to Meet Timing Requirements section.	
	02	3	Inverse sinc enable	0: inverse sinc filter disabled	0
				1: inverse sinc filter enabled	
	02	2	DATACLK invert	0: output DATACLK same phase as internal capture clock	0
				1: output DATACLK opposite phase as internal capture clock	
	02	1	TxEnable invert	Inverts the function of TxEnable Pin 39, see the Interleaved Data Mode section	0
	02	0	Q first	0: first byte of data is always I data at beginning of transmit	
				1: first byte of data is always Q data at beginning of transmit	
Sync Control Register	03	7:6	Data clock delay mode	00: manual	00
	03	5:4	Extra data clock divide ratio	Data clock output divider (see Table 22 for divider ratio)	00
	03	3:0	Reserved		000
	04	7:4	Data clock delay	Sets delay of REFCLK in to DATACLK out	0000
	04	3:1	Output sync pulse divide	Sets frequency of SYNC_O pulses	000
	04	0	Sync out delay	Sync output delay, Bit 4	
	05	7:4	Sync out delay	Sync output delay, Bits<3:0>	0
	05	3:1	Input sync pulse frequency	Input sync pulse frequency divider, see the AN-822 application note	000
	05	0	Sync input delay	Sync input delay, Bit 4	0

Register Name	Address		Description	Function	Default
	Reg. No.	Bits			
Sync Control Register	06	7:4	Sync input delay	See the Multiple DAC Synchronization section for details on using these registers to synchronize multiple DACs	0
	06	3:0	Input sync pulse timing error tolerance		0
	07	7	Sync receiver enable		0
	07	6	Sync driver enable		0
	07	5	Sync triggering edge		0
	07	4:0	SYNC_I to input data sampling clock offset		0
PLL Control	08	7:2	PLL band select	VCO frequency range vs. PLL band select value (see Table 18)	111001
	08	1:0	VCO AGC gain control	Lower number (low gain) is generally better for performance	11
	09	7	PLL enable	0: PLL off, DAC rate clock supplied by outside source 1: PLL on, DAC rate clock synthesized internally from external reference clock via PLL clock multiplier	0
	09	6:5	PLL VCO divide ratio	F_{VCO}/f_{DAC} 00 × 1 01 × 2 10 × 4 11 × 8	
	09	4:3	PLL loop divide ratio	f_{DAC}/f_{REF} 00 × 2 01 × 4 10 × 8 11 × 16	
	09	2:0	PLL bias setting	Always set to 010	010
Misc Control	0A	7:5	PLL control voltage range	000 to 111, proportional to voltage at PLL loop filter output, readback only	
	0A	4:0	PLL loop bandwidth adjustment	See PLL Loop Filter Bandwidth section for details	
I DAC Control Register	0B	7:0	I DAC gain adjustment	(7:0) LSB slice of 10-bit gain setting word for I DAC	11111001
	0C	7	I DAC sleep	0: I DAC on 1: I DAC off	0
	0C	6	I DAC power-down	0: I DAC on 1: I DAC off	0
	0C	1:0	I DAC gain adjustment	(9:8) MSB slice of 10-bit gain setting word for I DAC	01
Aux DAC1 Control Register	0D	7:0	Aux DAC1 gain adjustment	(7:0) LSB slice of 10-bit gain setting word for Aux DAC1	00000000
	0E	7	Aux DAC1 sign	0: positive 1: negative	
	0E	6	Aux DAC1 current direction	0: source 1: sink	0
	0E	5	Aux DAC1 power-down	0: Aux DAC1 on 1: Aux DAC1 off	0
	0E	1:0	Aux DAC1 gain adjustment	(9:8) MSB slice of 10-bit gain setting word for Aux DAC1	00

Register Name	Address		Description	Function	Default
	Reg. No.	Bits			
Q DAC Control Register	0F	7:0	Q DAC gain adjustment	(7:0) LSB slice of 10-bit gain setting word for Q DAC	11111001
	10	7	Q DAC sleep	0: Q DAC on	0
				1: Q DAC off	
	10	6	Q DAC power-down	0: Q DAC on	0
				1: Q DAC off	
	10	1:0	Q DAC gain adjustment	(9:8) MSB slice of 10-bit gain setting word for Q DAC	
Aux DAC2 Control Register	11	7:0	Aux DAC2 gain adjustment	(7:0) LSB slice of 10-bit gain setting word for Aux DAC2	00000000
	12	7	Aux DAC2 sign	0: positive	
				1: negative	
	12	6	Aux DAC2 current direction	0: source	0
				1: sink	
	12	5	Aux DAC2 power-down	0: Aux DAC2 on	0
				1: Aux DAC2 off	
	12	1:0	Aux DAC2 gain adjustment	(9:8) MSB slice of 10-bit gain setting word for Aux DAC2	00
Interrupt Register	19	7			0
	19	6	Sync delay IRQ	Readback, must write 0 to clear	0
	19	5			0
	19	3			0
	19	2	Sync delay IRQ enable		0
	19	1			0
	19	0	Internal sync loopback		0

INTERPOLATION FILTER ARCHITECTURE

The AD9776/AD9778/AD9779 can provide up to 8× interpolation, or the interpolation filters can be entirely disabled. It is important to note that the input signal should be backed off by approximately 0.01 dB from full scale to avoid overflowing the interpolation filters. The coefficients of the low-pass filters and the inverse sinc filter are given in Table 13, Table 14, Table 15, and Table 16. Spectral plots for the filter responses are shown in Figure 57, Figure 58, and Figure 59.

Table 13. Half-Band Filter 1

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(55)	−4
H(2)	H(54)	0
H(3)	H(53)	+13
H(4)	H(52)	0
H(5)	H(51)	−34
H(6)	H(50)	0
H(7)	H(49)	+72
H(8)	H(48)	0
H(9)	H(47)	−138
H(10)	H(46)	0
H(11)	H(45)	+245
H(12)	H(44)	0
H(13)	H(43)	−408
H(14)	H(42)	0
H(15)	H(41)	+650
H(16)	H(40)	0
H(17)	H(39)	−1003
H(18)	H(38)	0
H(19)	H(37)	+1521
H(20)	H(36)	0
H(21)	H(35)	−2315
H(22)	H(34)	0
H(23)	H(33)	+3671
H(24)	H(32)	0
H(25)	H(31)	−6642
H(26)	H(30)	0
H(27)	H(29)	+20,755
H(28)		+32,768

Table 14. Half-Band Filter 2

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	−2
H(2)	H(22)	0
H(3)	H(21)	+17
H(4)	H(20)	0
H(5)	H(19)	−75
H(6)	H(18)	0
H(7)	H(17)	+238
H(8)	H(16)	0
H(9)	H(15)	−660
H(10)	H(14)	0
H(11)	H(13)	+2530
H(12)		+4096

Table 15. Half-Band Filter 3

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(15)	−39
H(2)	H(14)	0
H(3)	H(13)	+273
H(4)	H(12)	0
H(5)	H(11)	−1102
H(6)	H(10)	0
H(7)	H(9)	+4964
H(8)		+8192

Table 16. Inverse Sinc Filter

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(9)	+2
H(2)	H(8)	−4
H(3)	H(7)	+10
H(4)	H(6)	−35
H(5)		+401

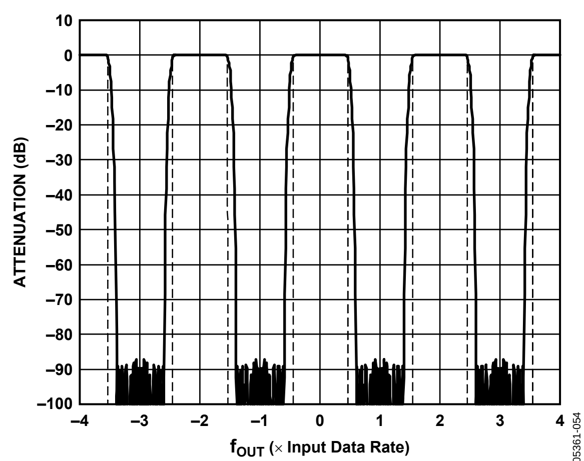


Figure 57. 2× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

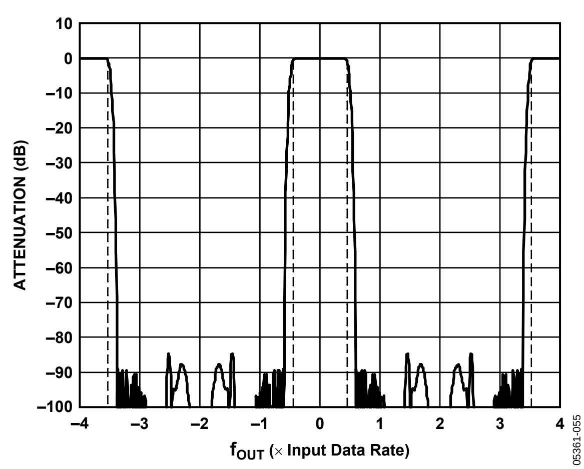


Figure 58. 4× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

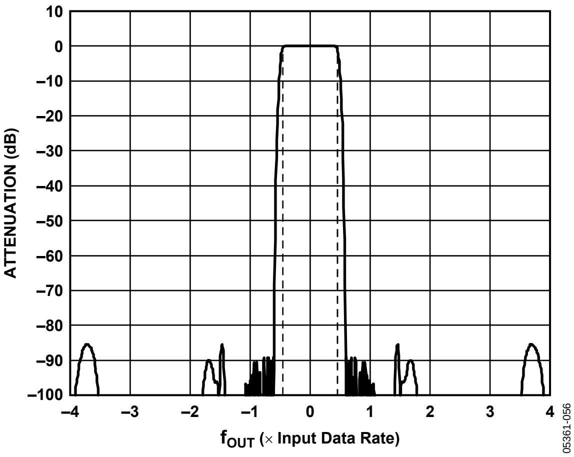


Figure 59. 8× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

With the interpolation filter and modulator combined, the incoming signal can be placed anywhere within the Nyquist region of the DAC output sample rate. When the input signal is complex, this architecture allows modulation of the input signal to positive or negative Nyquist regions (see Table 17).

The Nyquist regions of up to 4× the input data rate can be seen in Figure 60.

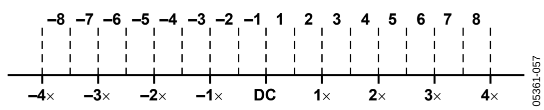


Figure 60. Nyquist Zones

Figure 57, Figure 58, and Figure 59 show the low-pass response of the digital filters with no modulation. By turning on the modulation feature, the response of the digital filters can be tuned to anywhere within the DAC bandwidth. As an example, Figure 61 to Figure 67 show the nonshifted mode filter responses (refer to Table 17 for shifted/nonshifted mode filter responses).

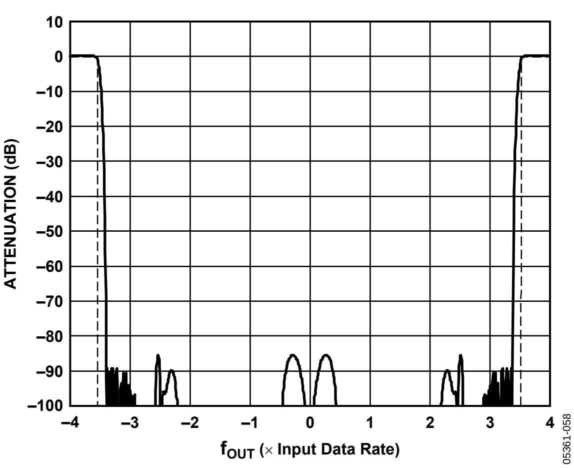


Figure 61. Interpolation/Modulation Combination of 4 f_{DAC}/8 Filter

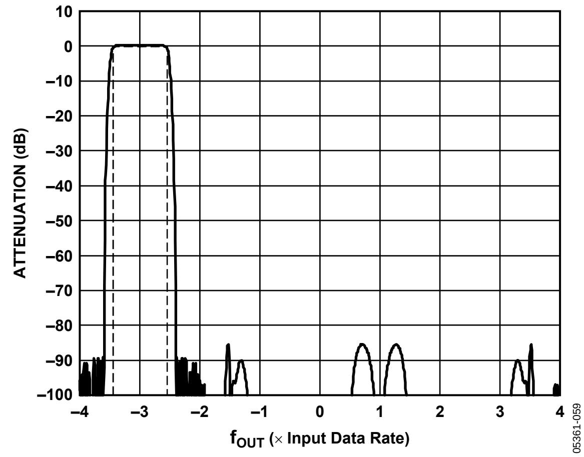


Figure 62. Interpolation/Modulation Combination of −3 f_{DAC}/8 Filter

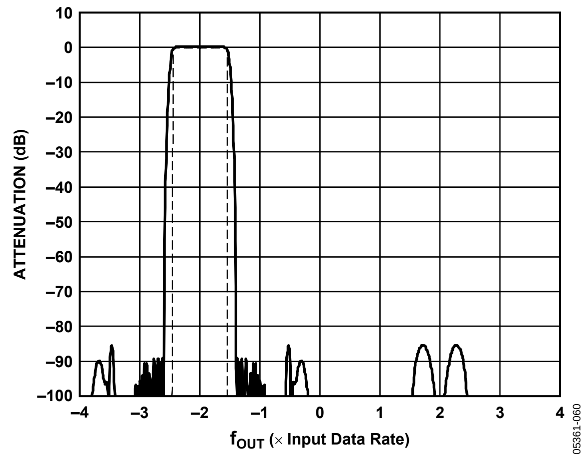


Figure 63. Interpolation/Modulation Combination of −2 f_{DAC}/8 Filter

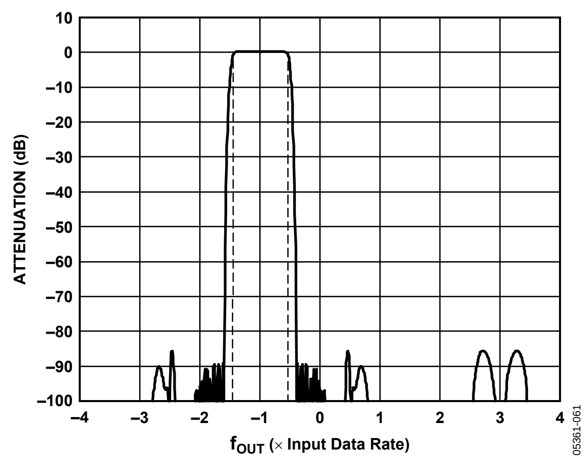


Figure 64. Interpolation/Modulation Combination of −1 f_{DAC}/8 Filter

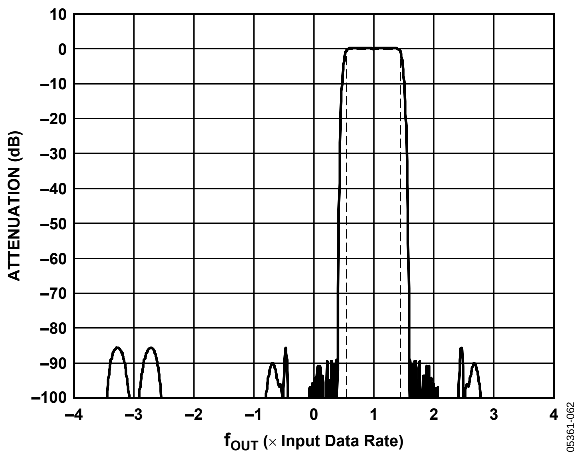


Figure 65. Interpolation/Modulation Combination of f_{DAC}/8 Filter

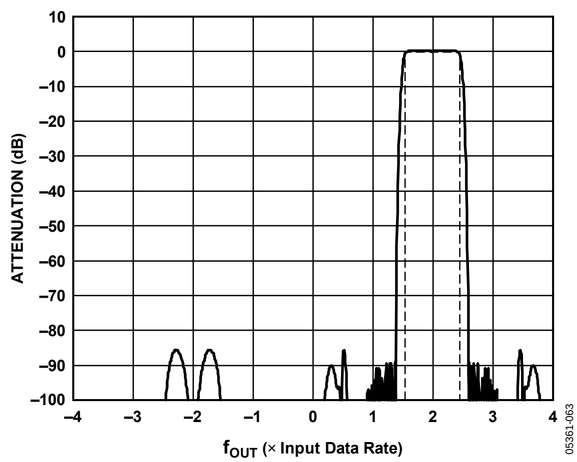


Figure 66. Interpolation/Modulation Combination of 2 f_{DAC}/8 Filter in Shifted Mode

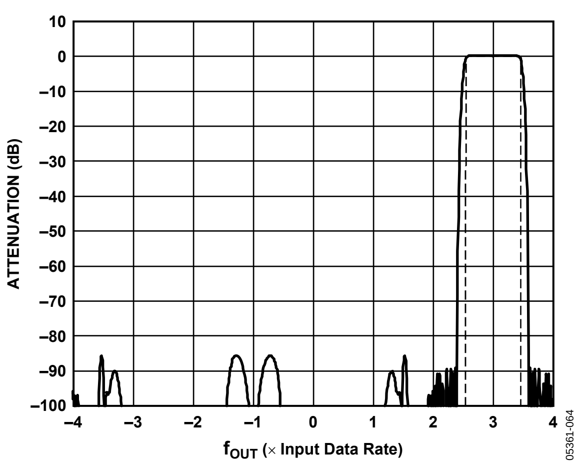


Figure 67. Interpolation/Modulation Combination of 3 f_{DAC}/8 Filter in Shifted Mode

Shifted mode filter responses allow the pass band to be centered around ±0.5 f_{DATA}, ±1.5 f_{DATA}, ±2.5 f_{DATA}, and ±3.5 f_{DATA}. Switching to the shifted mode response does not modulate the signal. Instead, the pass band is simply shifted. For example, picture the response shown in Figure 67 and assume the signal in-band is a complex signal over the bandwidth 3.2 f_{DATA} to 3.3 f_{DATA}. If the even mode filter response is then selected, the pass band becomes centered at 3.5 f_{DATA}. However, the signal remains at the same place in the spectrum. The shifted mode capability allows the filter pass band to be placed anywhere in the DAC Nyquist bandwidth.

The AD9776/AD9778/AD9779 are dual DACs with internal complex modulators built into the interpolating filter response. In dual channel mode, the devices expect the real and the imaginary components of a complex signal at Digital Input Port 1 and Digital Input Port 2 (I and Q, respectively). The DAC outputs then represent the real and imaginary components of the input signal, modulated by the complex carrier f_{DAC}/2, f_{DAC}/4, or f_{DAC}/8.

With Register 2, Bit 6 set, the device accepts interleaved data on Port 1 in the I, Q, I, Q . . . sequence. Note that in interleaved mode, the channel data rate at the beginning of the I and the Q data paths are now half the input data rate because of the interleaving. The maximum input data rate is still subject to the maximum specification of the device. This limits the synthesis bandwidth available at the input in interleaved mode.

With Register 0x02, Bit 5 (real mode) set, the Q channel and the internal I and Q digital modulation are turned off. The output spectrum at the I DAC then represents the signal at Digital Input Port 1, interpolated by 1×, 2×, 4×, or 8×.

The general recommendation is that if the desired signal is within ±0.4 × f_{DATA}, the odd filter mode should be used. Outside of this, the even filter mode should be used. In any situation, the total bandwidth of the signal should be less than 0.8 × f_{DATA}.

Table 17. Interpolation Filter Modes, (Register 0x01, Bits<5:2>)

Interpolation Factor <7:6>	Filter Mode <5:2>	Modulation	Nyquist Zone Pass Band	F_Low[1]	Center[1]	F_High[1]	Comments
8	0x00	DC	1	−0.05	0	+0.05	In 8× interpolation; BW (min) = 0.0375 × f_{DAC} BW (max) = 0.1 × f_{DAC}
8	0x01	DC shifted	2	0.0125	0.0625	0.1125	
8	0x02	F/8	3	0.075	0.125	0.175	
8	0x03	F/8 shifted	4	0.1375	0.1875	0.2375	
8	0x04	F/4	5	0.2	0.25	0.3	
8	0x05	F/4 shifted	6	0.2625	0.3125	0.3625	
8	0x06	3F/8	7	0.325	0.375	0.425	
8	0x07	3F/8 shifted	8	0.3875	0.4375	0.4875	
8	0x08	F/2	−8	−0.55	−0.5	−0.45	
8	0x09	F/2 shifted	−7	−0.4875	−0.4375	−0.3875	
8	0x0A	−3F/8	−6	−0.425	−0.375	−0.343	
8	0x0B	−3F/8 shifted	−5	−0.3625	−0.3125	−0.2625	
8	0x0C	−F/4	−4	−0.3	−0.25	−0.2	
8	0x0D	−F/4 shifted	−3	−0.2375	−0.1875	−0.1375	
8	0x0E	−F/8	−2	−0.175	−0.125	−0.075	
8	0x0F	−F/8 shifted	−1	−0.1125	−0.0625	−0.0125	
4	0x00	DC	1	−0.1	0	+0.1	In 4× interpolation; BW (min) = 0.075 × f_{DAC} BW (max) = 0.2 × f_{DAC}
4	0x01	DC shifted	2	0.025	0.125	0.225	
4	0x02	F/4	3	0.15	0.25	0.35	
4	0x03	F/4 shifted	4	0.275	0.375	0.475	
4	0x04	F/2	−4	−0.6	−0.5	−0.4	
4	0x05	F/2 shifted	−3	−0.475	−0.375	−0.275	
4	0x06	−F/4	−2	−0.35	−0.25	−0.15	
4	0x07	−F/4 shifted	−1	−0.225	−0.125	−0.025	
2	0x00	DC	1	−0.2	0	+0.2	In 2× interpolation; BW (min) = 0.15 × f_{DAC} BW (max) = 0.4 × f_{DAC}
2	0x01	DC shifted	2	0.05	0.25	0.45	
2	0x02	F/2	−2	−0.7	−0.5	−0.3	
2	0x03	F/2 shifted	−1	−0.45	−0.25	−0.05	

[1] Frequency normalized to f_{DAC}.

INTERPOLATION FILTER MINIMUM AND MAXIMUM BANDWIDTH SPECIFICATIONS

The AD977x uses a novel interpolation filter architecture that allows DAC IF frequencies to be generated anywhere in the spectrum. Figure 68 shows the traditional choice of DAC IF output bandwidth placement. Note that there are no possible filter modes in which the carrier can be placed near 0.5 × f_{DATA}, 1.5 × f_{DATA}, 2.5 × f_{DATA}, and so on.

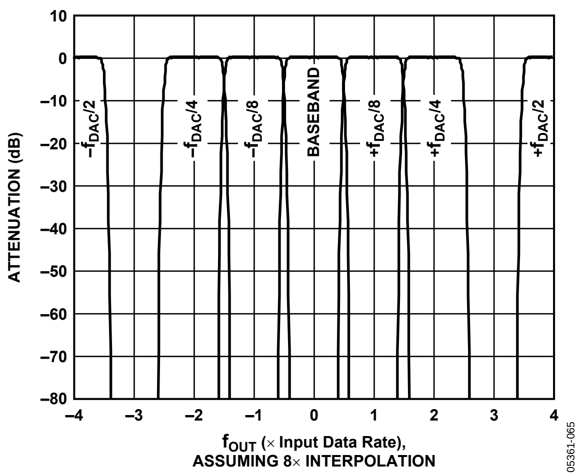


Figure 68. Traditional Bandwidth Options for TxDAC Output IF

The filter architecture not only allows the interpolation filter pass bands to be centered in the middle of the input Nyquist zones (as explained in this section), but also allows the possibility of a 3 × f_{DAC}/8 modulation mode. With all of these filter combinations, a carrier of given bandwidth can be placed anywhere in the spectrum and fall into a possible pass band of the interpolation filters. The possible bandwidths accessible with the filter architecture are shown in Figure 69 and Figure 70. Note that the shifted and nonshifted filter modes are all accessible by programming the filter mode for the particular interpolation rate.

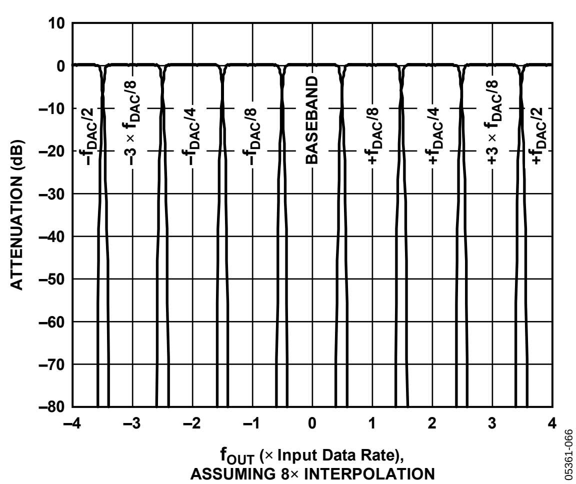


Figure 69. Nonshifted Bandwidths Accessible with the Filter Architecture

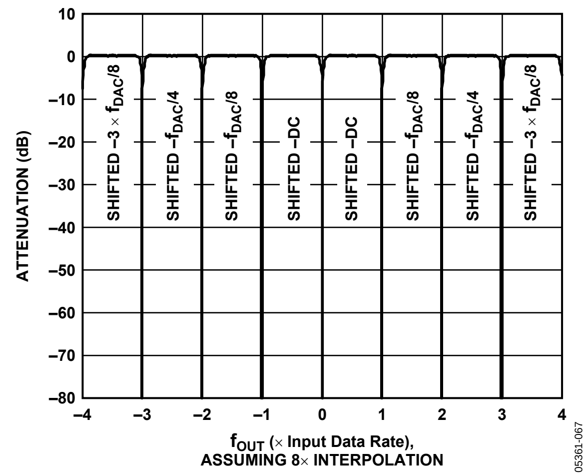


Figure 70. Shifted Bandwidths Accessible with the Filter Architecture

With this filter architecture, a signal placed anywhere in the spectrum is possible. However, the signal bandwidth is limited by the input sample rate of the DAC and the specific placement of the carrier in the spectrum. The bandwidth restriction resulting from the combination of filter response and input sample rate is often referred to as the synthesis bandwidth, since this is the largest bandwidth that the DAC can synthesize.

The maximum bandwidth condition exists if the carrier is placed directly in the center of one of the filter pass bands. In this case, the total 0.1 dB bandwidth of the interpolation filters is equal to 0.8 × f_{DATA}. As Table 17 shows, the synthesis bandwidth as a fraction of DAC output sample rate drops by a factor of 2 for every doubling of interpolation rate. The minimum bandwidth condition exists, for example, if a carrier is placed at 0.25 × f_{DATA}. In this situation, if the nonshifted filter response is enabled, the high end of the filter response cuts off at 0.4 × f_{DATA}, thus limiting the high end of the signal bandwidth. If the shifted filter response is enabled instead, then the low end of the filter response cuts off at 0.1 × f_{DATA}, thus limiting the low end of the signal bandwidth. The minimum bandwidth specification that applies for a carrier at 0.25 × f_{DATA} is therefore 0.3 × f_{DATA}. The minimum bandwidth behavior is repeated over the spectrum for carriers placed at (±*n* ± 0.25) × f_{DATA}, where *n* is any integer.

DRIVING THE REFCLK INPUT

The REFCLK input requires a low jitter differential drive signal. It is a PMOS input differential pair powered from the 1.8 V supply, therefore, it is important to maintain the specified 400 mV input common-mode voltage. Each input pin can safely swing from 200 mV p-p to 1 V p-p about the 400 mV common-mode voltage. While these input levels are not directly LVDS-compatible, REFCLK can be driven by an offset ac-coupled LVDS signal, as shown in Figure 71.

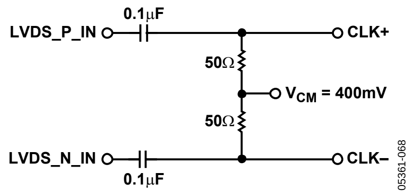


Figure 71. LVDS REFCLK Drive Circuit

If a clean sine clock is available, it can be transformer-coupled to REFCLK, as shown in Figure 71. Use of a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through a CMOS to LVDS translator, then ac-coupled, as described in this section. Alternatively, it can be transformer-coupled and clamped, as shown in Figure 72.

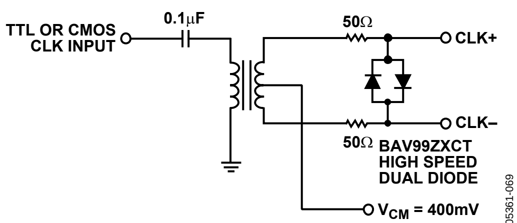


Figure 72. TTL or CMOS REFCLK Drive Circuit

A simple bias network for generating VCM is shown in Figure 73. It is important to use CVDD18 and CGND for the clock bias circuit. Any noise or other signal that is coupled onto the clock is multiplied by the DAC digital input signal and can degrade DAC performance.

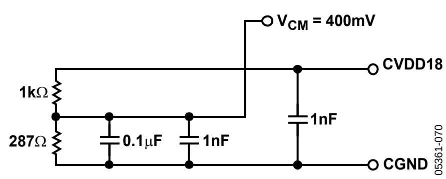


Figure 73. REFCLK VCM Generator Circuit

INTERNAL PLL CLOCK MULTIPLIER/CLOCK DISTRIBUTION

The internal clock structure on the devices allows the user to drive the differential clock inputs with a clock at 1× or an integer multiple of the input data rate or at the DAC output sample rate. An internal PLL provides input clock multiplication and provides all the internal clocks required for the interpolation filters and data synchronization.

The internal clock architecture is shown in Figure 74. The reference clock is the differential clock at Pin 5 and Pin 6. This clock input can be run differentially or singled-ended by driving Pin 5 with a clock signal and biasing Pin 6 to the midswing point of the signal at Pin 5. The clock architecture can be run in the following configurations:

PLL Enabled (Register 0x09, Bit 7 = 1)

The PLL enable switch shown in Figure 74 is connected to the junction of the N1 dividers (PLL VCO divide ratio) and N2 dividers (PLL loop divide ratio). Divider N3 determines the interpolation rate of the DAC, and the ratio N3/N2 determines the ratio of reference clock/input data rate. The VCO runs optimally over the range of 1.0 GHz to 2.0 GHz, so that N1 keeps the speed of the VCO within this range, although the DAC sample rate can be lower. The loop filter components are entirely internal and no external compensation is necessary.

PLL Disabled (Register 0x09, Bit 7 = 0)

The PLL enable switch shown in Figure 74 is connected to the reference clock input. The differential reference clock input is the same as the DAC output sample rate. N3 determines the interpolation rate.

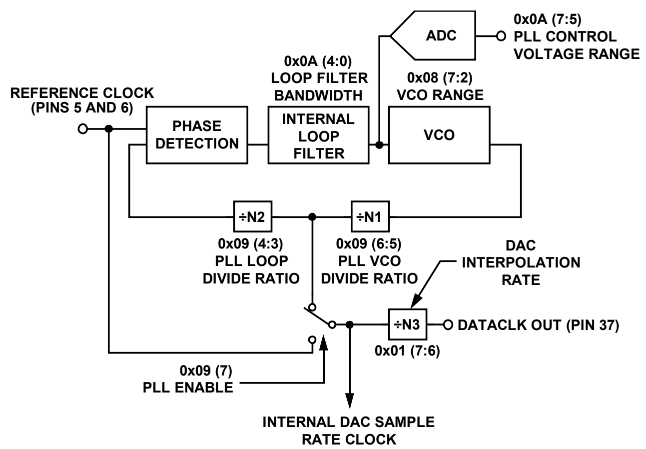


Figure 74. Internal Clock Architecture

Table 18. VCO Frequency Range vs. PLL Band Select Value

Typical PLL Lock Ranges				
PLL Band Select	VCO Frequency Range in MHz			
	Typ at 25°C		Typ over Temp	
	f_{LOW}	f_{HIGH}	f_{LOW}	f_{HIGH}
111111 (63)	Auto mode		Auto mode	
111110 (62)	2056	2170	2105	2138
111101 (61)	2002	2113	2048	2081
111100 (60)	1982	2093	2029	2061
111011 (59)	1964	2075	2010	2043
111010 58)	1947	2057	1992	2026
111001 (57)	1927	2037	1971	2006
111000 (56)	1907	2016	1951	1986
110111 (55)	1894	2003	1936	1972
110110 (54)	1872	1981	1913	1952
110101 (53)	1852	1960	1892	1931
110100 (52)	1841	1948	1881	1920
110011 (51)	1816	1923	1855	1895
110010 (50)	1796	1903	1835	1874
110001 (49)	1789	1895	1828	1867
110000 (48)	1764	1871	1803	1844
101111 (47)	1746	1853	1784	1826
101110 (46)	1738	1842	1776	1815
101101 (45)	1714	1820	1752	1794
101100 (44)	1700	1804	1737	1779
101011 (43)	1689	1790	1726	1764
101010 (42)	1657	1757	1695	1734
101001 (41)	1641	1738	1679	1714
101000 (40)	1610	1707	1649	1684
100111 (39)	1597	1689	1635	1666
100110 (38)	1568	1661	1607	1639
100101 (37)	1553	1641	1592	1617
100100 (36)	1525	1613	1562	1592
100011 (35)	1511	1595	1548	1572
100010 (34)	1484	1570	1519	1549
100001 (33)	1470	1552	1506	1528
100000 (32)	1441	1525	1474	1504
011111 (31)	1429	1509	1463	1487
011110 (30)	1403	1485	1433	1464
011101 (29)	1390	1469	1422	1447
011100 (28)	1362	1443	1391	1423
011011 (27)	1352	1429	1380	1407
011010 (26)	1325	1405	1352	1385
011001 (25)	1314	1390	1340	1369
011000 (24)	1290	1368	1315	1350
010111 (23)	1276	1351	1302	1332
010110 (22)	1253	1331	1277	1313
010101 (21)	1239	1313	1264	1295
010100 (20)	1183	1255	1205	1240
010011 (19)	1204	1275	1227	1259
010010 (18)	1151	1221	1172	1207
010001 (17)	1171	1240	1193	1224
010000 (16)	1148	1218	1170	1204
001111 (15)	1137	1204	1159	1189
001110 (14)	1116	1184	1137	1170
001101 (13)	1106	1171	1127	1157
001100 (12)	1086	1152	1106	1138
001011 (11)	1075	1138	1095	1124
001010 (10)	1055	1119	1075	1106
001001 (9)	1045	1107	1065	1093
001000 (8)	1027	1090	1047	1076
000111 (7)	1016	1076	1034	1062
000110 (6)	998	1059	1016	1046
000101 (5)	987	1046	1005	1032
000100 (4)	960	1017	977	1004
000011 (3)	933	989	949	976
000010 (2)	908	962	923	950
000001 (1)	883	936	898	925
000000 (0)	859	911	873	899

VCO Frequency Ranges

Because the PLL band covers greater than a 2× frequency range, there can be two options for the PLL band select: one at the low end of the range and one at the high end of the range. Under these conditions, the VCO phase noise is optimal when the user selects the band select value corresponding to the high end of the frequency range. Figure 75 shows how the VCO bandwidth and the optimal VCO frequency varies with the band select value.

VCO Frequency Ranges over Temperature

The specifications given over temperature in Table 18 are for a single part in a single lot. Part-to-part, and lot-to-lot, these specifications can exhibit a mean shift of several register settings. Systems should be designed to take this potential shift into account to maintain optimal PLL performance.

PLL Loop Filter Bandwidth

The loop filter bandwidth of the PLL is programmed via SPI Register 0x0A, Bits<4:0>. Changing these values switches capacitors on the internal loop filter. No external loop filter components are required. This loop filter has a pole at 0 (P1), and then a zero (Z1) pole (P2) combination. Z1 and P2 occur within a decade of each other. The location of the zero pole is determined by Bits<4:0>. For a setting of 00000, the zero pole occurs near 10 MHz. By setting Bits<4:0> to 11111, the Z1/P2 combination can be lowered to approximately 1 MHz. The relationship between Bits<4:0> and the position of the zero pole between 1 MHz and 10 MHz is linear. The internal components are not low tolerance, however, and can drift by as much as ±30%.

For optimal performance, the bandwidth adjustment (Register 0x0A, Bits<4:0>) should be set to 11111 for all operating modes with PLL enabled. The PLL bias settings

(Register 0x09, Bits<2:0>) should be set to 111. The PLL control voltage (Register 0x0A, Bits<7:5>) is read back and is proportional to the dc voltage at the internal loop filter output. With the PLL bias settings given in this section, the readback from the PLL control voltage should typically be 010, or possibly 001 or 011. Anything outside of this range indicates that the PLL is not operating correctly.

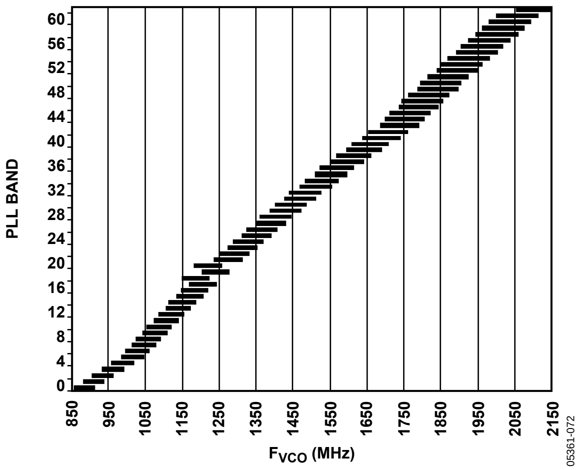


Figure 75. Typical PLL Band Select vs. Frequency at 25°C

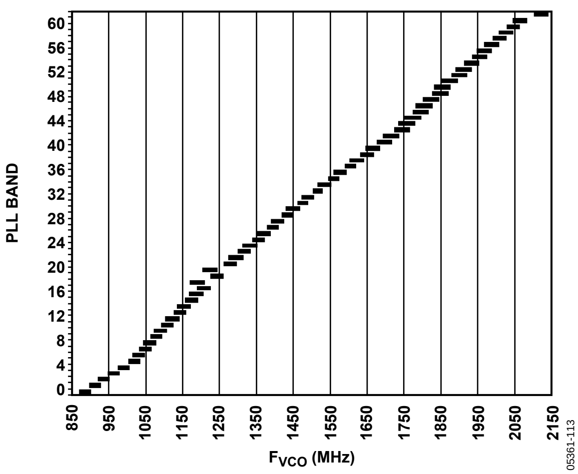


Figure 76. Typical PLL Band Select vs. Frequency over Temperature

The AD977x has an autosearch feature that determines the optimal settings for the PLL. To enable the autosearch mode, set Register 0x08, Bits<7:2> to 11111b, and read back the value from Register 0x08, Bits<7:2>. Autosearch mode is intended to find the optimal PLL settings only, after which the same settings should be applied in manual mode. It is not recommended that the PLL be set to autosearch mode during regular operation.

FULL-SCALE CURRENT GENERATION

Internal Reference

Full-scale current on the I DAC and Q DAC can be set from 8.66 mA to 31.66 mA. Initially, the 1.2 V band gap reference is used to set up a current in an external resistor connected to I120 (Pin 75). A simplified block diagram of the reference circuitry is shown in Figure 77. The recommended value for the external resistor is 10 kΩ, which sets up an $I_{REFERENCE}$ in the resistor of 120 μA, which in turn provides a DAC output full-scale current of 20 mA. Because the gain error is a linear function of this resistor, a high precision resistor improves gain matching to the internal matching specification of the devices. Internal current mirrors provide a current-gain scaling, where I DAC or Q DAC gain is a 10-bit word in the SPI port register (Register 0x0A, Register 0x0B, Register 0x0E, and Register 0x0F). The default value for the DAC gain registers gives an I_{FS} of approximately 20 mA, where I_{FS} is equal to

$$\frac{1.2\,V}{R}\times\left(\frac{27}{12}+\left(\frac{6}{1024}\times DAC\,gain\right)\right)\times 32$$

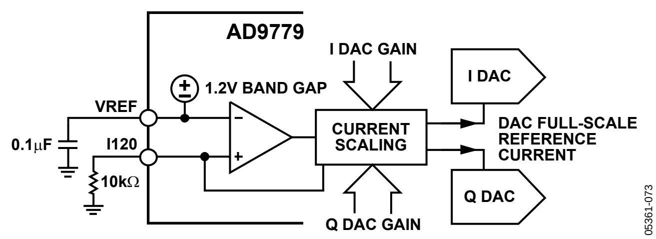


Figure 77. Reference Circuitry

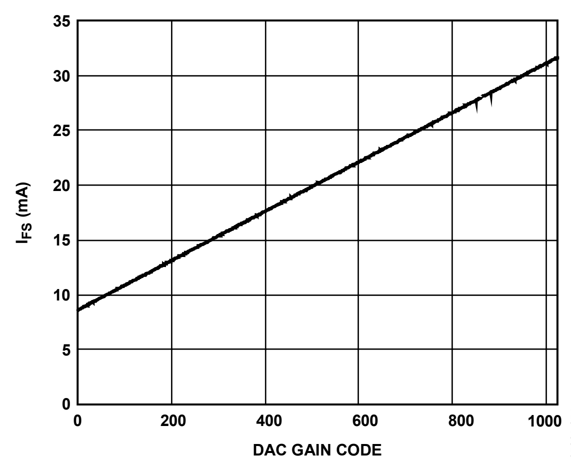


Figure 78. I_{FS} vs. DAC Gain Code

Application of Auxiliary DACs in Single Sideband Transmitter

Two auxiliary DACs are provided on the AD977x. The full-scale output current on these DACs is derived from the 1.2 V band gap reference and external resistor. The gain scale from the reference amplifier current $I_{REFERENCE}$ to the auxiliary DAC reference current is 16.67 with the auxiliary DAC gain set to full scale (10-bit values, SPI Register 0x0D and SPI Register 0x11), this gives a full-scale current of approximately 2 mA for auxiliary DAC1 and auxiliary DAC2. The auxiliary DAC outputs are not differential. Only one side of the auxiliary DAC (P or N) is active at one time. The inactive side goes into a high impedance state (>100 kΩ). In addition, the P or N outputs can act as current sources or sinks. The control of the P and N side for both auxiliary DACs is via Register 0x0E and Register 0x10, Bits<7:6>. When sourcing current, the output compliance voltage is 0 V to 1.6 V. When sinking current, the output compliance voltage is 0.8 V to 1.6 V.

The auxiliary DACs can be used for local oscillator (LO) cancellation when the DAC output is followed by a quadrature modulator. This LO feedthrough is caused by the input referred dc offset voltage of the quadrature modulator (and the DAC output offset voltage mismatch) and can degrade system performance. Typical DAC-to-quadrature modulator interfaces are shown in Figure 79 and Figure 80. Often, the input common-mode voltage for the modulator is much higher than the output compliance range of the DAC, so that ac coupling or a dc level shift is necessary. If the required common-mode input voltage on the quadrature modulator matches that of the DAC, then the dc blocking capacitors in Figure 79 can be removed. A low-pass or band-pass passive filter is recommended when spurious signals from the DAC (distortion and DAC images) at the quadrature modulator inputs can affect the system performance. Placing the filter at the location shown in Figure 79 and Figure 80 allows easy design of the filter, as the source and load impedances can easily be designed close to 50 Ω.

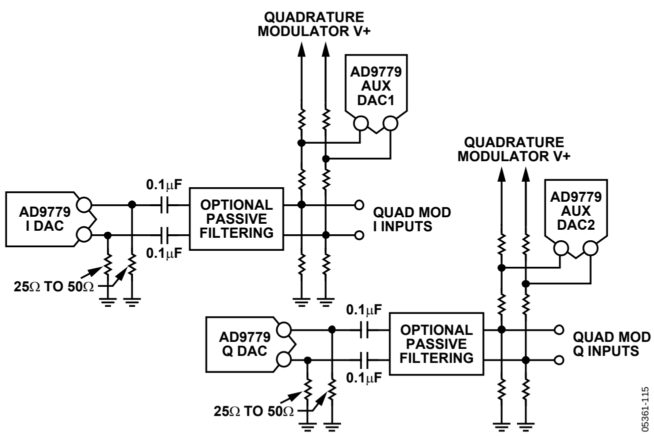


Figure 79. Typical Use of Auxiliary DACs AC Coupling to Quadrature Modulator

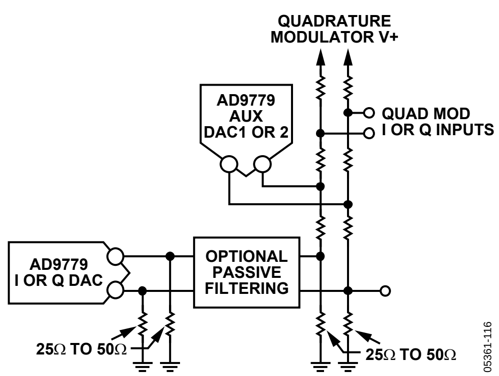


Figure 80. Typical Use of Auxiliary DACs DC Coupling to Quadrature Modulator with DC Shift

POWER DISSIPATION

Figure 81 to Figure 89 show the power dissipation of the 1.8 V and 3.3 V digital and clock supplies in single DAC and dual DAC modes. In addition to this, the power dissipation/current of the 3.3 V supply (mode and speed independent) in single DAC mode is 102 mW/31 mA. In dual DAC mode, this is 182 mW/55 mA. Furthermore, when the PLL is enabled, it adds 90 mW/50 mA to the 1.8 V clock supply regardless of the mode of the AD9779.

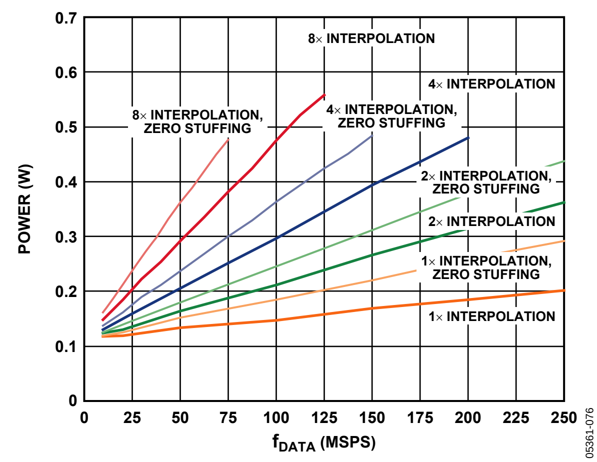


Figure 81. Total Power Dissipation, I Data Only, Real Mode

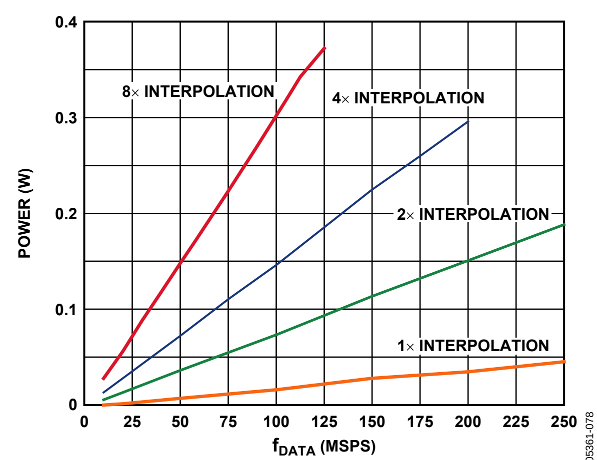


Figure 82. Power Dissipation, Digital 1.8 V Supply, I Data Only, Real Mode, Does Not Include Zero Stuffing

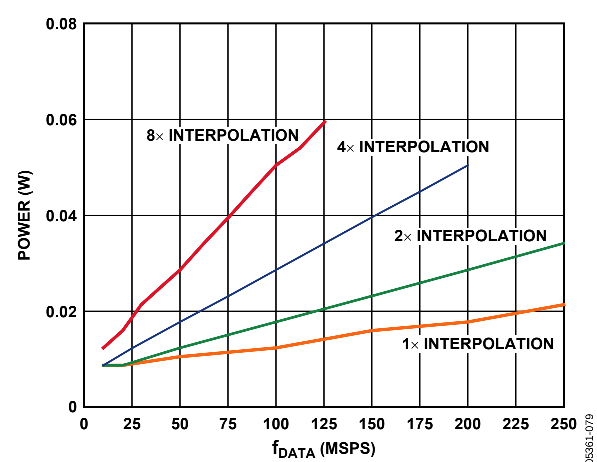


Figure 83. Power Dissipation, Clock 1.8 V Supply, I Data Only, Real Mode, Includes Modulation Modes, Does Not Include Zero Stuffing

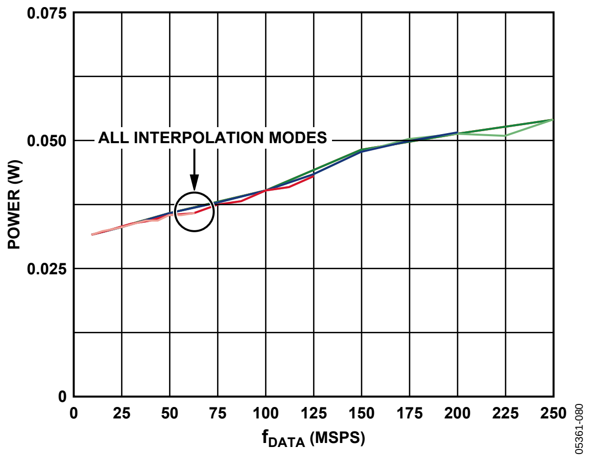


Figure 84. Digital 3.3 V Supply, I Data Only, Real Mode, Includes Modulation Modes and Zero Stuffing

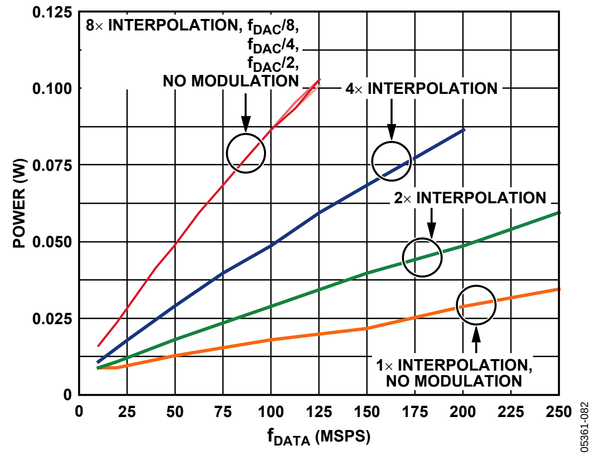


Figure 87. Power Dissipation, Clock 1.8 V Supply, I and Q Data, Dual DAC Mode, Does Not Include Zero Stuffing

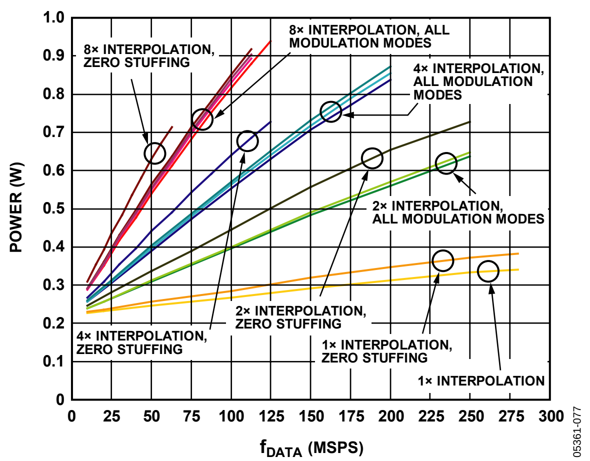


Figure 85. Total Power Dissipation, Dual DAC Mode

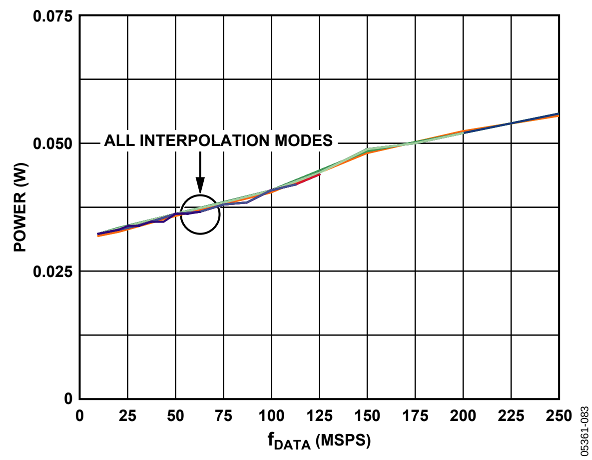


Figure 88. Digital 3.3 V Supply, I and Q Data, Dual DAC Mode

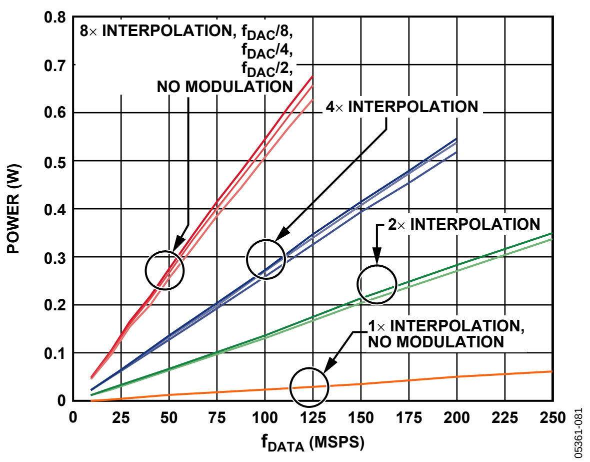


Figure 86. Power Dissipation, Digital 1.8 V Supply, I and Q Data, Dual DAC Mode, Does Not Include Zero Stuffing

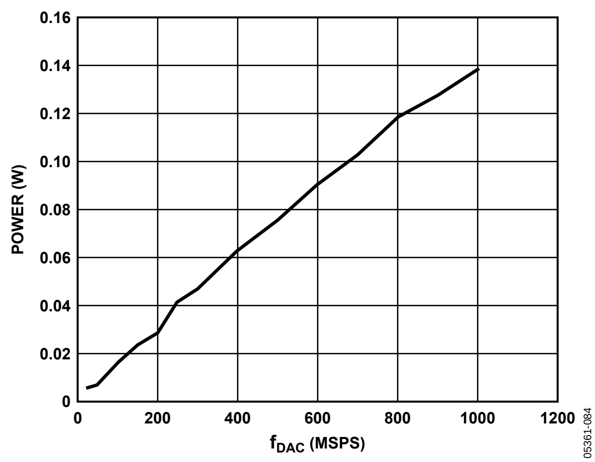


Figure 89. Power Dissipation of Inverse Sinc Filter

POWER-DOWN AND SLEEP MODES

The AD977x has a variety of power-down modes, so that the digital engine, main TxDACs, or auxiliary DACs can be powered down individually or together. Via the SPI port, the main TxDACs can be placed in sleep or power-down mode. In sleep mode, the TxDAC output is turned off, thus reducing power dissipation. The reference remains powered on, however, so that recovery from sleep mode is very fast. With the power-down mode bit set (Register 0x00, Bit 4), all analog and digital circuitry, including the reference, is powered down. The SPI port remains active in this mode. This mode offers more substantial power savings than sleep mode, but the turn-on time is much longer. The auxiliary DACs also have the capability to be programmed into sleep mode via the SPI port. The auto power-down enable bit (Register 0x00, Bit 3) controls the power-down function for the digital section of the devices. The auto power-down function works in conjunction with the TXENABLE pin (Pin 39) according to the following:

TXENABLE (Pin 39) =

- 0: autopower-down enable =
  - 0: flush data path with 0s
  - 1: flush data for multiple REFCLK cycles; then automatically place the digital engine in power-down state. DACs, reference, and SPI port are not affected.

or TXENABLE (Pin 39) =

- 1: normal operation

As shown in Figure 90, the power dissipation saved by using the power down mode is nearly proportional to the duty cycle of the signal at the TXENABLE pin.

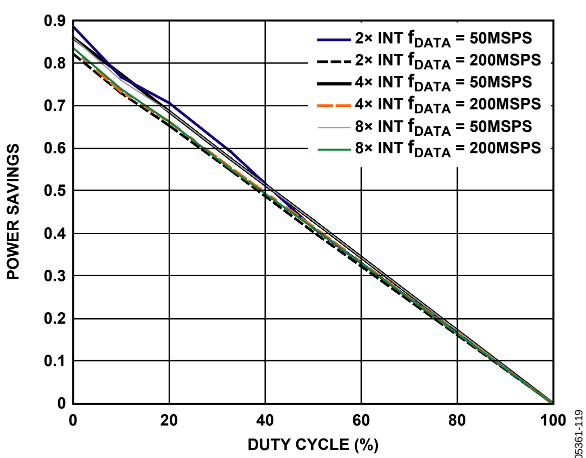


Figure 90. Power Savings Based on Duty Cycle of TxEnable

If the TxEnable invert bit (Register 0x02, Bit 1) is set, the function of this TXENABLE pin is inverted.

INTERLEAVED DATA MODE

The TxEnable bit is dual function. In dual port mode, it is simply used to power down the digital section of the devices. In interleaved mode, the IQ data stream is synchronized to TXENABLE. Therefore, to achieve IQ synchronization, TXENABLE should be held low until an I data word is present at the inputs to Data Port 1. If a DATACLK rising edge occurs while TXENABLE is at a high logic level, IQ data becomes synchronized to the DATACLK output. TXENABLE can remain high and the input IQ data remains synchronized. To be backwards-compatible with previous DACs from Analog Devices, Inc. such as the AD9777 and AD9786, the user can also toggle TXENABLE once during each data input cycle, thus continually updating the synchronization. If TXENABLE is brought low and held low for multiple REFCLK cycles, then the devices flush the data in the interpolation filters, and shut down the digital engine after the filters are flushed. The amount of REFCLK cycles it takes to go into this power-down mode is then a function of the length of the equivalent 2×, 4×, or 8× interpolation filter. The timing of TXENABLE, I/Q select, filter flush, and digital power-down are shown in Figure 91.

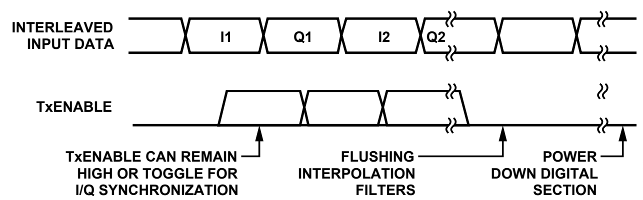


Figure 91. TXENABLE Function

The TXENABLE function can be inverted by changing the status of Register 0x02, Bit 1. The other bit that controls IQ ordering is the Q-first bit (Register 0x02, Bit 0). With the Q-first bit reset to the default of 0, the IQ pairing that is latched is the I1Q1, I2Q2, and so on. With IQ first set to 1, the first I data is discarded and the pairing is I2Q1, I3Q2, and so on. Note that with IQ-first set, the I data is still routed to the internal I channel, the Q data is routed to the internal Q channel, and only the pairing changes.

TIMING INFORMATION

Figure 92 to Figure 95 show some of the various timing possibilities when the PLL is enabled. The combination of the settings of N2 and N3 from Figure 74 means that the reference clock frequency can be a multiple of the actual input data rate. Figure 92 to Figure 95 show, respectively, what the timing looks like when N2/N3 = 1 and 2.

In interleaved mode, set-up and hold times of DATACLK out to data in are the same as those shown in Figure 92 to Figure 95. It is recommended that any toggling of TXENABLE occur concurrently with the digital data input updating. In this way, timing margins between DATACLK, TXENABLE, and digital input data are optimized.

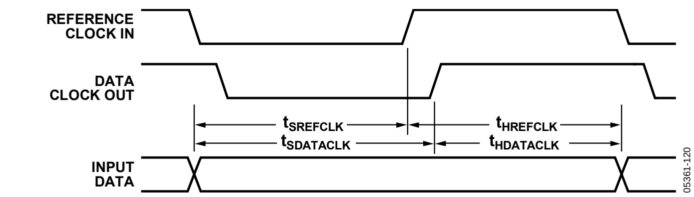


Figure 92. Timing Specifications, PLL Enabled or Disabled, Interpolation = 1×

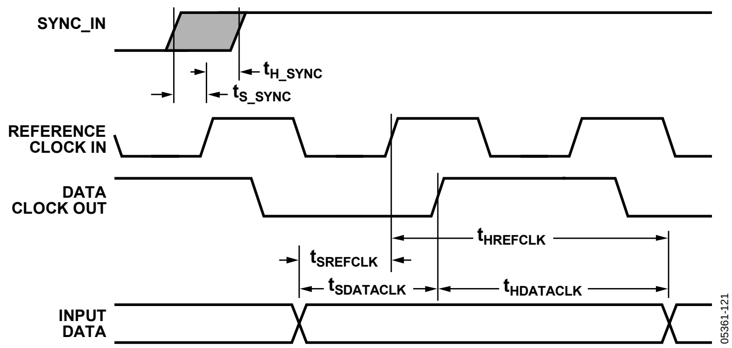


Figure 93. Timing Specifications, PLL Enabled or Disabled, Interpolation = 2×

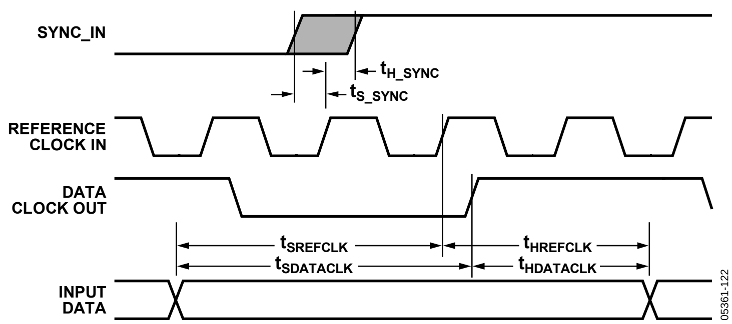


Figure 94. Timing Specifications, PLL Enabled or Disabled, Interpolation = 4×

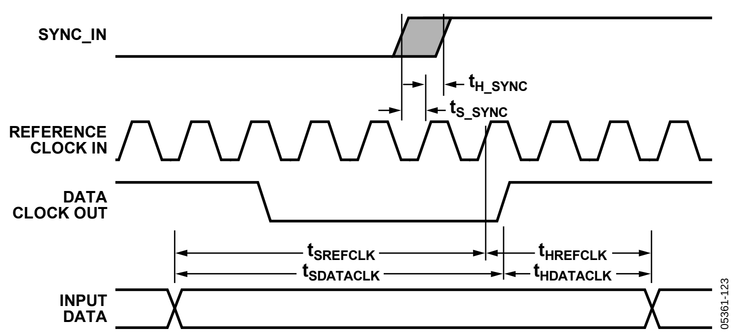


Figure 95. Timing Specifications, PLL Enabled or Disabled, Interpolation = 8×

Specifications are given in Table 19 for the drift of input data set up and hold time vs. temperature, as well as the data keep out window (KOW). Note that although these specifications do drift, the length of the keep out window, where input data is invalid, changes very little over temperature.

Table 19. AD9779 Timing Specifications vs. Temperature

Timing Parameter	Temperature	Min t_S (ns)	Min t_H (ns)	Max KOW (ns)
REFCLK to DATA	−40°C	−0.8	+2.2	+1.3
	+25°C	−1.1	+2.5	+1.4
	+85°C	−1.3	+2.9	+1.5
DATACLK to DATA	−40°C	+1.8	−0.4	+1.3
	+25°C	+2.1	−0.7	+1.4
	+85°C	+2.5	−0.9	+1.5
SYNC_I to REFCLK	−40°C to +85°C	−0.2	+1.0	+0.8

SYNCHRONIZATION OF INPUT DATA TO DATACLK OUTPUT (PIN 37)

Synchronizing the input data bus to the DATACLK out signal is achieved by meeting the timing relationships between DATACLK and DATA timing specified in Table 19. If the user is synchronizing the input data to the DATACLK out, the sync input (SYNC_I) signal does not need to be applied and can be ignored (connect to GND).

SYNCHRONIZATION OF INPUT DATA TO THE REFCLK INPUT (PIN 5 AND PIN 6) WITH PLL ENABLED OR DISABLED

Synchronizing the input data bus to the REFCLK input requires the use of the SYNC_I input pins (Pin 13 and Pin 14). If the SYNC_I input is not used, there is a phase ambiguity between the DATACLK out and the REFCLK in. This ambiguity matches the interpolation rate in which the AD9779, for example, is currently operating. Because input data is latched on the rising edge of DATACLK, it is impossible for the user to determine onto which one of the multiple internal DACCLK edges (as an example, one of four edges in 4× interpolation) the input data actually latches. For the user to specifically determine the exact edge of REFCLK on which the data is being latched, a rising edge must be periodically applied to SYNC_I. The frequency of the SYNC_I signal must be equal to $f_{DAC}/2^N$, N being an integer, and must be no greater than DATACLK for proper synchronization. There is no limit on how slow the SYNC_I signal can be driven. As long as the set up and hold timing relationship between SYNC_I and REFCLK given in Table 19 is met, the input data is latched on the immediate next rising edge of REFCLK. Note that a rising edge of DATACLK out occurs concurrently with the next REFCLK rising edge, after a short propagation delay. Although this propagation delay is not specified, input data setup and hold timing information is given with respect to REFCLK in and DATACLK out in Figure 92 to Figure 95. Also, note that in 1× interpolation, because there is no phase ambiguity, there is no need to use the SYNC_I signal.

Valid Timing Window

In addition to the timing requirements of SYNC_I with respect to REFCLK, it is important to understand that the valid timing window for SYNC_I is limited by the internal DAC sample rate. This is shown in Figure 96. When the t_S and t_H requirements are met, the valid timing window for SYNC_I extends only as far as one period of the internal DAC sample rate (minus t_S and t_H). Failure to meet this timing specification can potentially result in erroneous data being latched into the AD9779 digital inputs.

As an example, if the AD9779 input data rate is 122.88 MSPS and the REFCLK is the same, with the AD9779 in 4× interpolation, the DAC sample rate is 1/491.52 MHz or about 2 ns. With a t_S of −0.2 ns and t_H of 1.0 ns, this gives a valid timing window for SYNC_I of

$$2 \text{ ns} - 0.8 \text{ ns} = 1.2 \text{ ns}$$

The timing window of the digital input data to REFCLK can be moved in increments of one internal REFCLK cycle by using the REFCLK OFFSET register (Register 0x7, Bits<4:0>).

Because SYNC_I can be run at the same frequency as REFCLK when the PLL is enabled, best practice suggests that in this condition, REFCLK and SYNC_I originate from the same source. This limits the variation in time between these two signals and makes the overall timing budget easier to achieve. A slight delay may be necessary on the REFCLK path in this configuration to add more timing margin between REFCLK and SYNC_I (see Table 19 for timing relationship).

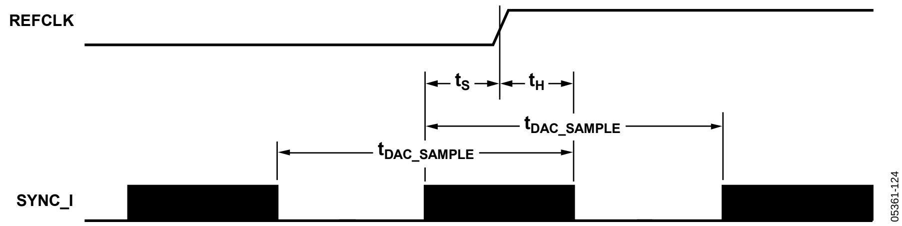


Figure 96. Valid Timing Relationship for SYNC_I to REFCLK

Using Data Delay to Meet Timing Requirements

To meet strict timing requirements at input data rates of up to 250 MSPS, the AD977x has a fine timing feature. Fine timing adjustments are made by programming values into the data clock delay register (Register 0x04, Bits<7:4>). This register can be used to add delay between the REFCLK in and the DATACLK out. Figure 97 shows the default delay present when DATACLK delay is disabled. The disable function bit is found in Register 0x02, Bit 4. Figure 98 shows the delay present when DATACLK delay is enabled and set to 0000. Figure 99 indicates the delay when DATACLK delay is enabled and set to 1111. Note that the setup and hold times specified for data to DATACLK are defined for DATACLK delay disabled.

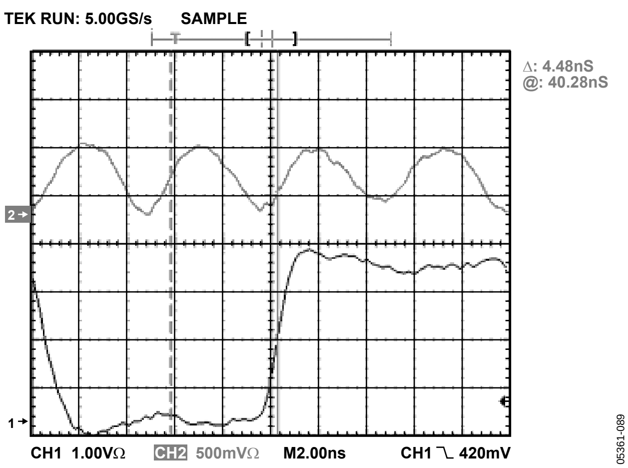


Figure 97. Delay from REFCLK to DATACLK with DATACLK Delay Disabled

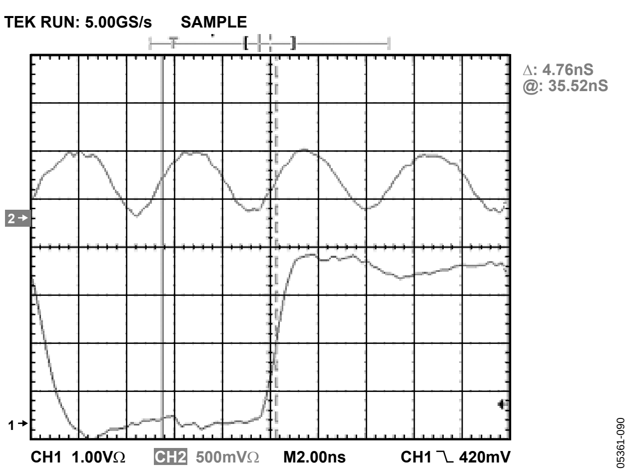


Figure 98. Delay from REFCLK to DATACLK Out with DATACLK Delay = 0000

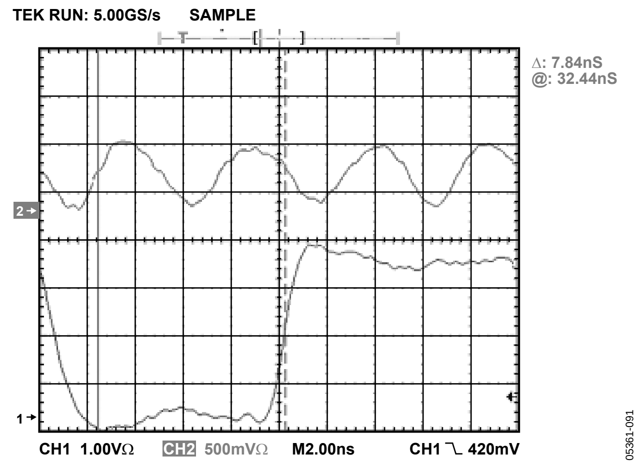


Figure 99. Delay from REFCLK to DATACLK Out with DATACLK Delay = 1111

The difference between the minimum delay shown in Figure 98 and the maximum delay shown in Figure 99 is the range programmable using the DATACLK delay register. The delay (in absolute time) when programming DATACLK delay between 0000 and 1111 is a linear extrapolation between these two figures. The typical delays per increment over temperature are shown in Table 20.

Table 20. Data Delay Line Typical Delays Over Temperature

Delays	−40°C	+25°C	+85°C	Unit
Delay Between Disabled and Enabled	370	416	432	ps
Average Delay per Increment	171	183	197	ps

The frequency of DATACLK out depends on several programmable settings: interpolation, zero stuffing, and interleaved/dual port mode, all of which have an effect on the REFCLK frequency. The divisor function between REFCLK and DATACLK is equal to the values shown in Table 21.

Table 21. REFCLK to DATACLK Divisor Ratio

Interpolation	Zero Stuffing	Input Mode	Divisor
1	Disabled	Dual port	1
2	Disabled	Dual port	2
4	Disabled	Dual port	4
8	Disabled	Dual port	8
1	Disabled	Interleaved	Invalid
2	Disabled	Interleaved	1
4	Disabled	Interleaved	2
8	Disabled	Interleaved	4
1	Enabled	Dual port	2
2	Enabled	Dual port	4
4	Enabled	Dual port	8
8	Enabled	Dual port	16
1	Enabled	Interleaved	1
2	Enabled	Interleaved	2
4	Enabled	Interleaved	4
8	Enabled	Interleaved	8

In addition to this divisor function, DATACLK can be divided by up to an additional factor of 4, according to the state of the DATACLK divide register (Register 0x03, Bits<5:4>). For more details, see Table 22).

Table 22. Extra DATACLK Divisor Ratio

Register 0x03, Bits<5:4>	Divider Ratio
00	1
01	2
10	4
11	1

The maximum divisor resulting from the combination of the values in Table 21, and the DATACLK divide register is 32.

Manual Input Timing Correction

Correction of input timing can be achieved manually. The correction function is controlled by Register 0x03, Bits<7:6>. The function is programmed as shown in Table 23.

Table 23. Input Timing Correction Mode

Register 0x03, Bits<7:6>	Function
00	Error check disabled
01	Reserved
10	Reserved
11	Reserved

Necessary corrections can be made by adjusting DATACLK delay and the DATACLK invert bit (Register 2, Bit 2). DATACLK delay can then be swept to find the range over which the timing is valid. The final value for data delay should be the value that corresponds to the middle of the valid timing range. If a valid timing range is not found during this sweep, the user should invert the DATACLK invert bit and repeat the process.

Multiple DAC Synchronization

The AD9779 has programmable features that allow the CMOS digital data bus inputs and internal filters on multiple devices to be synchronized. This means that the DATACLK output signal on one AD9779 can be used to register the output data for a data bus delivering data to multiple AD9779s. The details of this operation are given in the Analog Devices *Application Note AN-822*.

EVALUATION BOARD OPERATION

The AD977x evaluation board is designed to optimize the DAC performance and the speed of the digital interface, yet remains user friendly. To operate the board, the user needs a power source, a clock source, and a digital data source. The user also needs a spectrum analyzer or an oscilloscope to look at the DAC output. The diagram in Figure 100 illustrates the test setup. A sine or square wave clock works well as a clock source. The dc offset on the clock is not a problem, since the clock is ac-coupled on the evaluation board before the REFCLK inputs. All necessary connections to the evaluation board are shown in more detail in Figure 101.

The evaluation board comes with software that allows the user to program the SPI port. Via the SPI port, the devices can be programmed into any of its various operating modes. When first operating the evaluation board, it is useful to start with a simple configuration, that is, a configuration in which the SPI port settings are as close as possible to the default settings. The default software window is shown in Figure 102. The arrows indicate which settings need to be changed for an easy first time evaluation. Note that this implies that the PLL is not being used and that the clock being used is at the speed of the DAC output sample rate. For a more detailed description of how to use the PLL, see the PLL Loop Filter Bandwidth section.

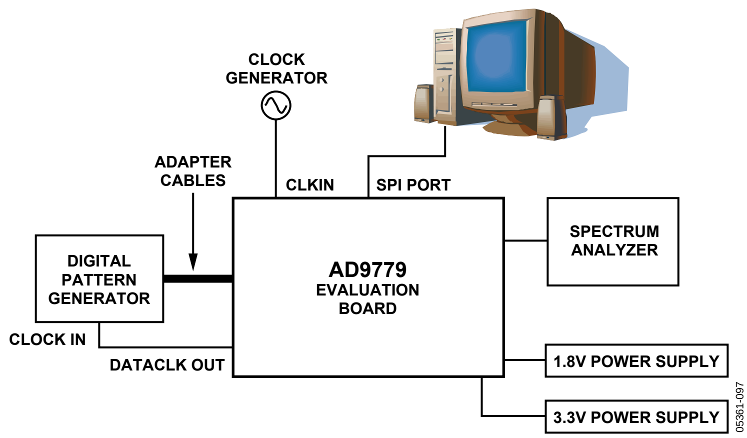


Figure 100. Typical Test Setup

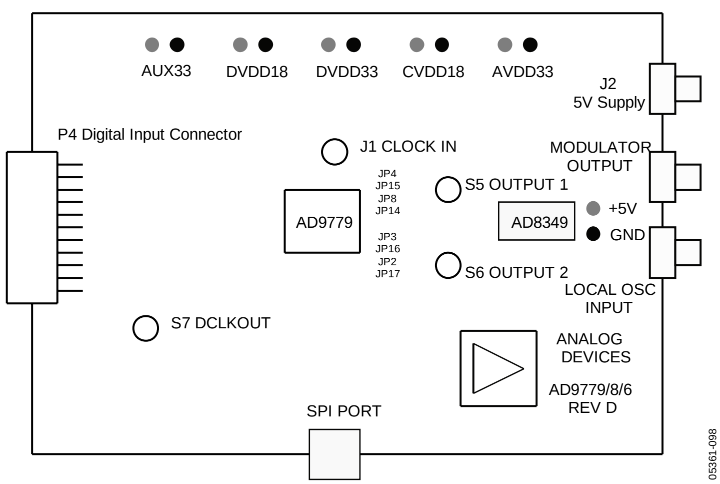


Figure 101. AD977x Evaluation Board Showing All Connections

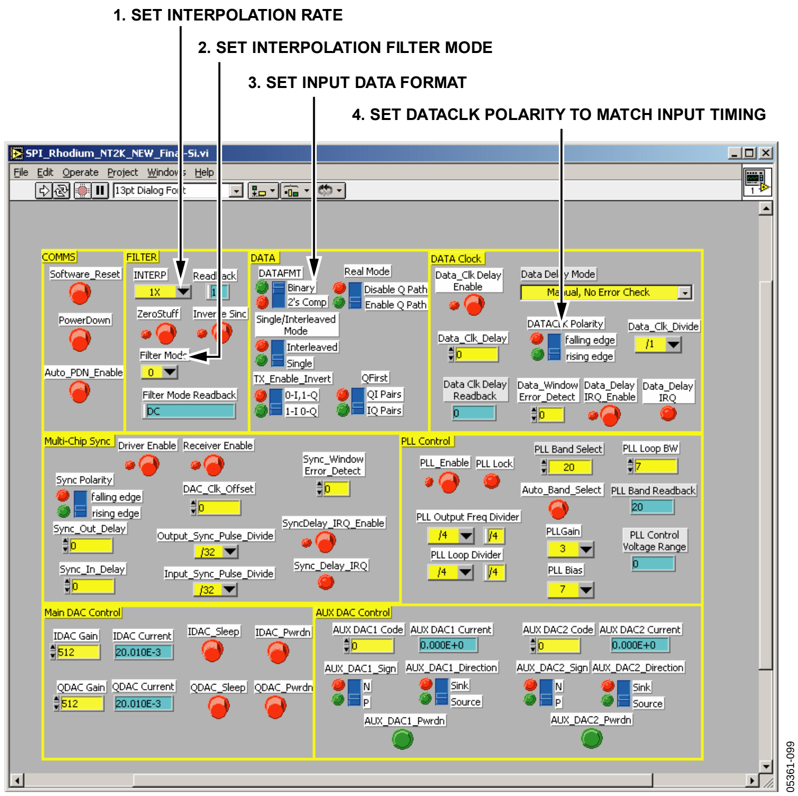


Figure 102. SPI Port Software Window

The default settings for the evaluation board allow the user to view the differential outputs through a transformer that converts the DAC output signal to a single-ended signal. On the evaluation board, these transformers are designated T1A, T2A, T3A, and T4A. There are also four common-mode transformers on the board that are designated T1B, T2B, T3B, and T4B. The recommended operating setup places the transformer and common-mode transformer in series. A pair of transformers and common-mode transformers are installed on each DAC output, so that the pairs can be set up in either order. As an example, for the frequency range of dc to 30 MHz, it is recommended that the transformer be placed right after the DAC. Above DAC output frequencies of 30 MHz, it is recommended that the common-mode transformer is placed right after the DAC outputs, followed by the transformer.

MODIFYING THE EVALUATION BOARD TO USE THE AD8349 ON-BOARD QUADRATURE MODULATOR

The evaluation board contains an Analog Devices AD8349 quadrature modulator. The AD977x and AD8349 provide an easy-to-interface DAC/modulator combination that can be easily evaluated on the evaluation board. To route the DAC output signal to the quadrature modulator, the following jumper settings must be made:

Unsoldered: JP14, JP15, JP16, JP17
Soldered: JP2, JP3, JP4, JP8

The DAC output area of the evaluation board is shown in Figure 103. The jumpers that need to be changed to use the AD8349 are circled. Also circled are the 5 V and GND connections for the AD8349.

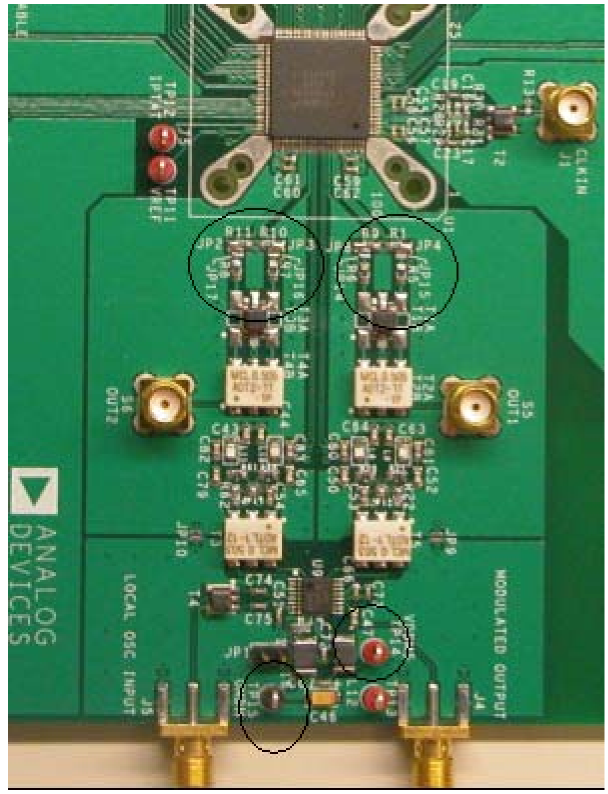

05361-100

Figure 103. Photo of Evaluation Board, DAC Output Area

EVALUATION BOARD SCHEMATICS

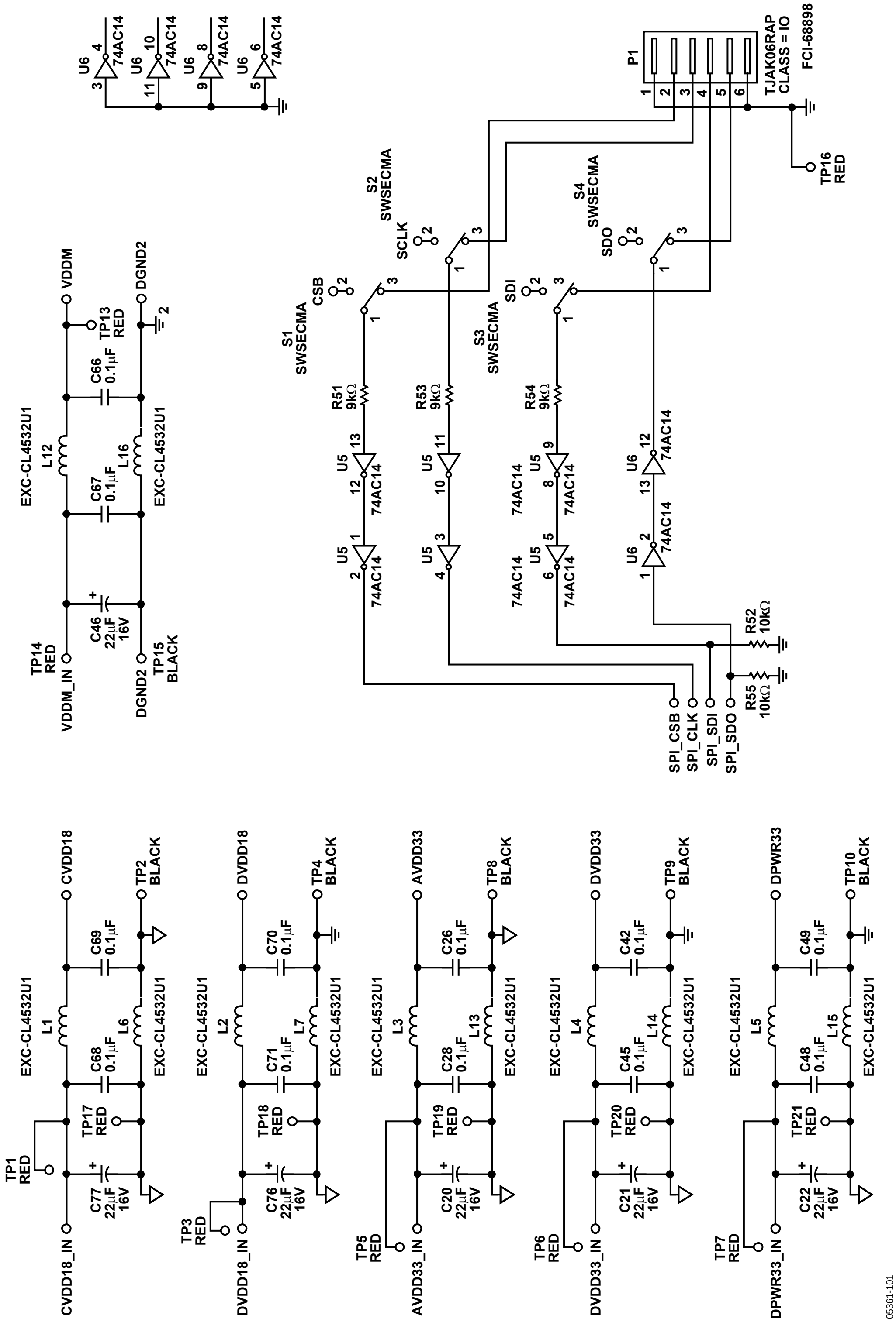


Figure 104. Evaluation Board, Rev. D, Power Supply Decoupling and SPI Interface

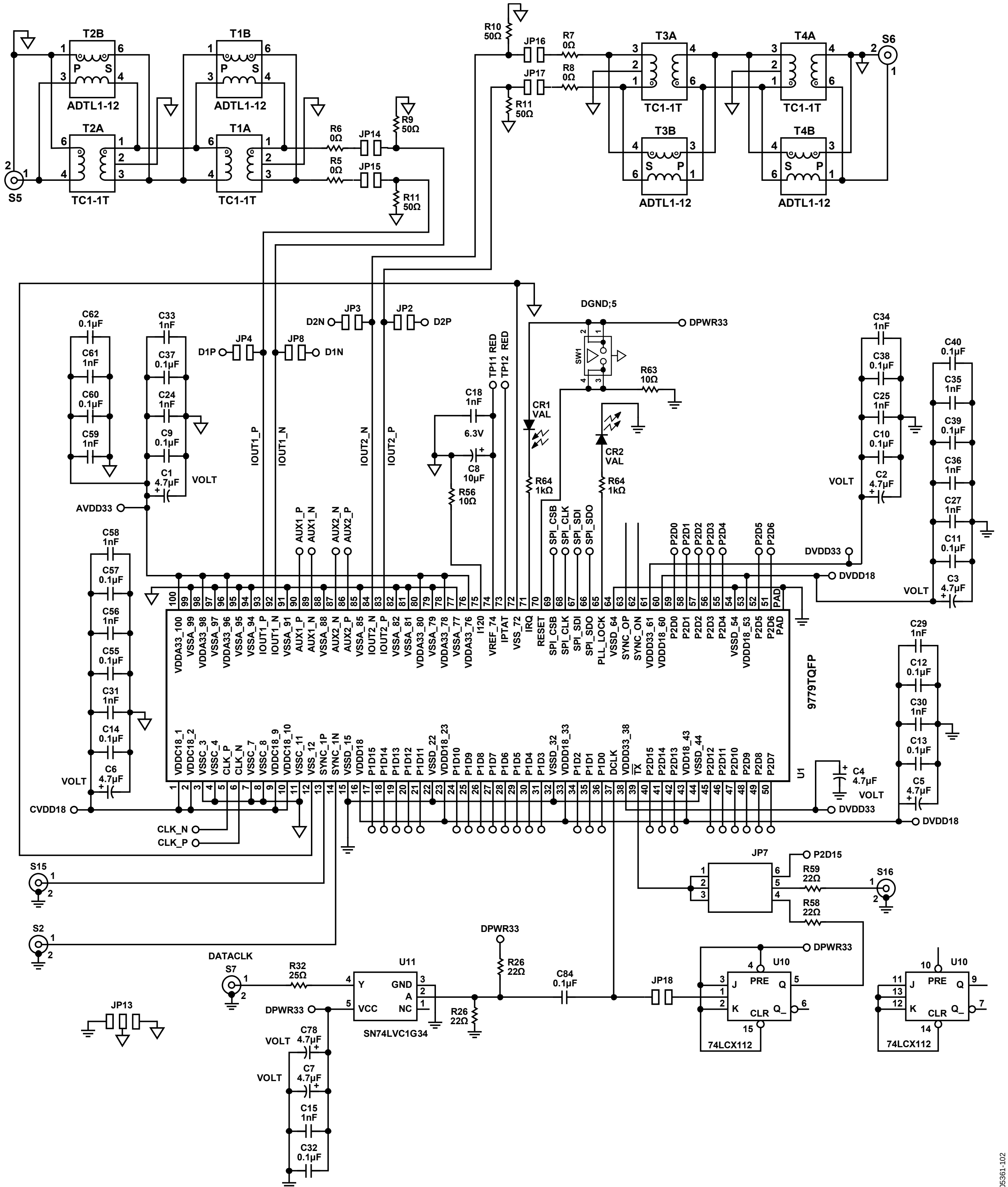


Figure 105. Evaluation Board, Rev. D, Circuitry Local to Devices

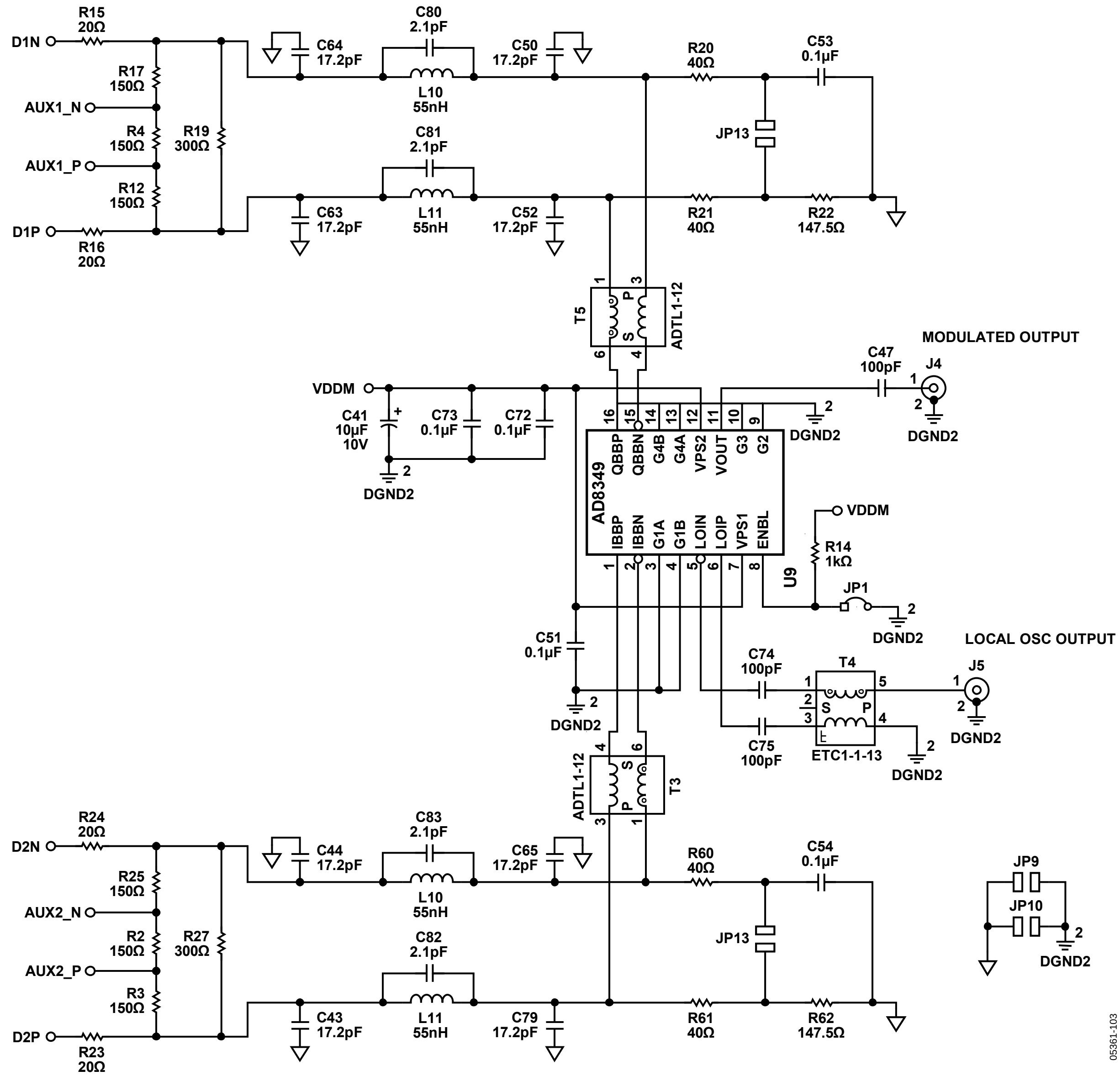


Figure 106. Evaluation Board, Rev. D, AD8349 Quadrature Modulator

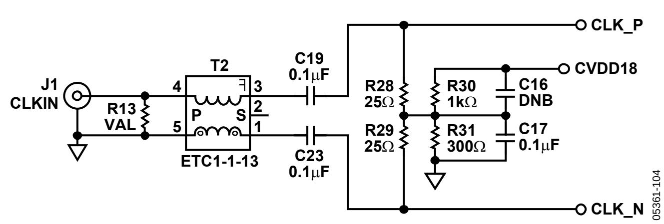


Figure 107. Evaluation Board, Rev. D, DAC Clock Interface

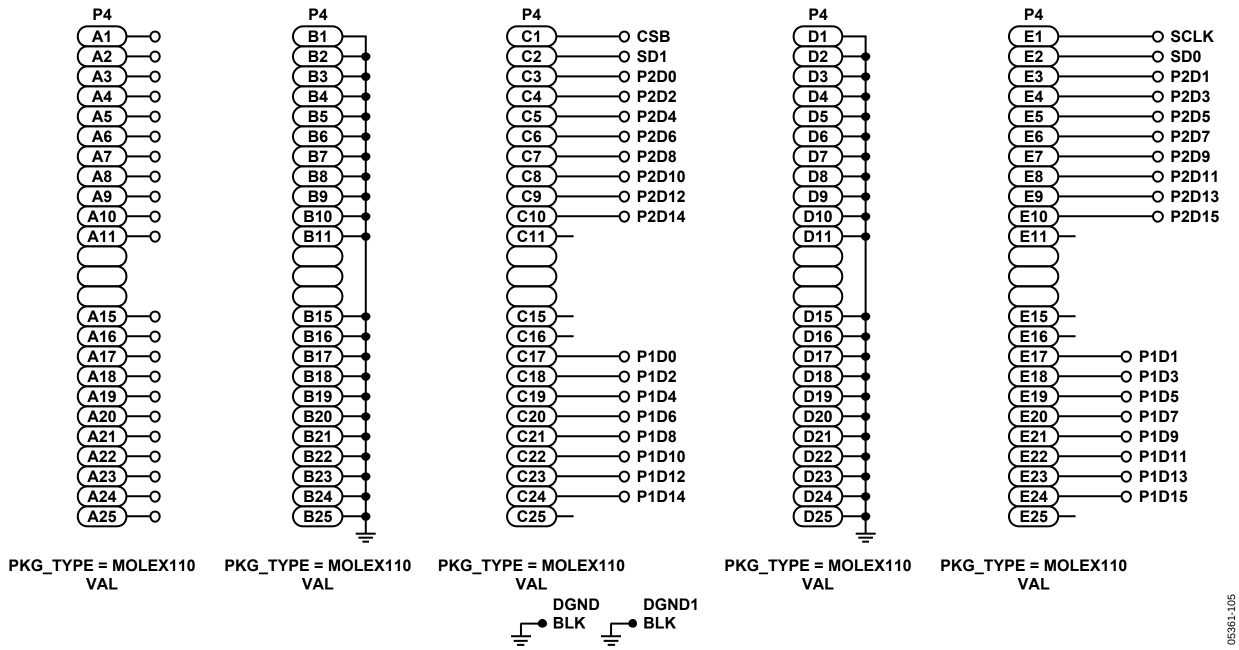


Figure 108. Evaluation Board, Rev. D, Digital Input Buffers

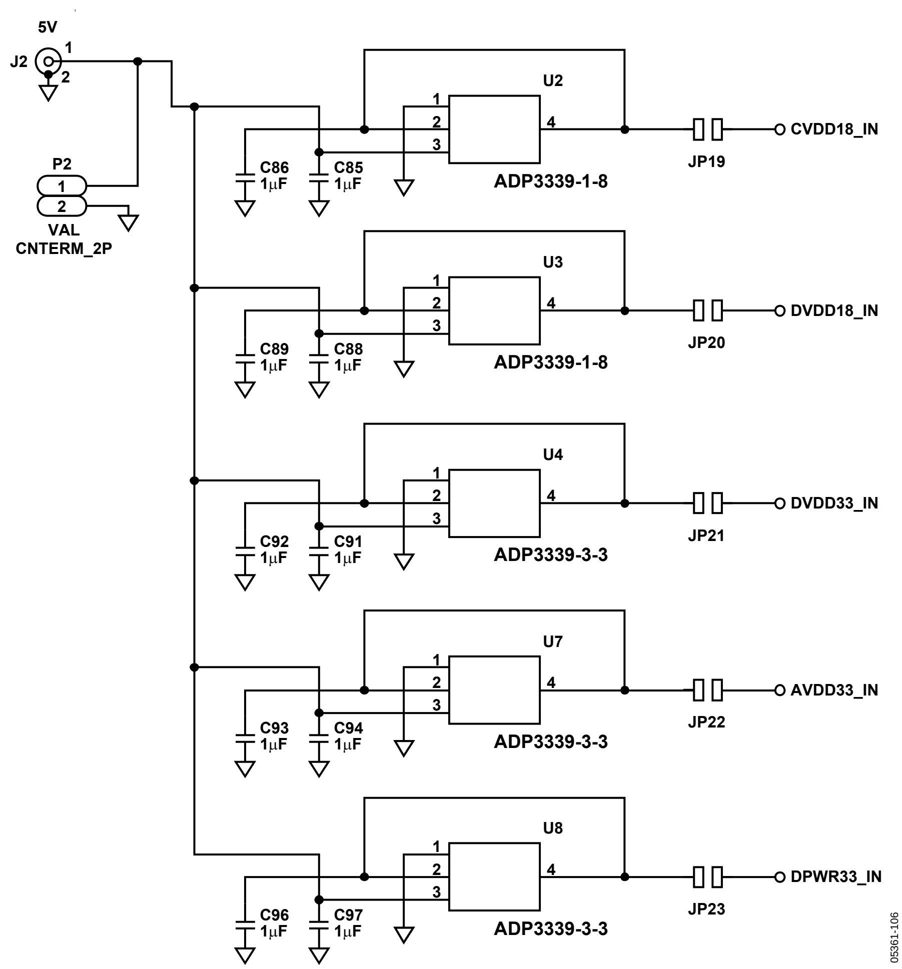


Figure 109. Evaluation Board, On-Board Voltage Regulators

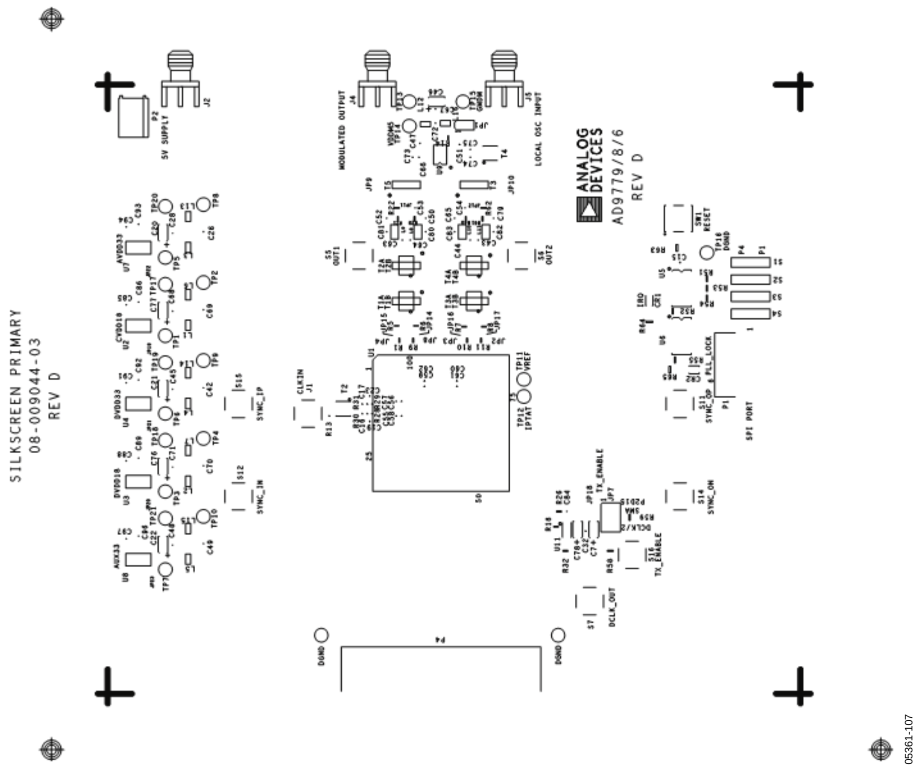


Figure 110. Evaluation Board, Rev. D, Top Silk Screen

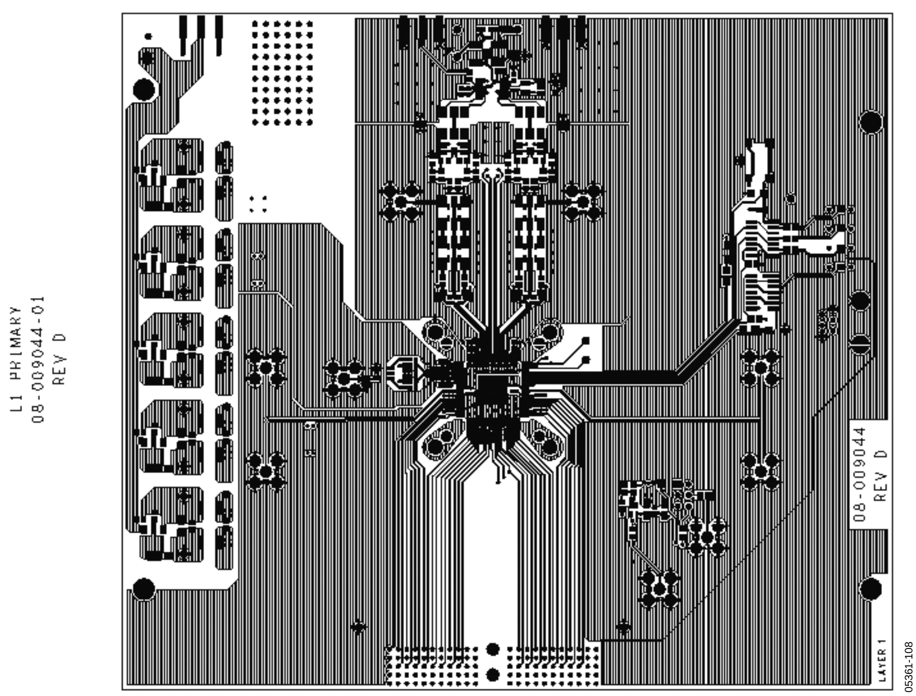


Figure 111. Evaluation Board, Rev. D, Top Layer

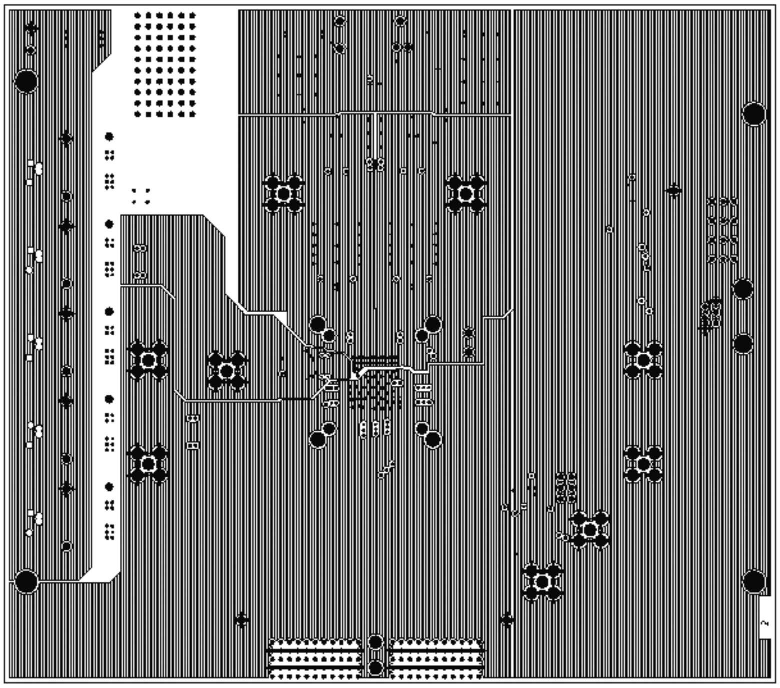


Figure 112. Evaluation Board, Rev. D, Layer 2

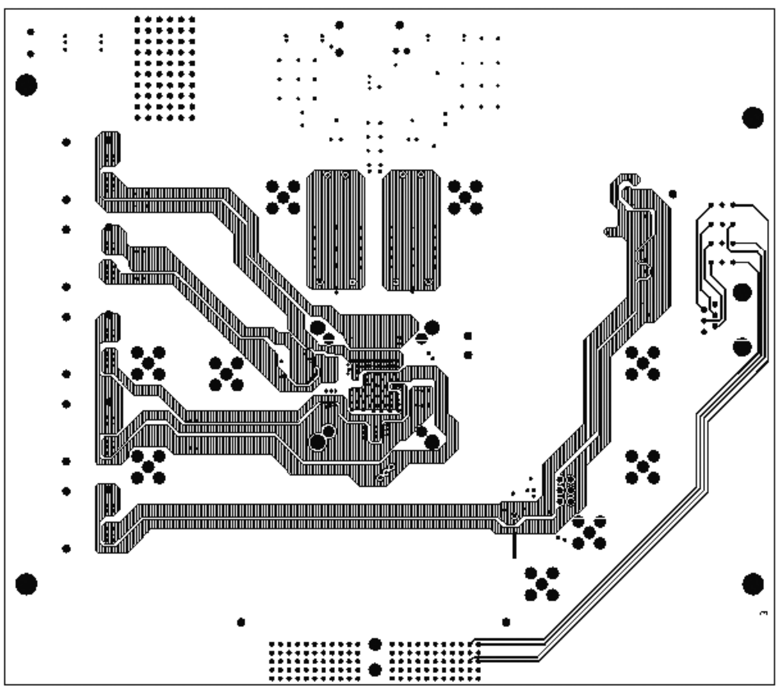


Figure 113. Evaluation Board, Rev. D, Layer 3

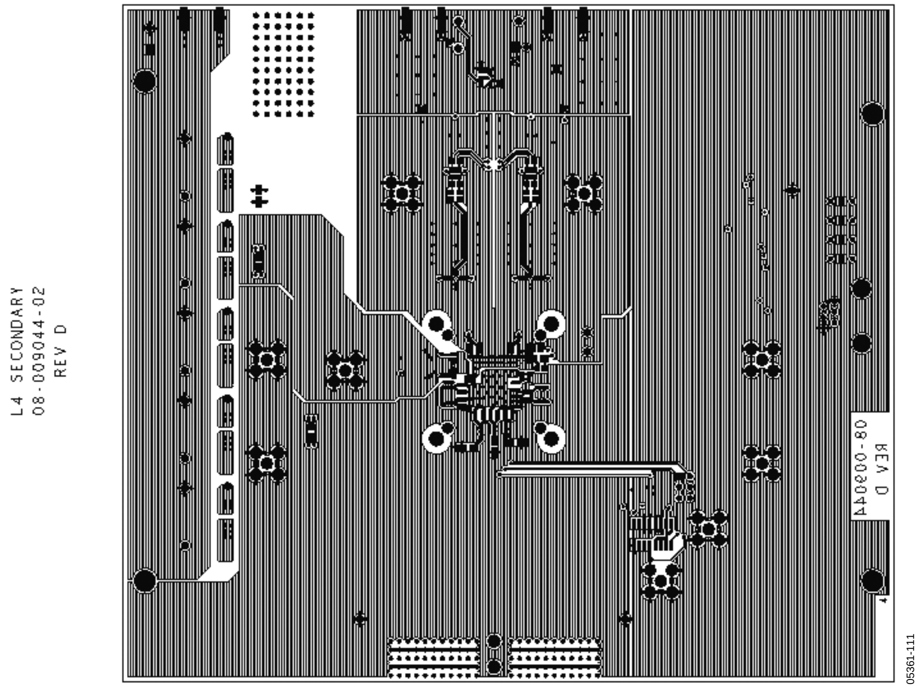


Figure 114. Evaluation Board, Rev. D, Bottom Layer

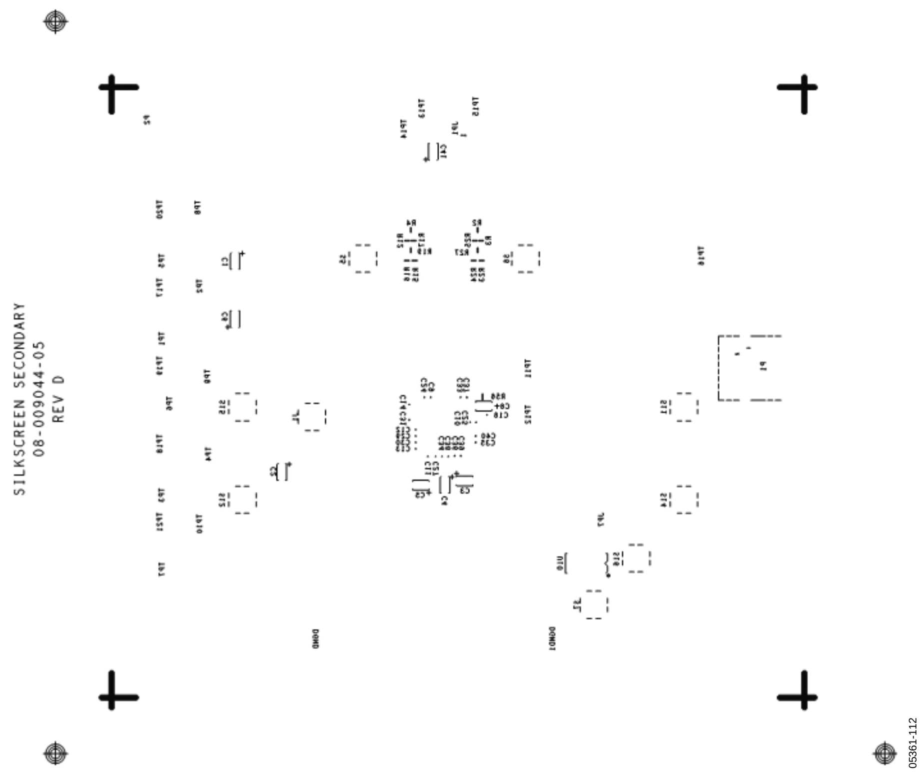
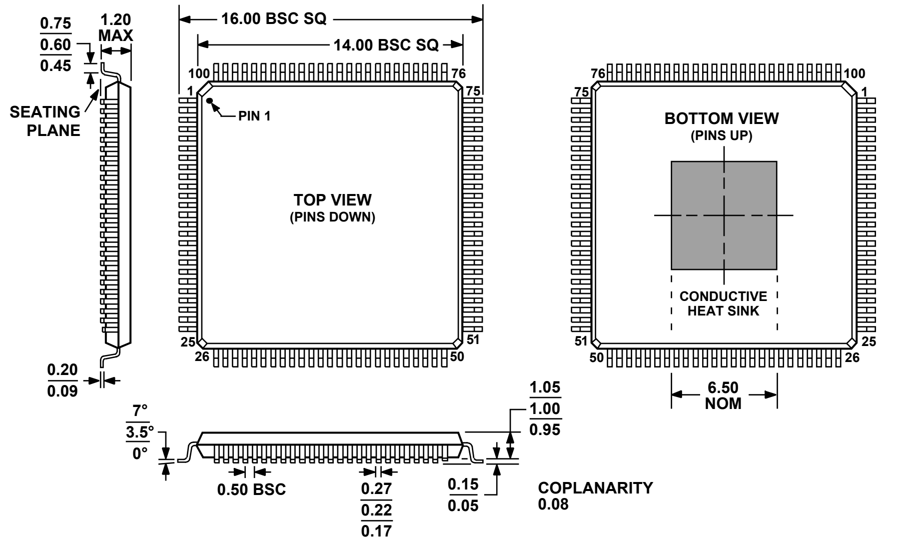


Figure 115. Evaluation Board, Rev. D, Bottom Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

NOTES
1. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
2. THE PACKAGE HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO CHIP GROUND. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A GROUND PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

Figure 116. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-1)
Dimensions shown in millimeters

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Model	Temperature Range	Package Description	Package Option
AD9776BSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9776BSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9778BSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9778BSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9779BSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9779BSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-1
AD9776-EB		Evaluation Board	
AD9778-EB		Evaluation Board	
AD9779-EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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