ANALOG DEVICES

Quad 8-Bit Multiplying CMOS D/A Converter with Memory

DAC8408

FEATURES

- Four DACs in a 28 Pin, 0.6 Inch Wide DIP or 28-Pin JEDEC Plastic Chip Carrier
- ±1/4 LSB Endpoint Linearity
- Guaranteed Monotonic
- DACs Matched to Within 1%
- Microprocessor Compatible
- Read/Write Capability (with Memory)
- TTL/CMOS Compatible
- Four-Quadrant Multiplication
- Single-Supply Operation (+5 V)
- Low Power Consumption
- Latch-Up Resistant
- Available In Die Form

APPLICATIONS

- Voltage Set Points in Automatic Test Equipment
- Systems Requiring Data Access for Self-Diagnostics
- Industrial Automation
- Multichannel Microprocessor-Controlled Systems
- Digitally Controlled Op Amp Offset Adjustment
- Process Control
- Digital Attenuators

GENERAL DESCRIPTION

The DAC8408 is a monolithic quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its own reference input, feedback resistor, and onboard data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ determine which DAC will accept data. Data loading is similar to that of a RAMs write cycle. Data can be read back onto the same data bus with control line R/$\overline{W}$. The DAC8408 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. The DAC8408 operates on a single +5 volt supply and dissipates less than 20 mW. The DAC8408 is manufactured using PMI's highly stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

ORDERING INFORMATION[1]

Model	INL	DNL	Temperature Range	Package Description
DAC8408GP	±1/4 LSB	±1/2 LSB	0°C to +70°C	28-Pin Plastic DIP
DAC8408ET	±1/4 LSB	±1/2 LSB	–40°C to +85°C	28-Pin Cerdip
DAC8408AT[2]	±1/4 LSB	±1/2 LSB	–55°C to +125°C	28-Pin Cerdip
DAC8408FT	±1/2 LSB	±1 LSB	–40°C to +85°C	28-Pin Cerdip
DAC8408BT[2]	±1/2 LSB	±1 LSB	–55°C to +125°C	28-Pin Cerdip
DAC8408FPC[3]	±1/2 LSB	±1 LSB	–40°C to +85°C	28-Contact PLCC
DAC8408FS	±1/2 LSB	±1 LSB	–40°C to +85°C	28-Pin SOL
DAC8408FP	±1/2 LSB	±1 LSB	–40°C to +85°C	28-Pin Plastic DIP

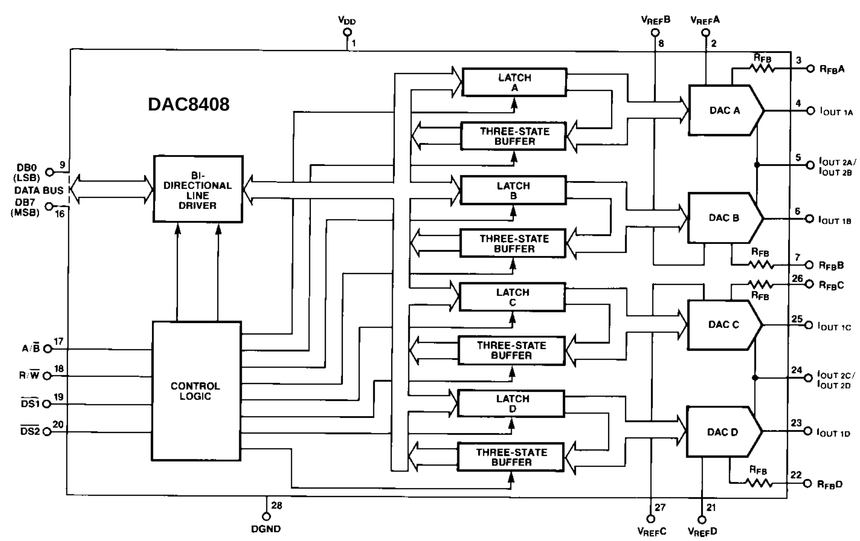
NOTES

[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages. For outline information see Package Information section.

[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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Tel: 617/329-4700 Fax: 617/326-8703

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5 V; V_{REF} = ±10 V; V_{OUT}A, B, C, D = 0 V; T_A = –55°C to +125°C apply for DAC8408AT/BT, T_A = –40°C to +85°C apply for DAC8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D.)

Parameter	Symbol	Conditions	DAC8408 Min	Typ	Max	Units
STATIC ACCURACY						
Resolution	N		8			Bits
Nonlinearity[1, 2]	INL	DAC8408A/E/G			±1/4	LSB
		DAC8408B/F/H			±1/2	LSB
Differential Nonlinearity	DNL	DAC8408A/E/G			±1/2	LSB
		DAC8408B/F/H			±1	LSB
Gain Error	G_{FSE}	(Using Internal R_{FB})			±1	LSB
Gain Tempco[3, 6]	TC_{GFS}			±2	±40	ppm/°C
Power Supply Rejection (ΔV_{DD} = ±10%)	PSR				0.001	%FSR/%
$I_{OUT\ 1A,\ B,\ C,\ D}$ Leakage Current[13]	I_{LKG}	T_A =+25°C			±30	nA
		T_A = Full Temperature Range			±100	nA
REFERENCE INPUT						
Input Voltage Range					±20	V
Input Resistance Match[4]		$R_{A,\ B,\ C,\ D}$			±1	%
Input Resistance	R_{IN}		6	10	14	kΩ
DIGITAL INPUTS						
Digital Input Low	V_{IL}				0.8	V
Digital Input High	V_{IH}		2.4			V
Input Current[5]		T_A = +25°C		±0.01	±1.0	µA
	I_{IN}	T_A = Full Temperature Range			±10.0	µA
Input Capacitance[6]	C_{IN}				8	pF
DATA BUS OUTPUTS						
Digital Output Low	V_{OL}	16 mA Sink			0.4	V
Digital Output High	V_{OH}	400 µA Source	4			V
Output Leakage Current	I_{LKG}	T_A = +25°C		±0.005	±1.0	µA
		T_A = Full Temperature Range		±0.075	±10.0	µA
DAC OUTPUTS[6]						
Propagation Delay[7]	t_{PD}			150	180	ns
Settling Time[11,12]	t_S			190	250	ns
Output Capacitance	C_{OUT}	DAC Latches All "0s"			30	pF
		DAC Latches All "1s"			50	pF
AC Feedthrough	FT	(20 V_{p-p} @ F = 100 kHz)	54			dB
SWITCHING CHARACTERISTICS[6, 10]						
Write to Data Strobe Time	t_{DS1} or	T_A = +25°C	90			ns
	t_{DS2}	T_A = Full Temperature Range	145			ns
Data Valid to Strobe Set-Up Time	t_{DSU}	T_A = +25°C	150			ns
		T_A = Full Temperature Range	175			ns
Data Valid to Strobe Hold Time	t_{DH}		10			ns
DAC Select to Strobe Set-Up Time	t_{AS}		0			ns
DAC Select to Strobe Hold Time	t_{AH}		0			ns
Write Select to Strobe Set-Up Time	t_{WSU}		0			ns
Write Select to Strobe Hold Time	t_{WH}		0			ns
Read to Data Strobe Width	t_{RDS}	T_A = +25°C	220			ns
		T_A = Full Temperature Range	350			ns
Data Strobe to Output Valid Time	t_{CO}	T_A = +25°C	320			ns
		T_A = Full Temperature Range	430			ns
Output Data to Deselect Time	t_{OTD}	T_A = +25°C	200			ns
		T_A = Full Temperature Range	270			ns
Read Select to Strobe Set-Up Time	t_{RSU}		0			ns
Read Select to Strobe Hold Time	t_{RH}		0			ns

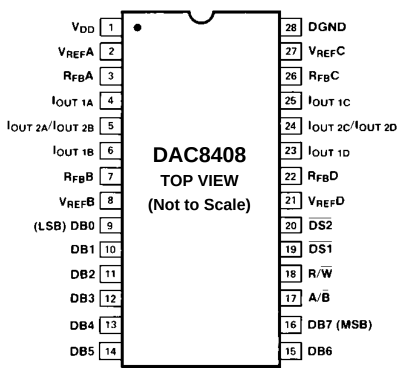
Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS @ V_{DD} = +5 V; V_{REF} = ±10 V; V_{OUT}A, B, C, D = 0 V; T_A = –55°C to +125°C apply for DAC8408AT/BT, T_A = –40°C to +85°C apply for DAC8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D. *Continued*

Parameter	Symbol	Conditions	DAC8408 Min	DAC8408 Typ	DAC8408 Max	Units
POWER SUPPLY						
Voltage Range	V_{DD}		4.5		5.5	V
Supply Current[8]	I_{DD}				50	µA
Supply Current[9]	I_{DD}	T_A = +25°C			1.0	mA
		T_A = Full Temperature Range			1.5	mA

NOTES
[1]This is an end-point linearity specification.
[2]Guaranteed to be monotonic over the full operating temperature range.
[3]ppm/°C of FSR (FSR = Full Scale Range = V_{REF}-1 LSB.)
[4]Input Resistance Temperature Coefficient = +300ppm/°C.
[5]Logic Inputs are MOS gates. Typical input current at +25°C Is less than 10 nA.
[6]Guaranteed by design.
[7]From Digital Input to 90% of final analog output current.
[8]All Digital Inputs "0" or V_{DD}.
[9]All Digital Inputs V_{IH} or V_{IL}.
[10]See Timing Diagram.
[11]Digital Inputs = 0 V to V_{DD} or V_{DD} to 0 V.
[12]Extrapolated: t_S (1/2 LSB) = t_{PD} + 6.2τ where τ = the measured first time constant of the final RC decay.
[13]All Digital Inputs = 0 V; V_{REF} = +10 V.
Specifications subject to change without notice.

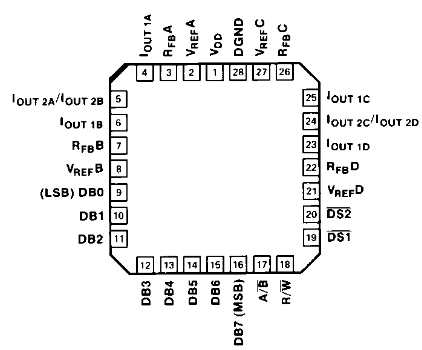
PIN CONNECTIONS



28-PIN HERMETIC DIP (T-Suffix)

28-PIN EPOXY DIP (P-Suffix)

28-PIN SOL (S-Suffix)



28-PIN PLASTIC LEADED CHIP CARRIER (PC-Suffix)

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

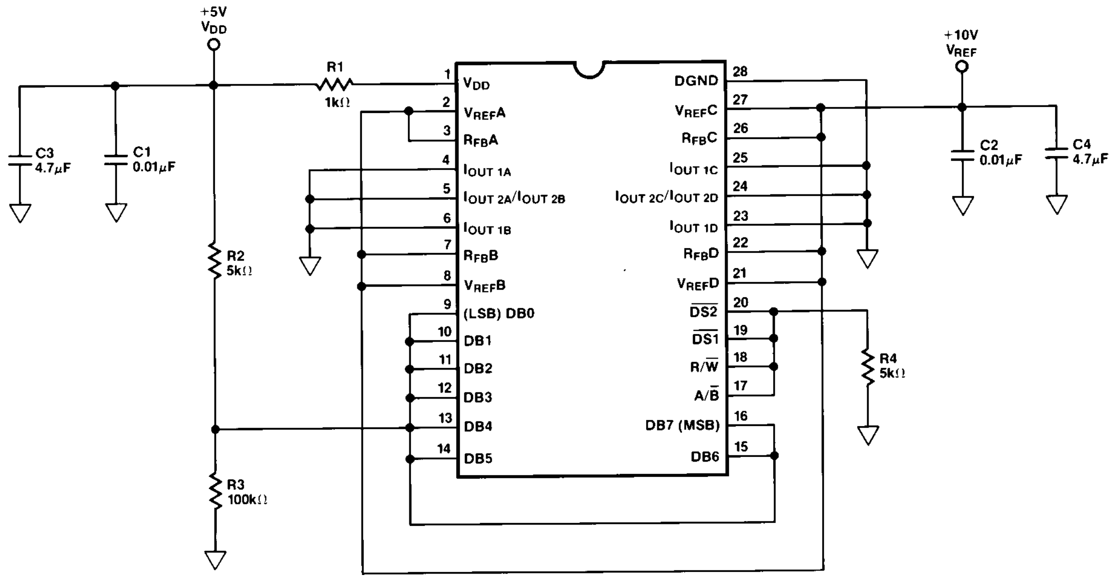
V_{DD} to $I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ . . . . 0 V, +7 V
V_{DD} to DGND . . . . 0 V, +7 V
$I_{OUT\ 1A}$, $I_{OUT\ 1B}$,
$I_{OUT\ 1C}$, $I_{OUT\ 1D}$ to DGND . . . . –0.3 V to V_{DD} +0.3 V
R_{FB}A, R_{FB}B, R_{FB}C, R_{FB}D to I_{OUT} . . . . ±25 V
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$,
$I_{OUT\ 2C}$, $I_{OUT\ 2D}$ to DGND . . . . –0.3 V to V_{DD} + 0.3 V
DB0 through DB7 to DGND . . . . –0.3 V to V_{DD} + 0.3 V
Control Logic
Input Voltage to DGND . . . . –0.3 V + V_{DD} + 0.3 V
V_{REF}A, V_{REF}B, V_{REF}C, V_{REF}D to
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ . . . . ±25 V
Operating Temperature Range
Commercial Grade (GP) . . . . 0°C to +70°C
Industrial Grade (ET, FT, FP, FPC, FS) . . –40°C to +85°C
Military Grade (AT, BT) . . . . –55°C to +125°C
Junction Temperature . . . . +150°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C

Package Type	θ_{JA}*	θ_{JC}	Units
28-Pin Hermetic DIP (T)	55	10	°C/W
28-Pin Plastic DIP (P)	53	27	°C/W
28-Pin SOL (S)	68	23	°C/W
28-Contact PLCC (PC)	66	29	°C/W

*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION

1. Do not apply voltages higher than V_{DD} +0.3 V or less than –0.3 V potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high energy electrostatic fields. Keep in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

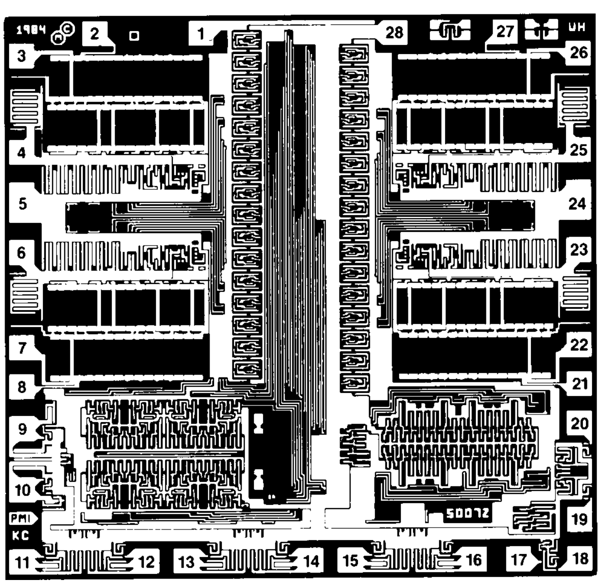


Burn-in Circuit

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the DAC8408 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DICE CHARACTERISTICS



DIE SIZE 0.130 × 0.124 inch, 16,120 sq. mils
(3.30 × 3.15 mm, 10.4 sq. mm)

1. V_{DD}
2. $V_{REF}A$
3. $R_{FB}A$
4. $I_{OUT\ 1A}$
5. $I_{OUT\ 2A}/I_{OUT\ 2B}$
6. $I_{OUT\ 1B}$
7. $R_{FB}B$
8. $V_{REF}B$
9. DB0 (LSB)
10. DB1
11. DB2
12. DB3
13. DB4
14. DB5
15. DB6
16. DB7 (MSB)
17. $A/\overline{B}$
18. $\overline{R/W}$
19. $\overline{DS1}$
20. $\overline{DS2}$
21. $V_{REF}D$
22. $R_{FB}D$
23. $I_{OUT\ 1D}$
24. $I_{OUT\ 2C}/I_{OUT\ 2D}$
25. $I_{OUT\ 1C}$
26. $R_{FB}C$
27. $V_{REF}C$
28. DGND

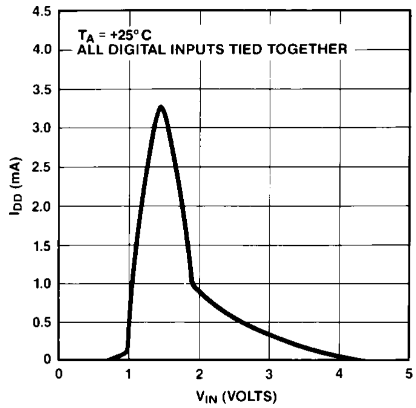
WAFER TEST LIMITS at V_{DD} = +5 V; V_{REF} = ±10 V; V_{OUT}A, B, C, D = 0 V; T_A = +25°C, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

Parameter	Symbol	Conditions	DAC8408G Limits	Units
STATIC ACCURACY				
Resolution	N		8	Bits min
Nonlinearity[1]	INL		±1/2	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Gain Error	G_{FSE}	Using Internal R_{FB}	±1	LSB max
Power Supply Rejection (ΔV_{DD} = ±10%)[2]	PSR	Using Internal R_{FB}	0.001	%FSR/% max
$I_{OUT\ 1A,\ B,\ C,\ D}$ Leakage Current	I_{LKG} V_{REF} = +10 V	All Digital Inputs = 0 V	±30	nA max
REFERENCE INPUT				
Reference Input Resistance[3]	R_{IN}		6/14	kΩ min/max
Input Resistance Match	R_{IN}		±1	% max
DIGITAL INPUTS				
Digital Input Low	V_{IL}		0.8	V max
Digital Input High	V_{IH}		2.4	V min
Input Current[4]	I_{IN}		±1.0	µA max
DATA BUS OUTPUTS				
Digital Output Low	V_{OL}	1.6 mA Sink	0.4	V max
Digital Output High	V_{OH}	400 µA Source	4	V min
Output Leakage Current	I_{LKG}		±1.0	µA max
POWER SUPPLY				
Supply Current[5]	I_{DD}		50	µA max
Supply Current[6]	I_{DD}		1.0	mA max

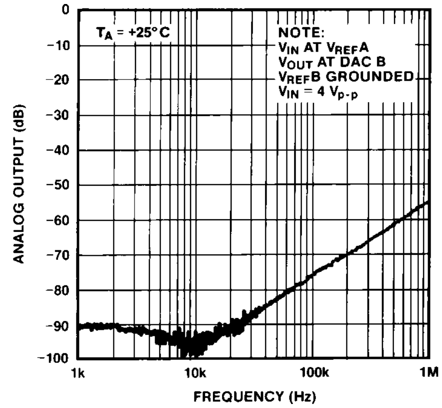
NOTES
[1]This is an endpoint linearity specification.
[2]FSR is Full Scale Range = V_{REF} –1 LSB.
[3]Input Resistance Temperature Coefficient approximately equals +300 ppm/°C.
[4]Logic inputs are MOS gates.Typical input current at +25°C is less than 10 nA.
[5]All Digital Inputs are either “0” or V_{DD}.
[6]All Digital Inputs are either V_{IH} or V_{IL}.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

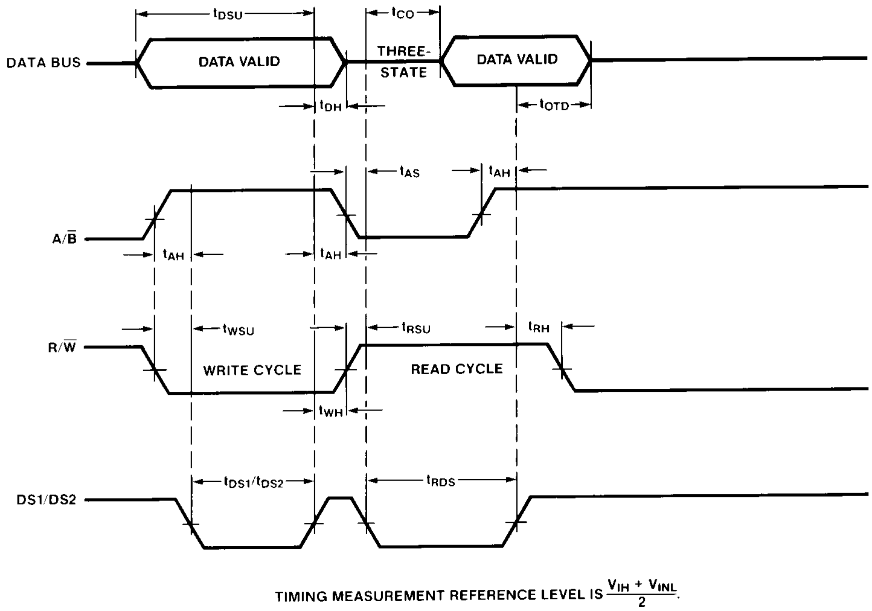
TYPICAL PERFORMANCE CHARACTERISTICS



Supply Current vs. Logic Level



Analog Crosstalk vs. Frequency



Timing Diagram

PARAMETER DEFINITIONS

RESOLUTION

Resolution is the number of states (2^n) that the full-scale range (FSR) of a DAC is divided (or resolved) into.

NONLINEARITY

Nonlinearity (Relative Accuracy) is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in LSB, %, or ppm of full-scale range.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1 LSB step size. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain Error (full-scale error) is a measure of the output error between the ideal and actual DAC output. The ideal full-scale output is V_{REF} –1 LSB.

OUTPUT CAPACITANCE

Output Capacitance is that capacitance between $I_{OUT\ 1A}$, $I_{OUT\ 1B}$, $I_{OUT\ 1C}$, or $I_{OUT\ 1D}$ and AGND.

AC FEEDTHROUGH ERROR

This is the error caused by capacitance coupling from V_{REF} to the DAC output with all switches off.

SETTLING TIME

Settling Time is the time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input signal.

PROPAGATION DELAY

This is a measure of the internal delays of the DAC. It is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

CHANNEL-TO-CHANNEL ISOLATION

This is the portion of input signal that appears at the output of a DAC from another DAC's reference input. It is expressed as a ratio in dB.

DIGITAL CROSSTALK

Digital Crosstalk is the glitch energy transferred to the output of one DAC due to a change in digital input code from other DACs. It is specified in nVs.

CIRCUIT INFORMATION

The DAC8408 combines four identical 8-bit CMOS DACs onto a single monolithic chip. Each DAC has its own reference input, feedback resistor, and on-board data latches. It also features a read/write function that serves as an accessible memory location for digital-input data words. The DAC's three-state readback drivers place the data word back onto the data bus.

D/A CONVERTER SECTION

Each DAC contains a highly stable, silicon-chromium, thin-film, R-2R resistor ladder network and eight pairs of current steering switches. These switches are in series with each ladder resistor and are single-pole, double-throw NMOS transistors; the gates of these transistors are controlled by CMOS inverters. Figure 1 shows a simplified circuit of the R-2R resistor ladder section, and Figure 2 shows an approximate equivalent switch circuit. The current through each resistor leg is switched between $I_{OUT\ 1}$ and $I_{OUT\ 2}$. This maintains a constant current in each leg, regardless of the digital input logic states.

Each transistor switch has a finite "ON" resistance that can introduce errors to the DAC's specified performance. These resistances must be accounted for by making the voltage drop across each transistor equal to each other. This is done by binarily-scaling the transistor's "ON" resistance from the most significant bit (MSB) to the least significant bit (LSB). With 10 volts applied at the reference input, the current through the MSB switch is 0.5 mA, the next bit is 0.25 mA, etc.; this maintains a constant 10 mV drop across each switch and the converter's accuracy is maintained. It also results in a constant resistance appearing at the DAC's reference input terminal; this allows the DAC to be driven by a voltage or current source, ac or dc of positive or negative polarity.

Shown in Figure 3 is an equivalent output circuit for DAC A. The circuit is shown with all digital inputs high. The leakage current source is the combination of surface and junction leakages to the substrate. The 1/256 current source represents the constant 1-bit current drain through the ladder terminating resistor. The situation is reversed with all digital inputs low, as shown in Figure 4. The output capacitance is code dependent, and therefore, is modulated between the low and high values.

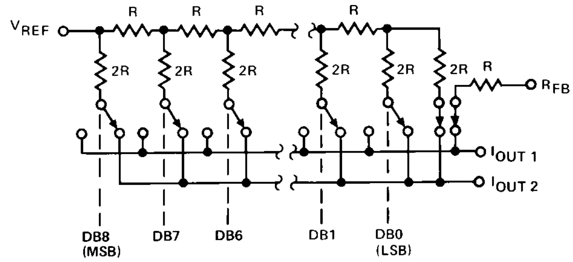


Figure 1. Simplified D/A Circuit of DAC8408

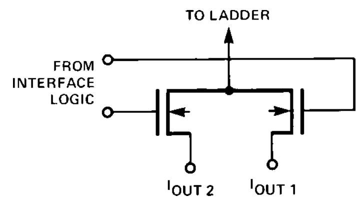


Figure 2. N-Channel Current Steering Switch

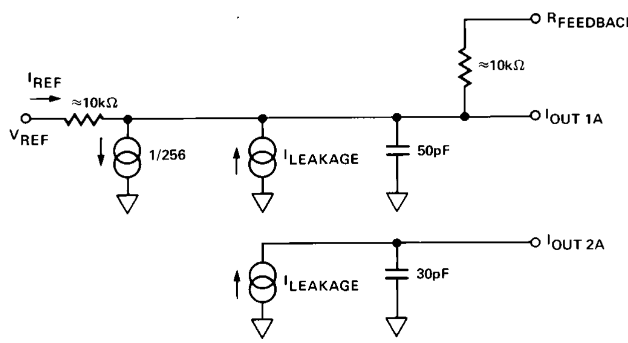


Figure 3. Equivalent DAC Circuit (All Digital Inputs HIGH)

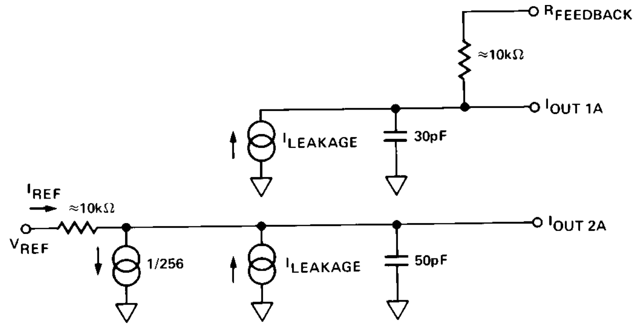


Figure 4. Equivalent DAC Circuit (All Digital Inputs LOW)

DIGITAL SECTION

Figure 5 shows the digital input/output structure for one bit. The digital WR, $\overline{WR}$, and $\overline{RD}$ controls shown in the figure are internally generated from the external A/$\overline{B}$, R/$\overline{W}$, $\overline{DS1}$, and $\overline{DS2}$ signals. The combination of these signals decide which DAC is selected. The digital inputs are CMOS inverters, designed such that TTL input levels (2.4 V and 0.8 V) are converted into CMOS logic levels. When the digital input is in the region of 1.2 V to 1.8 V, the input stages operate in their linear region and draw current from the +5 V supply (see Typical Supply Current vs. Logic Level curve on page 6). It is recommended that the digital input voltages be as close to V_{DD} and DGND as is practical in order to minimize supply currents. This allows maximum savings in power dissipation inherent with CMOS devices. The three-state readback digital output drivers (in the active mode) provide TTL-compatible digital outputs with a fan-out of one TTL load. The three state digital readback leakage-current is typically 5 nA.

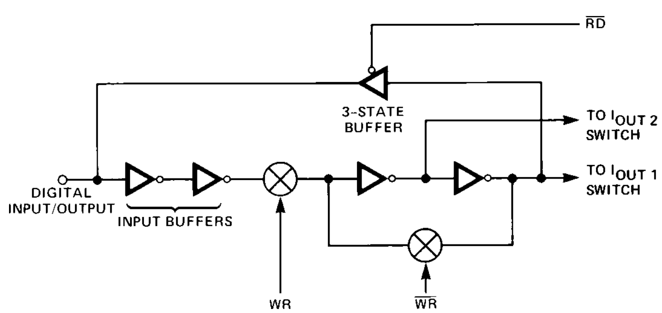


Figure 5. Digital Input/Output Structure

INTERFACE LOGIC SECTION

DAC Operating Modes

- All DACs in HOLD MODE.
- DAC A, B, C, or D individually selected (WRITE MODE).
- DAC A, B, C, or D individually selected (READ MODE).
- DACs A and C simultaneously selected (WRITE MODE).
- DACs B and D simultaneously selected (WRITE MODE).

DAC Selection: Control inputs, $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ select which DAC can accept data from the input port (see Mode Selection Table).

Mode Selection: Control inputs $\overline{DS}$ and R/$\overline{W}$ control the operating mode of the selected DAC.

Write Mode: When the control inputs $\overline{DS}$ and R/$\overline{W}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent, and its analog output responds to activity on the data inputs DB0–DB7.

Hold Mode: The selected DAC latch retains the data that was present on the bus line just prior to $\overline{DS}$ or R/$\overline{W}$ going to a high state. All analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When $\overline{DS}$ is low and R/$\overline{W}$ is high, the selected DAC is in the read mode, and the data held in the appropriate latch is put back onto the data bus.

MODE SELECTION TABLE

Control Logic					
$\overline{DS1}$	**$\overline{DS2}$**	**A/$\overline{B}$**	**R/$\overline{W}$**	**Mode**	**DAC**
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A&C
L	L	L	L	WRITE	B&D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

L = Low State, H = High State, X = Irrelevant

BASIC APPLICATIONS

Some basic circuit configurations are shown in Figures 6 and 7. Figure 6 shows the DAC8408 connected in a unipolar configuration (2-Quadrant Multiplication), and Table I shows the Code Table. Resistors R1, R2, R3, and R4 are used to trim full scale output. Full-scale output voltage = V_{REF} –1 LSB = V_{REF} $(1–2^{-8})$ or $V_{REF} \times (255/256)$ with all digital inputs high. Low temperature coefficient (approximately 50 ppm/°C) resistors or trimmers should be selected if used. Full scale can also be adjusted using V_{REF} voltage. This will eliminate resistors R1, R2, R3, and R4. In many applications, R1 through R4 are not required, and the maximum gain error will then be that of the DAC.

Each DAC exhibits a variable output resistance that is code-dependent. This produces a code-dependent, differential nonlinearity term at the amplifier's output which can have a maximum value of 0.67 × the amplifier's offset voltage. This differential nonlinearity term adds to the R-2R resistor ladder differential-nonlinearity; the output may no longer be monotonic. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (1 LSB = $2^{-8} \times V_{REF}$ or $1/256 \times V_{REF}$), or less than 3.9 mV over the operating temperature range. Zero-scale output voltage (with all digital inputs low) may be adjusted using the op amp offset adjustment. Capacitors C1, C2, C3, and C4 provide phase compensation and help prevent overshoot and ringing when using high speed op amps.

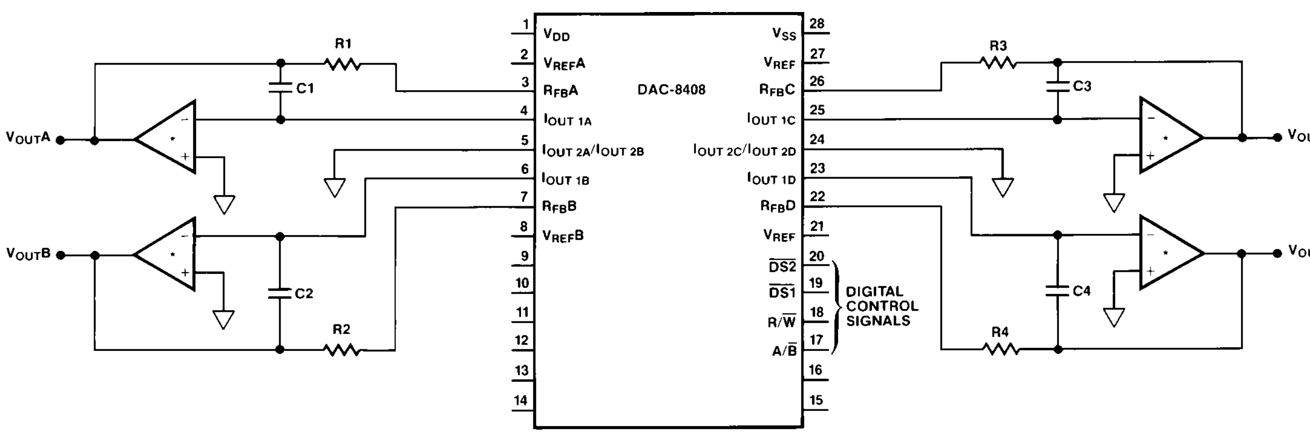
Figure 7 shows the recommended circuit configuration for the bipolar operation (4-quadrant multiplication), and Table II shows the Code Table. Trimmer resistors R17, R18, R19, and R20 are used only if gain error adjustments are required and range between 50 Ω and 1000 Ω. Resistors R21, R22, R23, and R24 will range betwen 50 Ω and 500 Ω. If these resistors are used, it is essential that resistor pairs R9–R13, R10–R14, R11–R15, R12–R16 are matched both in value and tempco. They should be within 0.01%; wire wound or metal foil types are preferred for best temperature coefficient matching. The circuits of Figure 6 and 7 can either be used as a fixed reference D/A converter, or as an attenuator with an ac input voltage.

Table I. Unipolar Binary Code Table (Refer to Figure 6)

DAC Data Input MSB LSB	Analog Output
1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{256}\right) = \frac{-V_{IN}}{2}$
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

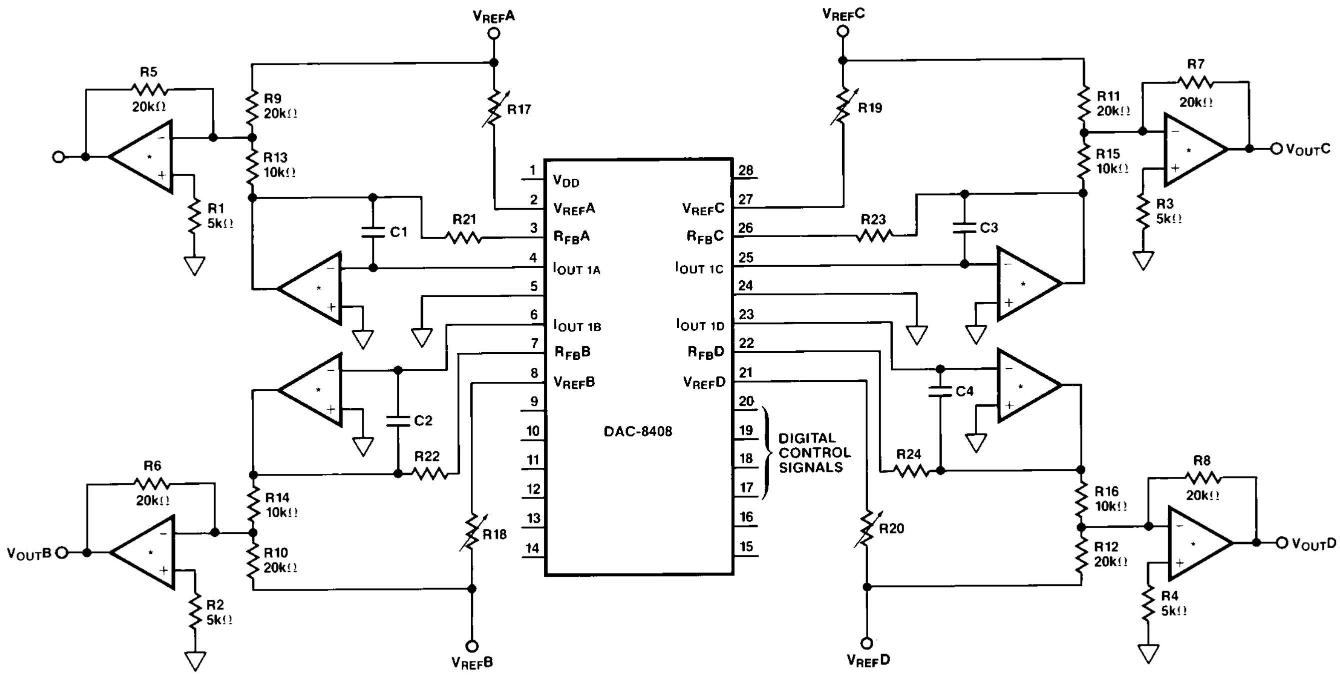
NOTE

1 LSB = $(2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$



*ALL AMPLIFIERS ARE OP-27s, 1/4 OP-420s, OR 1/4 OP-421s.

Figure 6. Quad DAC Unipolar Operation (2-Quadrant Multiplication)



*ALL AMPLIFIERS ARE OP-27s, 1/4 OP-420s, OR 1/4 OP-421s.

Figure 7. Quad DAC Bipolar Operation (4-Quadrant Multiplication)

Table II. Bipolar (Offset Binary) Code Table (Refer to Figure 7)

DAC Data Input MSB LSB	Analog Output (DAC A OR DAC B)
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right)$

NOTE

$1\ LSB = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

APPLICATION HINTS

General Ground Management: AC or transient voltages between AGND and DGND can appear as noise at the DAC8408's analog output. Note that in Figures 5 and 6, I_{OUT2A}/I_{OUT2B} and $I_{OUT\ 2C}/I_{OUT\ 2D}$ are connected to AGND. Therefore, it is recommended that AGND and DGND be tied together at the DAC8408 socket. In systems where AGND and DGND are tied together on the backplane, two diodes (1N914 or equivalent) should be connected in inverse parallel between AGND and DGND.

Write Enable Timing: During the period when both $\overline{DS}$ and $R/\overline{W}$ are held low, the DAC latches are transparent and the analog output responds directly to the digital data input. To prevent unwanted variations of the analog output, the $R/\overline{W}$ should not go low until the data bus is fully settled (DATA VALID).

SINGLE SUPPLY, VOLTAGE OUTPUT OPERATION

The DAC8408 can be connected with a single +5 V supply to produce DAC output voltages from 0 V to +1.5 V. In Figure 8, the DAC8408 R-2R ladder is inverted from its normal connection. A +1.500 V reference is connected to the current output pin 4 ($I_{OUT\ 1A}$), and the normal V_{REF} input pin becomes the DAC output. Instead of a normal current output, the R-2R ladder outputs a voltage. The OP-490, consisting of four precision low power op amps that can operate its inputs and outputs to zero volts, buffers the DAC to produce a low impedance output voltage from 0 V to +1.5 V full-scale. Table III shows the code table.

With the supply and reference voltages as shown, better than 1/2 LSB differential and integral nonlinearity can be expected. To maintain this performance level, the +5 V supply must not drop below 4.75 V. Similarly, the reference voltage must be no higher than 1.5 V. This is because the CMOS switches require a minimum level of bias in order to maintain the linearity performance.

Table III. Single Supply Binary Code Table (Refer to Figure 8)

DAC Data Input MSB LSB	Analog Output
1 1 1 1 1 1 1 1	$V_{REF}\left(\frac{255}{256}\right)$, +1.4941 V
1 0 0 0 0 0 0 1	$V_{REF}\left(\frac{129}{256}\right)$, +0.7559 V
1 0 0 0 0 0 0 0	$V_{REF}\left(\frac{128}{256}\right)$, +0.7500 V
0 1 1 1 1 1 1 1	$V_{REF}\left(\frac{127}{256}\right)$, +0.7441 V
0 0 0 0 0 0 0 1	$V_{REF}\left(\frac{1}{256}\right)$, +0.0059 V
0 0 0 0 0 0 0 0	$V_{REF}\left(\frac{0}{256}\right)$, 0.0000 V

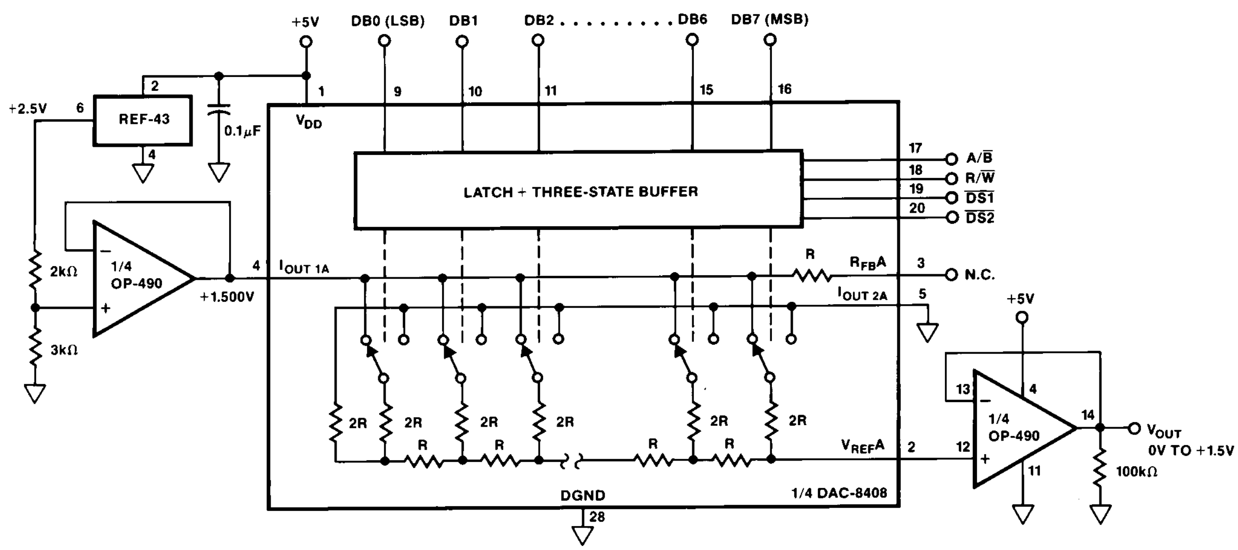


Figure 8. Unipolar Supply, Voltage Output DAC Operation

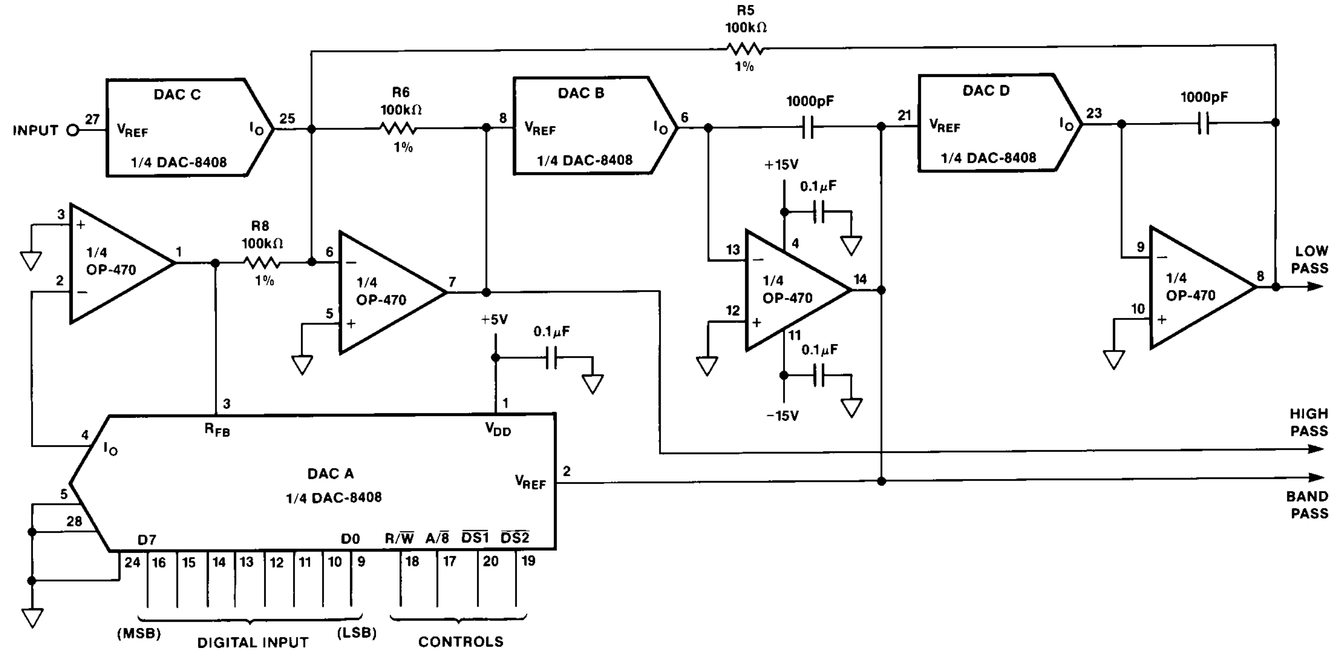
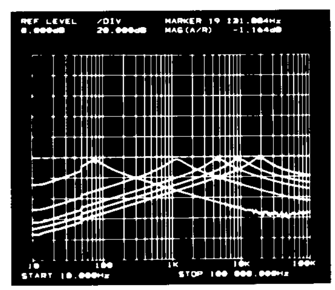


Figure 9. A Digitally Programmable Universal Active Filter

A DIGITALLY PROGRAMMABLE ACTIVE FILTER

A powerful D/A converter application is a programmable active filter design as shown in Figure 9. The design is based on the state-variable filter topology which offers stable and repeatable filter characteristics. DAC B and DAC D can be programmed in tandem with a single digital byte load which sets the center frequency of the filter. DAC A sets the Q of the filter. DAC C sets the gain of the filter transfer function. The unique feature of this design is that varying the gain of filter does not affect the Q of the filter. Similarly, the reverse is also true. This makes the programmability of the filter extremely reliable and predictable. Note that low-pass, high-pass, and bandpass outputs are available. This sophisticated function is achieved in only two IC packages.

The network analyzer photo shown in Figure 10 superimposes five actual bandpass responses ranging from the lowest frequency of 75 Hz (1 LSB ON) to a full-scale frequency of 19.132 kHz (all bits ON), which is equivalent to a 256 to 1 dynamic range. The frequency is determined by $f_C = 1/2\pi RC$ where R is the ladder resistance (R_{IN}) of the DAC8408, and C is 1000 pF. Note that from device to device, the resistance R_{IN} varies. Thus some tuning may be necessary.



THE CIRCUIT PROVIDES FULL 8-BIT
(> 2 DECADE) DYNAMIC RANGE OF
FREQUENCY CONTROL

Figure 10. Programmable Active Filter Band-Pass Frequency Response

All components used are available off-the-shelf. Using low drift thin-film resistors, the DAC8408 exhibits very stable performance over temperature. The wide bandwidth of the OP-470 produces excellent high frequency and high Q response. In addition, the OP470's low input offset voltage assures an unusually low dc offset at the filter output.

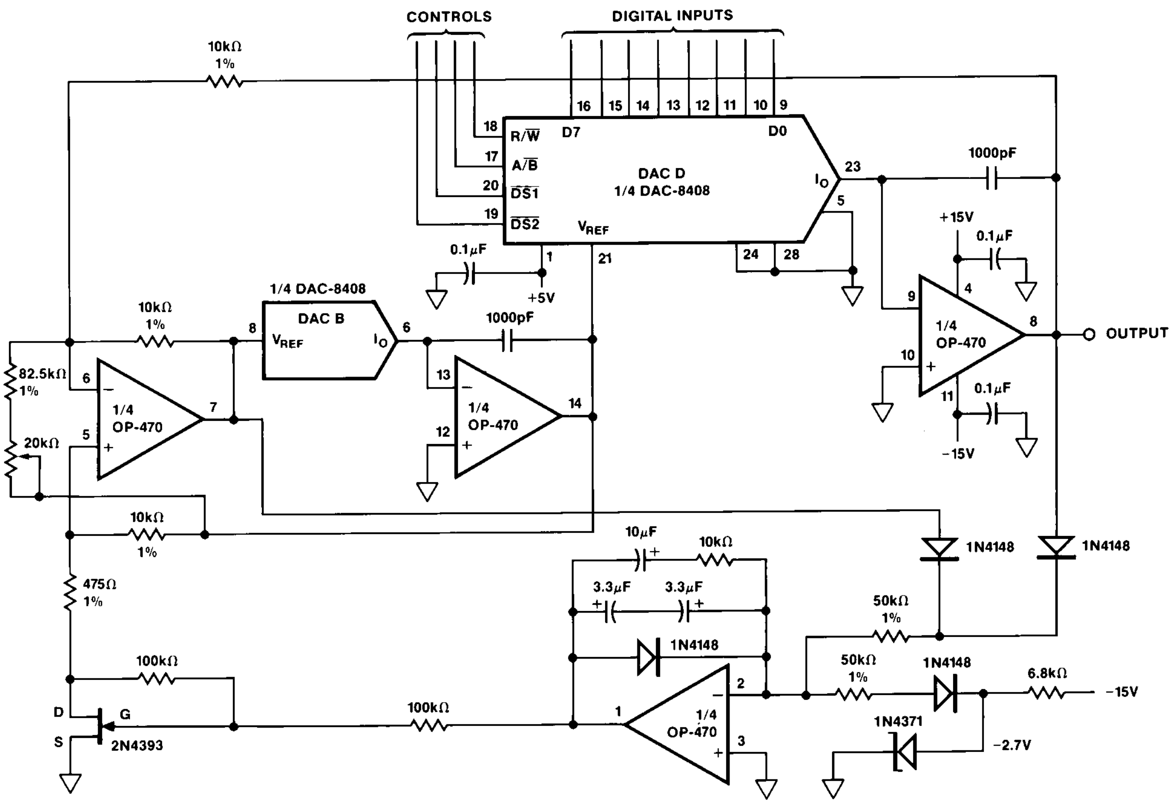


Figure 11. A Digitally Programmable, Low-Distortion Sinewave Oscillator

A LOW-DISTORTION, PROGRAMMABLE SINEWAVE OSCILLATOR

By varying the previous state-variable filter topology slightly, one can obtain a very low distortion sinewave oscillator with programmable frequency feature as shown in Figure 11. Again, DAC B and DAC D in tandem control the oscillating frequency based on the relationship $f_C = 1/2\pi RC$. Positive feedback is accomplished via the 82.5 kΩ and the 20 kΩ potentiometer. The Q of the oscillator is determined by the ratio of 10 kΩ and 475Ω in series with the FET transistor, which acts as an automatic gain control variable resistor. The AGC action maintains a very stable sinewave amplitude at any frequency. Again, only two ICs accomplish a very useful function.

At the highest frequency setting, the harmonic distortion level measures 0.016%. As the frequencies drop, distortion also drops to a low of 0.006%. At the lowest frequency setting, distortion came back up to a worst case of 0.035%.

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Package/Price Information

Quad 8-Bit Multiplying CMOS D/A Converter with Memory

Model	Status	Package Description	Pin Count	Temperature Range	Price* (100-499)
5962-8967801XA	PRODUCTION	CERDIP GLASS SEAL	28	MILITARY	$53.66
5962-8967802XA	PRODUCTION	CERDIP GLASS SEAL	28	MILITARY	$45.79
DAC8408AT/883C	PRODUCTION	CERDIP GLASS SEAL	28	MILITARY	$48.79
DAC8408BTC/883C	PRODUCTION	CER. LEADLESS CHIP CARRIER	28	MILITARY	$57.20
DAC8408ET	PRODUCTION	CERDIP GLASS SEAL	28	INDUSTRIAL	-
DAC8408FP	PRODUCTION	PLASTIC/EPOXY DIP	28	INDUSTRIAL	$8.83
DAC8408FPC	PRODUCTION	PLASTIC LEAD CHIP CARRIER	28	INDUSTRIAL	$9.71
DAC8408FS	PRODUCTION	STD S.O. PKG (SOIC)	28	INDUSTRIAL	$9.71
DAC8408FT	PRODUCTION	CERDIP GLASS SEAL	28	INDUSTRIAL	-
DAC8408GBC	PRODUCTION	CHIPS/DIE SALES	-	TBD	$18.26
DAC8408GP	PRODUCTION	PLASTIC/EPOXY DIP	28	INDUSTRIAL	$14.85

* This price is provided for budgetary purposes as recommended list price in U.S. Dollars per unit in the stated volume. Pr
Boards and Kits is based on 1-piece pricing. View Pricing and Availability for further information.