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AD7091R FMC-SDP Interposer & Evaluation Board / Xilinx AC701 Reference Design

Supported Devices

- AD7091R

Evaluation Boards

- EVAL-AD7091RSDZ

Overview

This document presents the steps to setup an environment for using the **EVAL-AD7091RSDZ** evaluation board together with the Xilinx KC705 FPGA board and the Xilinx Embedded Development Kit (EDK). Below is presented a picture of the EVAL-AD7091RSDZ Evaluation Board with the Xilinx KC705 board.

For component evaluation and performance purposes, as opposed to quick prototyping, the user is directed to use the part evaluation setup. This consists of:

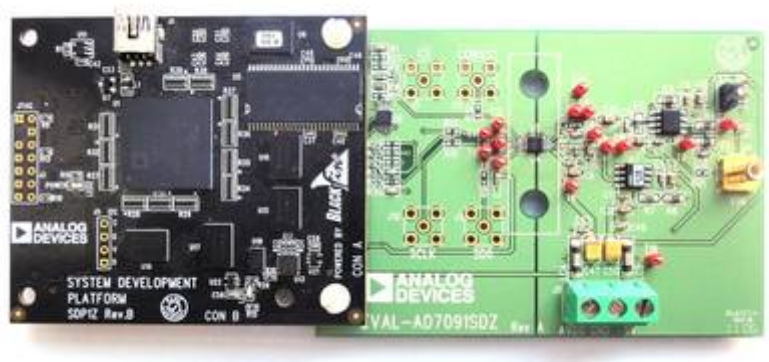
- 1. A controller board like the SDP-B (EVAL-SDP-CS1Z)
- 2. The component SDP compatible product evaluation board
- 3. Corresponding PC software (shipped with the product evaluation board)

The SDP-B controller board is part of Analog Devices System Demonstration Platform (SDP). It provides a high speed USB 2.0 connection from the PC to the component evaluation board. The PC runs the evaluation software. Each evaluation board, which is an SDP compatible daughter board, includes the necessary installation file required for performance testing.

Note: it is expected that the analog performance on the two platforms may differ.

28 Sep 2012 09:32 · Adrian Costina

Below is presented a picture of **SDP-B** Controller Board with the **EVAL-AD7091RSDZ** Evaluation Board.



The AD7091R is a 12-bit successive approximation analog-to-digital converter (ADC) that offers ultralow power consumption (typically 349 µA at 3 V and 1 MSPS) while achieving fast throughput rates (1 MSPS with a 50 MHz SCLK). Operating from a single 2.7 V to 5.25 V power supply, the part contains a wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 7 MHz. The AD7091R also features an on-chip conversion clock, accurate reference, and high speed serial interface.

The **EVAL-AD7091RSDZ** evaluation board is a member of a growing number of boards available for the **SDP**. They were designed to help customers evaluate performance or quickly prototype new **AD7091R** circuits and reduce design time.

More information

- AD7091R Product Info - pricing, samples, datasheet
- EVAL-AD7091RSDZ evaluation board user guide
- Xilinx AC705 FPGA board

Getting Started

The first objective is to ensure that you have all of the items needed and to install the software tools so that you are ready to create and run the evaluation project.

Required Hardware

- Xilinx AC705 FPGA board
- FMC-SDP adapter board
- **EVAL-AD7091RSDZ** evaluation board

Required Software

- Xilinx ISE 14.6
- A UART terminal (Tera Term/Hyperterminal/Termite), baud rate 115200.

Downloads

- **IP Core Files:** https://github.com/analogdevicesinc/fpgahdl_xilinx/tree/master/cf_lib/edk/pcores/axi_ad7091_v1_00_a
- **EDK AC701 Reference project:** https://github.com/analogdevicesinc/fpgahdl_xilinx/tree/master/cf_sdp_adc/cf_ad7091_ac701
- **AD7091R Drivers:** https://github.com/analogdevicesinc/no-OS/tree/master/device_drivers/AD7091
- **ADC specific files:** https://github.com/analogdevicesinc/no-OS/tree/master/platform_drivers/Xilinx/SDP_ADC/AD7091
- **Platform specific files:** https://github.com/analogdevicesinc/no-OS/tree/master/platform_drivers/Xilinx/SDP_Common

Run the Demonstration Project

Hardware Setup

Before connecting the ADI evaluation board to the Xilinx KC705 make sure that the VADJ_FPGA voltage of the KC705 is set to 3.3V. For more details on how to change the setting for VADJ_FPGA visit the Xilinx KC705 product page.

- Use the FMC-SDP interposer to connect the ADI evaluation board to the Xilinx KC705 board on the FMC LPC connector.
- Connect the JTAG and UART cables to the KC705 and power up the FPGA board.
- Power the ADI evaluation board.
- Start a UART terminal and set the baud rate to 115200 bps.

The next step is to setup the software project.

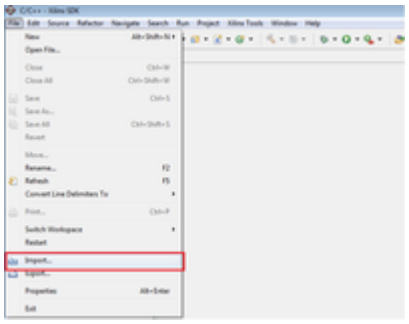
Software Project Setup

The next steps should be followed to recreate the software project of the reference design:

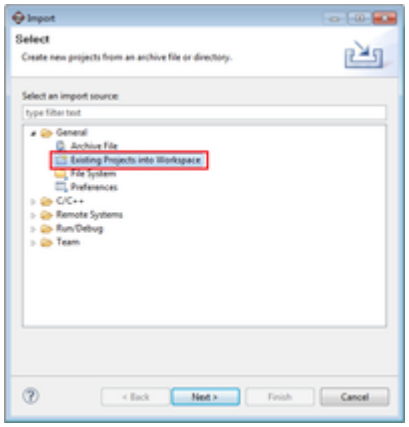
- First clone the AC701 Reference project for AD7091 and the ADI IP cores from Github to your

computer, by using the following link: https://github.com/analogdevicesinc/fpgahdl_xilinx/

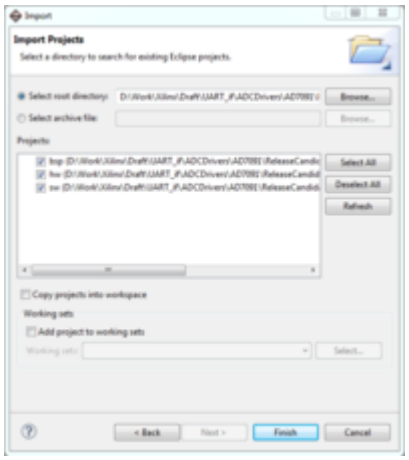
- Copy the folder **../fpgahdl_xilinx/cf_lib** and **../fpgahdl_xilinx/cf_sdp_adc/cf_ad7091_ac701** to your working directory
- Open a Xilinx SDK and setup your workspace to **%Working directory%/cf_ad7091_ac701/SDK/SDK_Workspace**
- In the SDK select the **File→Import** menu option to import the software project into your workspace.



- In the *Import* window select the **General→Existing Projects into Workspace** option.

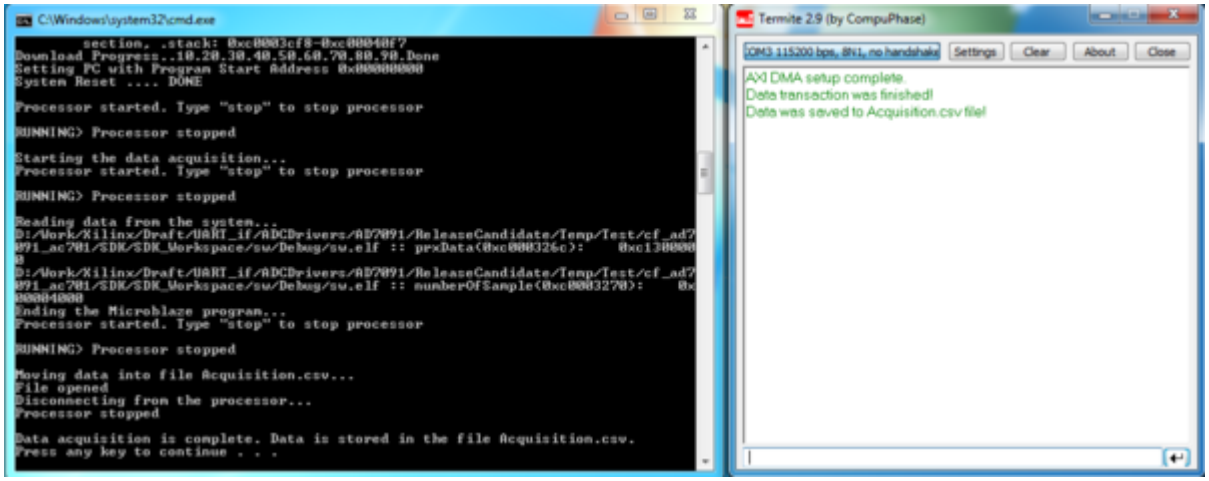


- In the *Import Projects* window select the **%Working directory%/cf_ad7091_ac701/** folder as root directory and verify if all the three project (**hw**, **bsp**, **sw**) are checked.

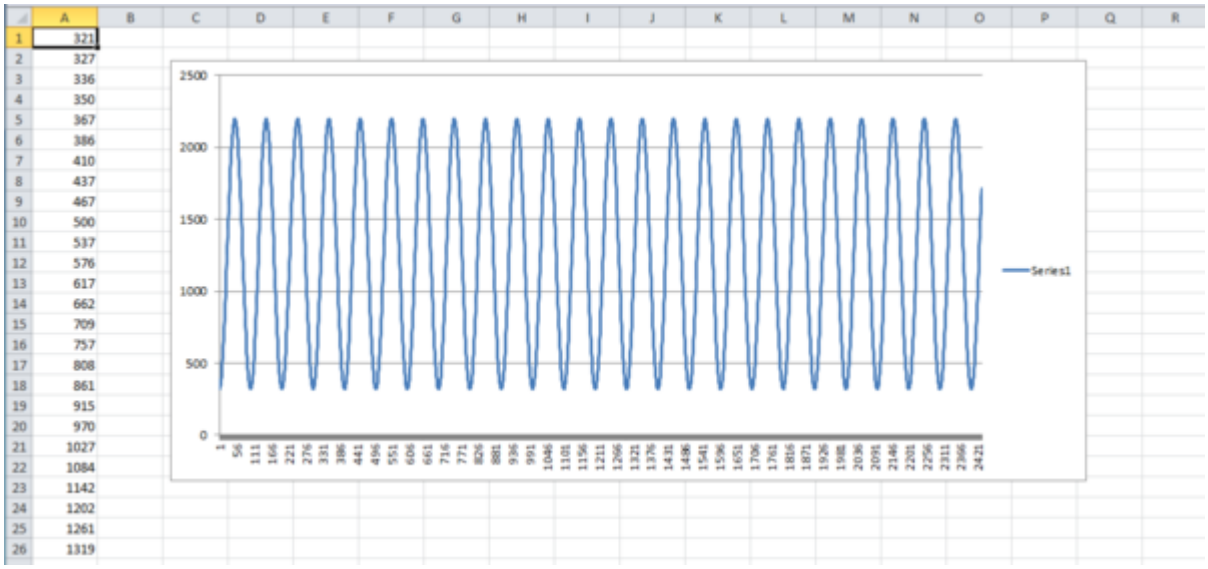


- The Project Explorer window now shows the projects that exist in the workspace without software files.

- Now you have to add the source files to your project. You can download all the source files for the current reference project using the links from the **Downloads** section. List of source files for the current project is:
  - **Driver files** : *ad7091.h* and *ad7091.c*
  - **Platform specific files** : *Communication.h*, *Communication.c*, *TIME.h* and *TIME.c*
  - **ADC specific files** : *main.c* and *xdma_config.h*
- All these files must be copied into the **%Working directory%/cf_ad7091_ac701/SDK/SDK_Workspace/sw/src/** folder.
- The SDK should automatically build the project and the Console window will display the result of the build. If the build is not done automatically, select the Project→Build Automatically menu option.
- If the project was built without any errors, you need to download the data capture script, from here. Copy the **Data_capture** folder to your working directory.
- Run the **data_capture.bat** script. If the acquisition is finished with success, it should appear a file called **Acquisition.csv** with the result of the conversion.



- By default the length of a transaction is 16k samples. The input signal used in this reference design was a 10 Khz sine wave.



More information

- ask questions about the FPGA reference design
- Example questions:
  - AXI_AD9361 Core by maxpayne
  - AD9625 Xilinx code by ADIguy
  - FPGA <=> DAC AD9122 digital interface timing validation (VC707+FMCOMMS1) by aismekalov
  - setup and hold time of axi_ad9361 hdl design by bhatnagar.vaibhav81
  - Tx_frame signal missing on the test point AD9364 by bhatnagar.vaibhav81

28 May 2012 14:18