CY7C291A

2K x 8 Reprogrammable PROM

Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - — 20 ns (Commercial)
  - — 35 ns (Military)
- Low power
  - — 660 mW (Commercial and Military)
- Low standby power
  - — 220 mW (Commercial and Military)
- EPROM technology 100% programmable
- Slim 300-mil or standard 600-mil packaging available
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding >2001V static discharge

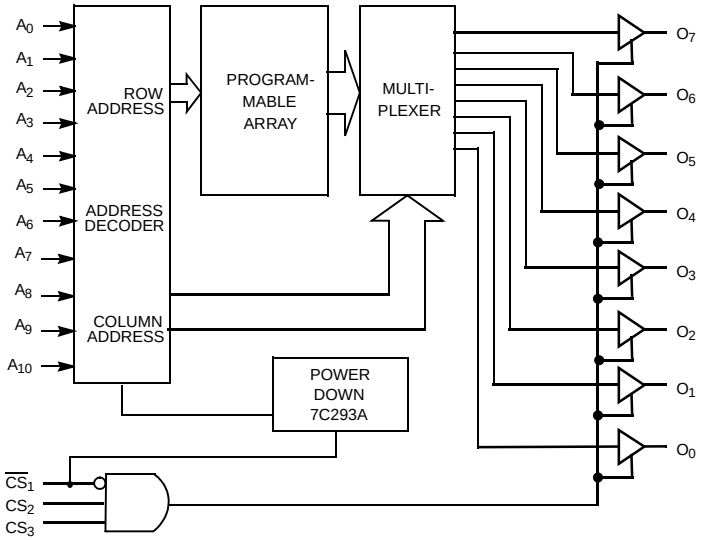
Functional Description

The CY7C291A is a high-performance 2K-word by 8-bit CMOS PROM. It is packaged in a 300-mil ceramic package which may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C291A is a plug-in replacement for bipolar devices and offers the advantage of lower power, reprogrammability, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

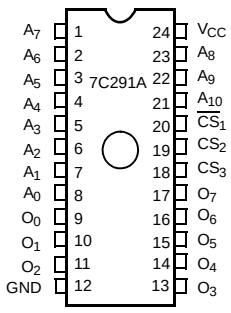
A read is accomplished by placing an active LOW signal on $\overline{CS_1}$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address line (A_0–A_{10}) will become available on the output lines (O_0–O_7).

Logic Block Diagram

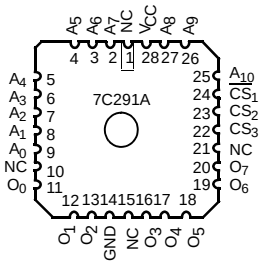


Pin Configurations

DIP
Top View



LCC/PLCC (Opaque Only)
Top View



Window available

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Selection Guide

			7C291A-20	7C291A-25	7C291A-35 7C291AL-35	7C291A-50	Unit
Maximum Access Time			20	25	35	50	ns
Maximum Operating Current	Standard	Commercial	120	90	90	90	mA
		Military			90		mA
	L	Commercial			60		mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –3.0V to +7.0V

DC Program Voltage..... 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ±10%
Military[1]	–55°C to + 125°C	5V ±10%

Note
1. T_A is the "instant on" case temperature.

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Electrical Characteristics Over the Operating Range[2, 3]

Parameter	Description	Test Conditions		7C291A-20		7C291A-25		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 3				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND		–20	–90	–20	–90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		90	mA
I_{SB}	Standby Supply Current (7C293A Only)	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}	Com'l		40		30	mA
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

Notes
2. See the last page of this specification for Group A subgroup testing information.
3. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

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Electrical Characteristics Over the Operating Range[2,3] (continued)

Parameter	Description	Test Conditions		7C291AL-35		7C291A-35 7C291A-50		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 3				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND		–20	–90	–20	–90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., V_{IN} = 2.0V I_{OUT} = 0 mA	Commercial		60		90	mA
			Military				90	
I_{SB}	Standby Supply Current (7C293A Only)	V_{CC} = Max., $\overline{CS_1}$ = V_{IH}	Commercial		30		30	mA
			Military				40	
V_{PP}	Programming Supply Voltage			12	13	12	13	V
I_{PP}	Programming Supply Current				50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4	V

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

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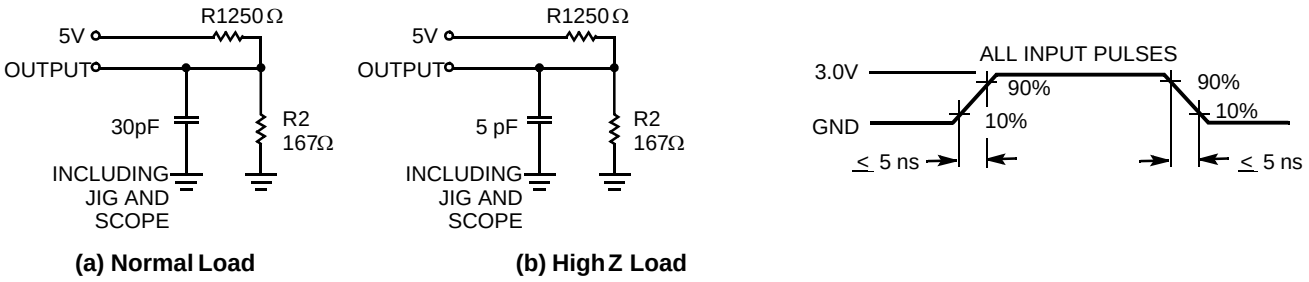
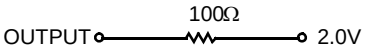
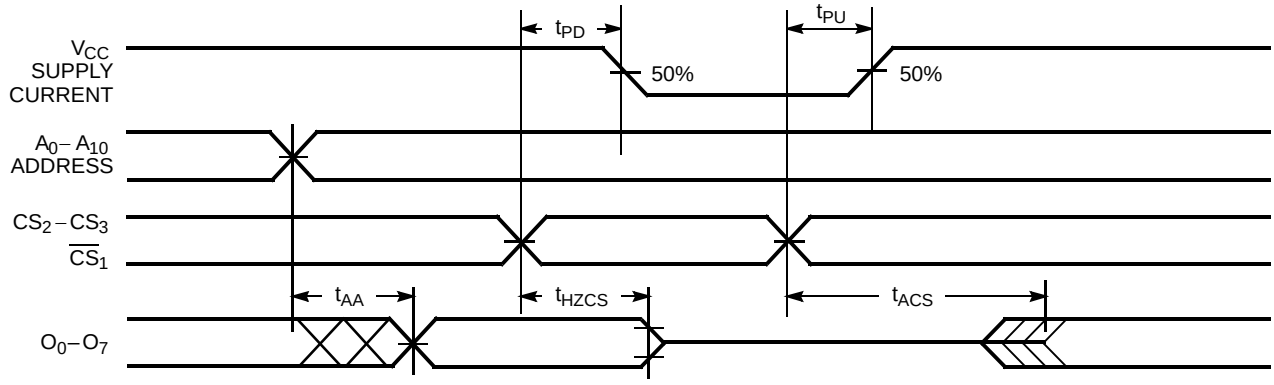
AC Test Loads and Waveforms[3]



(a) Normal Load **(b) High Z Load**

Equivalent to: THÉVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[2, 3]

Parameter	Description	7C291A-20		7C291A-25		7C291A-35 7C291AL-35		7C291A-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		35		50	ns
t_{HZCS1}	Chip Select Inactive to High Z		15		15		20		20	ns
t_{ACS1}	Chip Select Active to Output Valid		15		15		20		20	ns
t_{HZCS2}	Chip Select Inactive to High Z		22		27		35		45	ns
t_{ACS2}	Chip Select Active to Output Valid		22		27		35		45	ns
t_{PU}	Chip Select Active to Power-Up	0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power-Down		22		27		35		45	ns

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Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase these PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes.

These PROMs need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Information

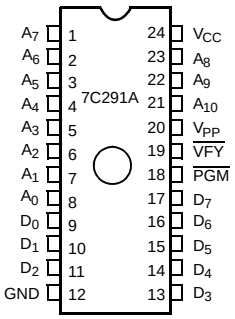
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

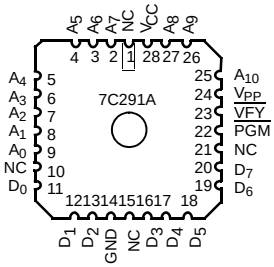
Mode		Pin Function[5]				
	Read or Output Disable	**A_{10}–A_0**	**$\overline{CS_3}$**	**$\overline{CS_2}$**	**$\overline{CS_1}$**	**O_7–O_0**
	Other	**A_{10}–A_0**	**$\overline{PGM}$**	**$\overline{VFY}$**	**V_{PP}**	**D_7–D_0**
Read		A_{10}–A_0	V_{IH}	V_{IH}	V_{IL}	O_7–O_0
Output Disable[6]		A_{10}–A_0	X	X	V_{IH}	High Z
Output Disable		A_{10}–A_0	X	V_{IL}	X	High Z
Output Disable		A_{10}–A_0	V_{IL}	X	X	High Z
Program		A_{10}–A_0	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Program Verify		A_{10}–A_0	V_{IHP}	V_{ILP}	V_{PP}	O_7–O_0
Program Inhibit		A_{10}–A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		A_{10}–A_0	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Blank Check Zeros		A_{10}–A_0	V_{IHP}	V_{ILP}	V_{PP}	Zeros

Figure 1. Programming Pinouts

DIP
Top View



LCC/PLCC (Opaque Only)
Top View



Notes
5. X = “don’t care” but not to exceed V_{CC} +5%.
6. The power-down mode for the CY7C293A is activated by deselecting $\overline{CS_1}$.

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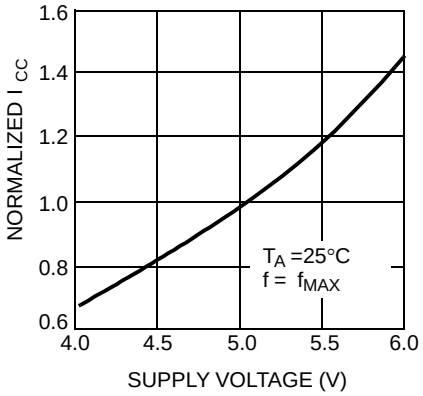
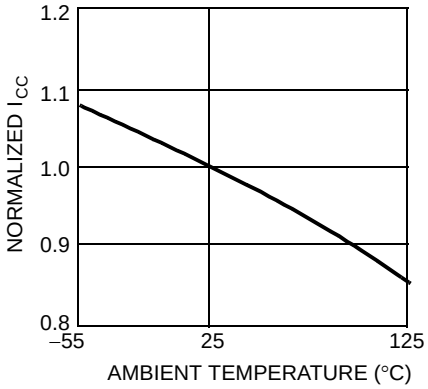
Typical DC and AC Characteristics

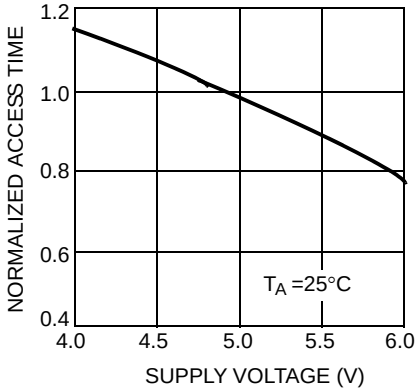
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



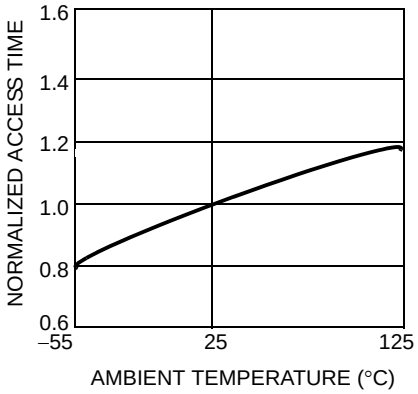
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



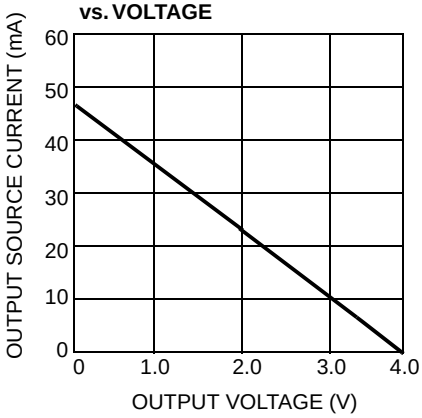
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



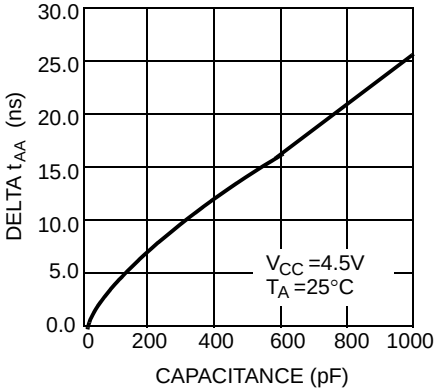
NORMALIZED ACCESS TIME vs. TEMPERATURE



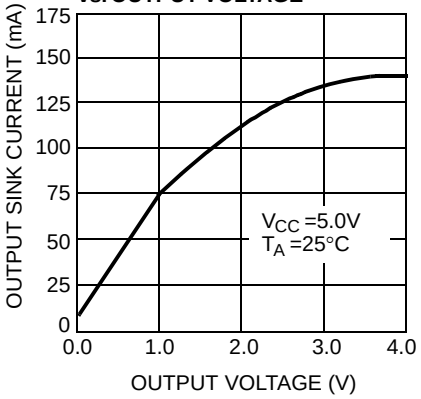
OUTPUT SOURCE CURRENT vs. VOLTAGE



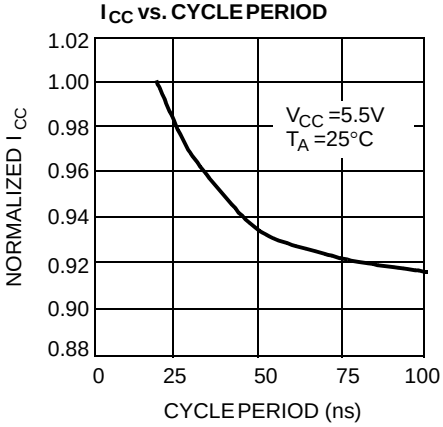
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



ICC vs. CYCLE PERIOD



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Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	120	CY7C291A-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
25	90	CY7C291A-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291A-25PC	P13	24-Lead (300-Mil) Molded DIP	
35	60	CY7C291AL-35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291AL-35PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291AL-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	90	CY7C291A-35JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C291A-35PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C291A-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
	120	CY7C291A-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
50	90	CY7C291A-50PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
		CY7C291A-50WMB	W14	24-Lead (300-Mil) Windowed CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962-87650	01LX	CY7C291-50WMB
5962-87650	03LX	CY7C291-35WMB
5962-88734	023X	CY7C291A-35LMB
5962-88734	033X	CY7C291A-35LMB
5962-88734	04LX	CY7C291A-25DMB
5962-88734	043X	CY7C291A-25LMB

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Package Diagrams

Figure 2. 24-Lead (300-Mil) CerDIP D14

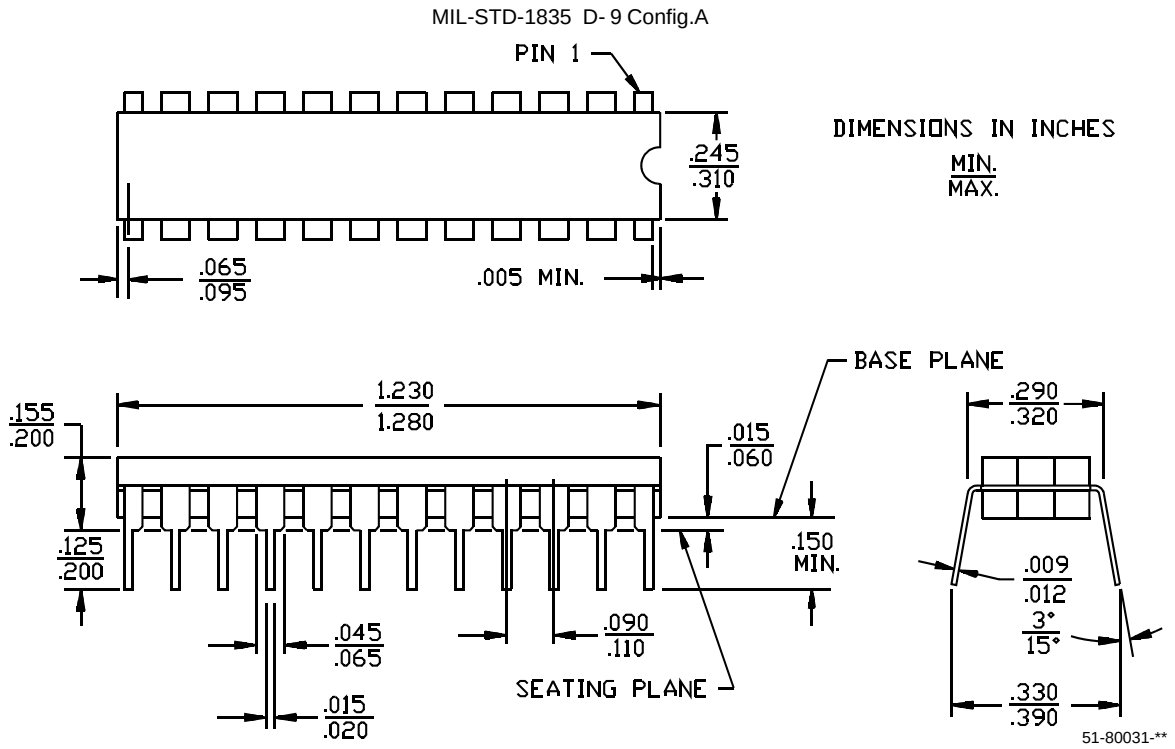
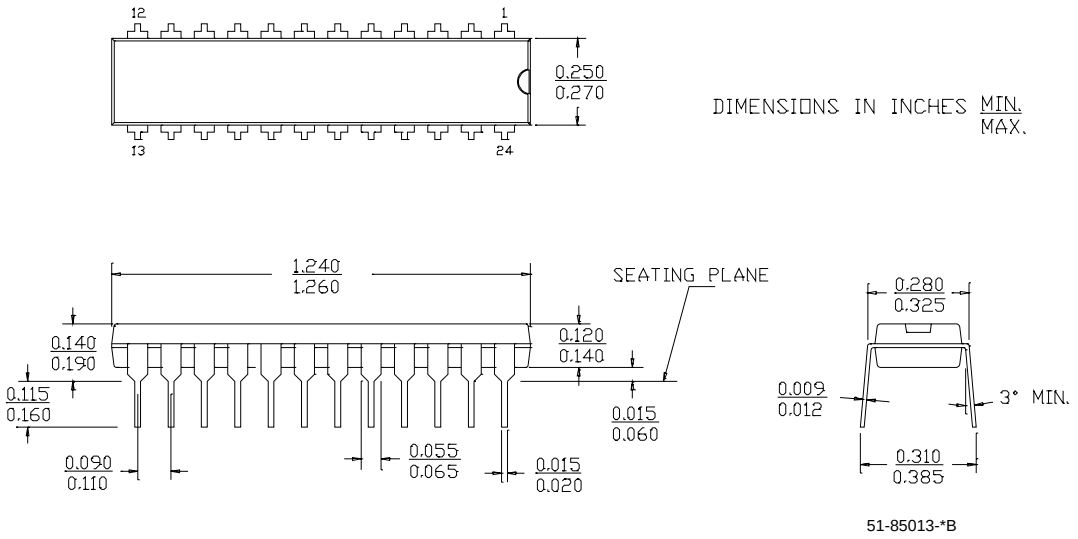


Figure 3. 24-Lead (300-Mil) PDIP P13



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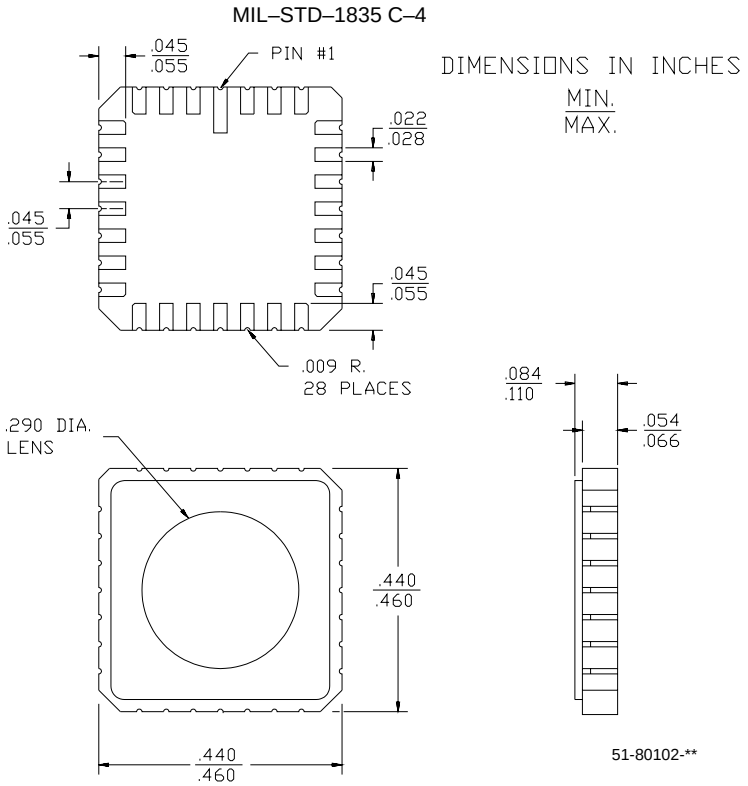
Package Diagrams (continued)

Figure 4. 28-Pin Windowed Leadless Chip Carrier Q64



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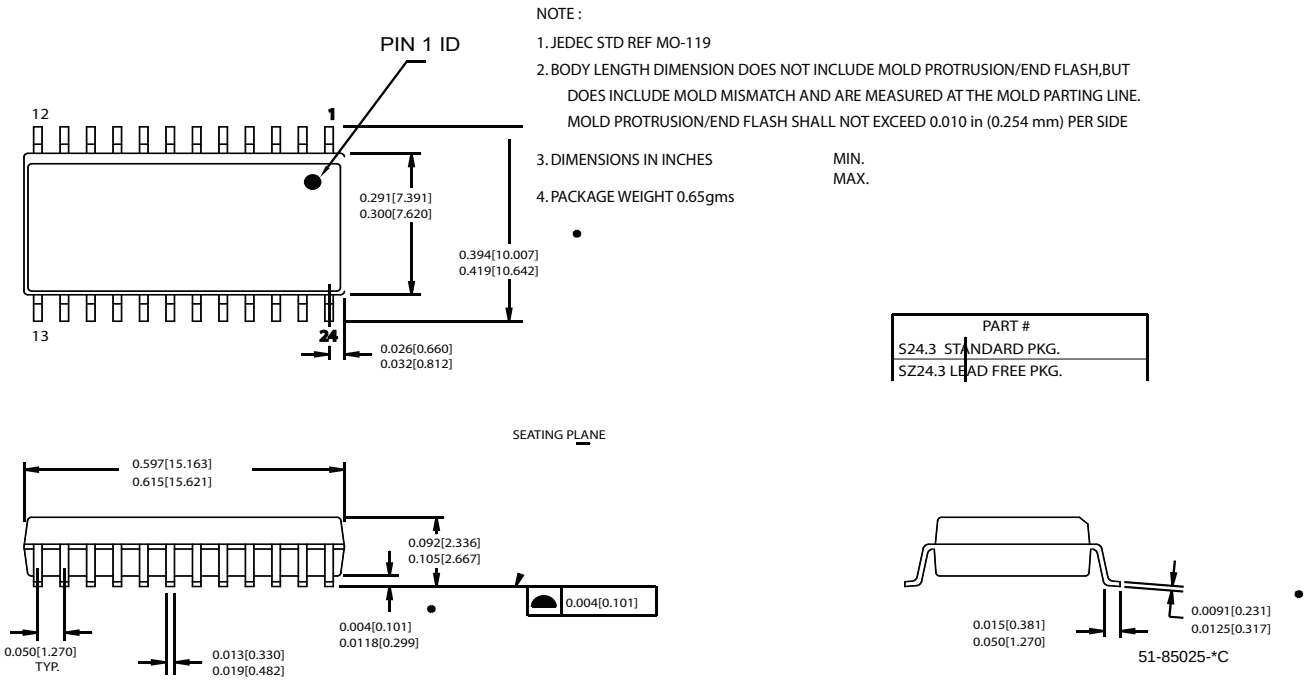
Package Diagrams (continued)

Figure 5. 24 Lead (300 Mil) SOIC - S13



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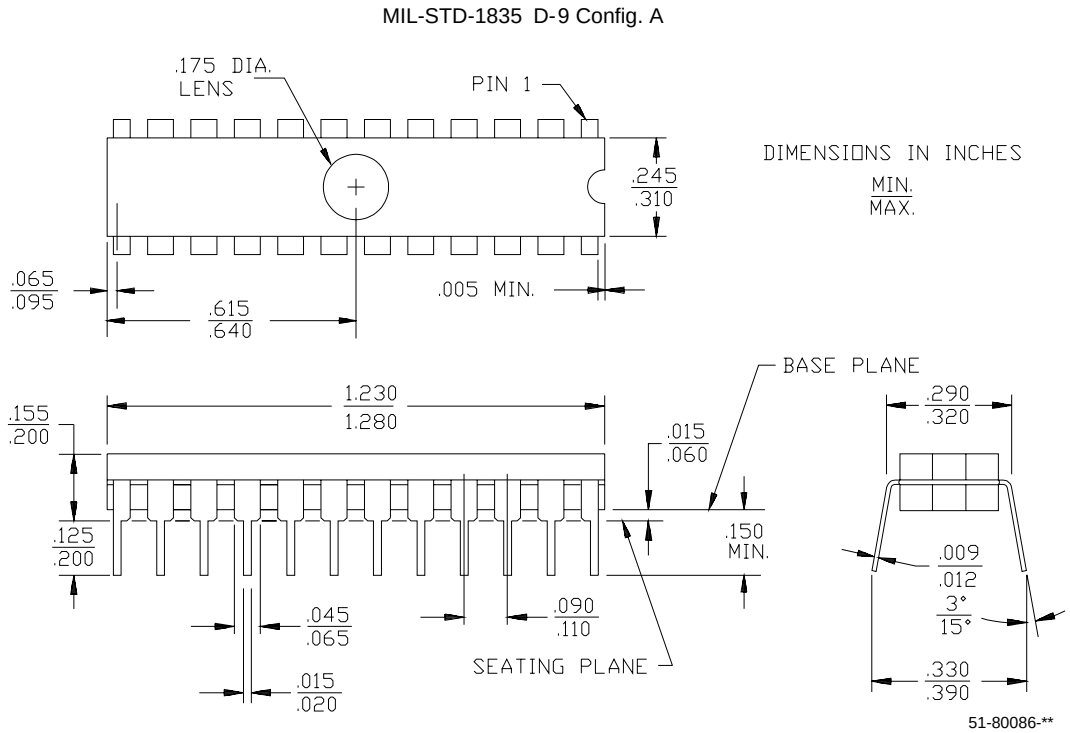
Package Diagrams (continued)

Figure 6. 24-Lead (300-Mil) Windowed CerDIP W14



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Document History Page

Document Title: CY7C291A 2K x 8 Reprogrammable PROM Document Number: 38-04011				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114138	03/18/02	DSG	Changed from Spec number: 38-00075 to 38-04011
*A	118905	10/11/02	GBI	Updated ordering information
*B	499562	See ECN	PCI	Updated ordering information

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