QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 552

12-BIT 10MSPS ADC

LTC1420CGN

DESCRIPTION

Demonstration circuit 552 is a quick way to try the LTC1420, and gives a clean, compact example of a PC board layout for the part. For a description of how the LTC1420 operates, please refer to the data sheet on the Linear Technology web-site.

Design files for this circuit board are available. Call the LTC factory.

QUICK START PROCEDURE

CONNECTING THE ANALOG POWER SUPPLIES

The part can run off of a single supply or dual supplies:

Single Supply: VDD=+5V, VSS=0V, GND=0V

Dual Supplies: VDD=+5V, VSS=–5V, GND=0V

CONNECTING THE DIGITAL OUTPUT POWER SUPPLY

OVDD is the supply for the digital output drivers on the part. VCC is the supply for the 74ACT16373 transparent latch that buffers the outputs. For best results, set OVDD=VCC=+3V to +5V. Connect the ground of the digital output supply to GND.

SENSE PIN JUMPERS

JP1, JP2 and JP3 configure the SENSE pin, which sets the voltage reference, VREF.

JP1: SENSE=GND VREF=4.096V

JP2: SENSE=VDD

VREF must be driven externally. Input impedance is about 1kΩ.

JP3: SENSE=VREF VREF=2.048V

GAIN PIN JUMPER

JP4 configures the GAIN pin, which sets the gain of the input PGA.

No jumper: GAIN pin is connected to the GAIN post. Drive externally with CMOS logic levels.

Left 2 pins: GAIN=GND PGA gain = 2x

Right 2 pins: GAIN=VDD PGA gain = 1x

DRIVING THE ANALOG INPUT

Apply the analog input signal to the +AIN BNC connector. The negative analog input can be driven at the –AIN BNC connector. For convenience, the negative analog input can also be connected to VCM or GND with JP5:

JP5 on left two pins: -AIN=GND Dual supply operation

JP5 on right two pins: -AIN=VCM (+2.5V) Single supply operation

The analog input range, Vin = +AIN – -AIN is:

-VREF/2 < VIN < +VREF/2 for PGA gain=1x

-VREF/4 < VIN < +VREF/4 for PGA gain=2x

INPUT RC FILTER

For optimal AC performance, the LTC1420 should have an NPO capacitor across its analog input (C6). This capacitor can be used along with R18 as an input filter to reduce noise in the input signal.

DRIVING THE CLOCK INPUT

Apply the encode clock to the CLK BNC connector. For best performance, the clock should have low jitter and rise and fall times of less than 5ns. R17 is a 50 Ohm resistor that terminates the clock to ground. R17 should be removed if the clock signal source cannot drive a 50 Ohm load.

DIGITAL OUTPUTS

The digital outputs appear at the 40-pin connector on the right side of the board. The signals are the twelve data bits, overflow, and a buffered version of the clock that can be used to latch the data. For best results all wires connected to the output bus should be as short as possible. The output-coding format is selected with JP6:

JP6 on top two pins: 2's complement

JP6 on bottom two pins: straight binary

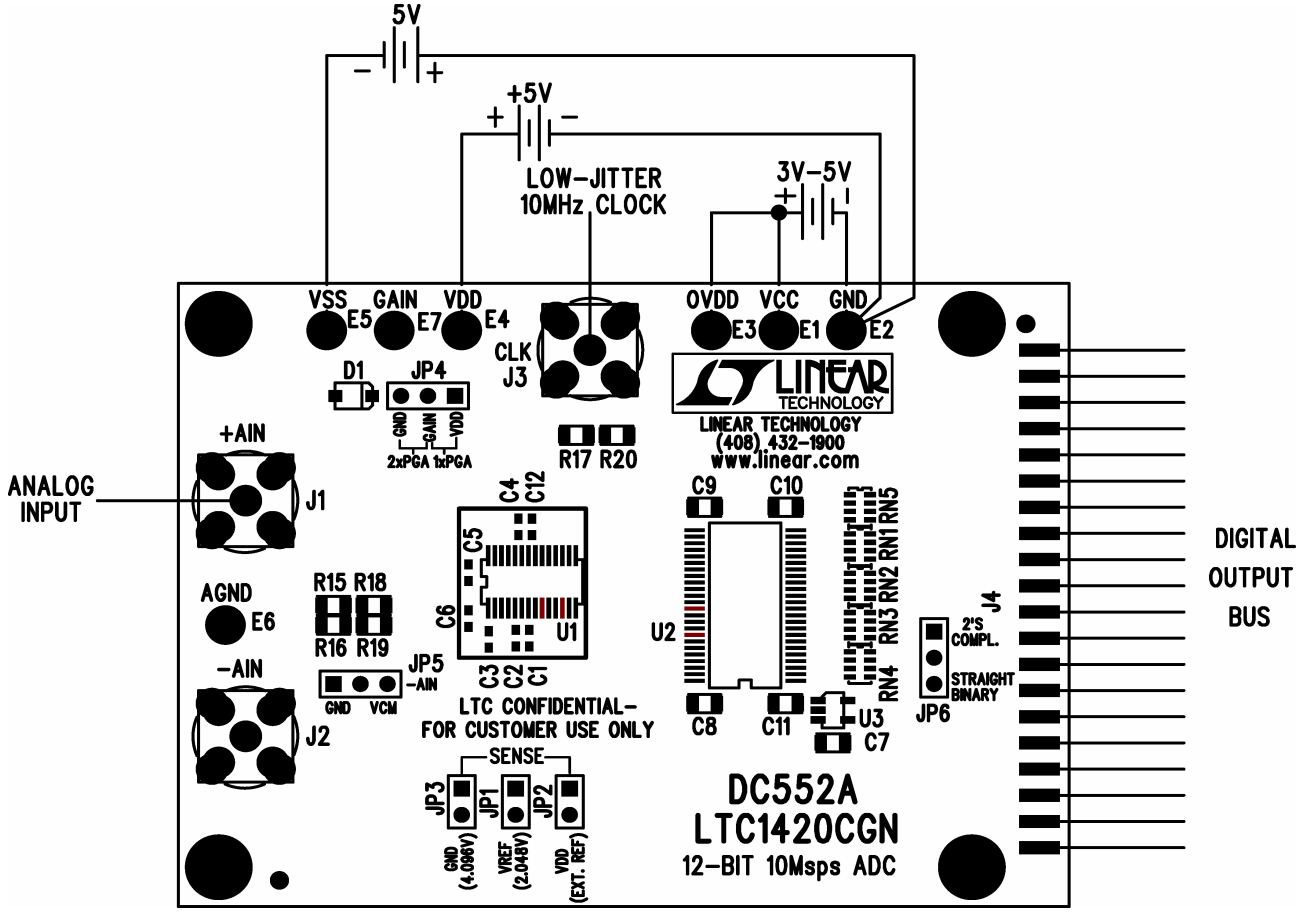

Figure 1. Proper Measurement Equipment Setup