8-/10-/12-Bit High Bandwidth Multiplying DACs with Serial Interface

Data Sheet

AD5426/AD5432/AD5443

FEATURES

2.5 V to 5.5 V supply operation
50 MHz serial interface
10 MHz multiplying bandwidth
2.5 MSPS update rate
INL of ±1 LSB for 12-bit DAC
±10 V reference input
Low glitch energy < 2 nV-s
Extended temperature range −40°C to +125°C
10-lead MSOP
Pin-compatible 8-, 10-, and 12-bit current output DACs
Guaranteed monotonic
4-quadrant multiplication
Power-on reset with brownout detection
Daisy-chain mode
Readback function
0.4 µA typical power consumption

APPLICATIONS

Portable battery-powered applications
Waveform generators
Analog processing
Instrumentation
Programmable amplifiers and attenuators
Digitally controlled calibration
Programmable filters and oscillators
Composite video
Ultrasound
Gain, offset, and voltage trimming

GENERAL DESCRIPTION

The AD5426/AD5432/AD5443[1] are CMOS 8-, 10-, and 12-bit current output digital-to-analog converters (DACs), respectively. These devices operate from a 2.5 V to 5.5 V power supply, making them suitable for battery-powered applications and many other applications.

These DACs use a double buffered, 3-wire serial interface that is compatible with SPI, QSPI™, MICROWIRE, and most DSP interface standards. In addition, a serial data out pin (SDO) allows for daisy-chaining when multiple packages are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with 0s and the DAC outputs are at zero scale.

As a result of manufacturing on a CMOS submicron process, the parts offer excellent 4-quadrant multiplication characteristics with large signal multiplying bandwidths of 10 MHz. The applied external reference input voltage, V_{REF}, determines the full-scale output current. An integrated feedback resistor, R_{FB}, provides temperature tracking and full-scale voltage output when combined with an external current to voltage precision amplifier.

The AD5426/AD5432/AD5443 DACs are available in small, 10-lead MSOPs.

The EV-AD5443/46/53SDZ evaluation board is available for evaluating DAC performance. For more information, see the UG-327 evaluation board user guide.

FUNCTIONAL BLOCK DIAGRAM

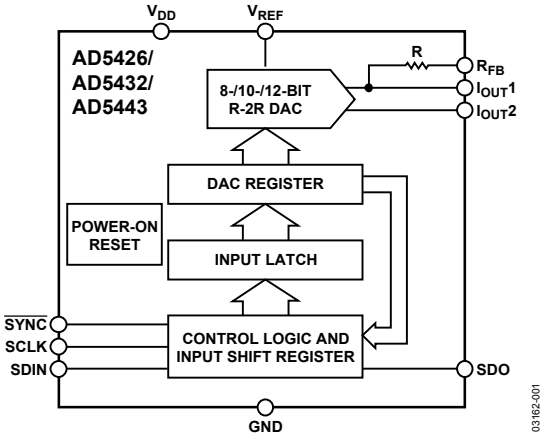

Figure 1.

[1] Protected by U.S. Patent No. 5,689,257.

Rev. H **Document Feedback**

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2/04—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V; temperature range for Y version: −40°C to +125°C; all specifications T_{MIN} to T_{MAX}, unless otherwise noted; dc performance measured with OP177; ac performance with AD8038, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
AD5426					
Resolution			8	Bits	
Relative Accuracy			±0.25	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic
AD5432					
Resolution			10	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5443					
Resolution			12	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			−1/+2	LSB	Guaranteed monotonic
Gain Error			±10	mV	
Gain Error Temperature Coefficient[1]		±5		ppm FSR/°C	
Output Leakage Current			±10	nA	Data = 0x0000, T_A = 25°C, $I_{OUT}1$
			±20	nA	Data = 0x0000, T = −40°C to 125°C, $I_{OUT}1$
REFERENCE INPUT[1]					
Reference Input Range		±10		V	
V_{REF} Input Resistance	8	10	12	kΩ	Input resistance TC = −50 ppm/°C
R_{FB} Resistance	8	10	12	kΩ	Input resistance TC = −50 ppm/°C
Input Capacitance					
Code Zero Scale		3	6	pF	
Code Full Scale		5	8	pF	
DIGITAL INPUT/OUTPUT[1]					
Input High Voltage, V_{IH}	1.7			V	
Input Low Voltage, V_{IL}			0.6	V	
Output High Voltage, V_{OH}	V_{DD} − 1			V	V_{DD} = 4.5 V to 5 V, I_{SOURCE} = 200 µA
	V_{DD} − 0.5			V	V_{DD} = 2.5 V to 3.6 V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	V_{DD} = 4.5 V to 5 V, I_{SINK} = 200 µA
			0.4	V	V_{DD} = 2.5 V to 3.6 V, I_{SINK} = 200 µA
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance		4	10	pF	
DYNAMIC PERFORMANCE[1]					
Reference Multiplying Bandwidth		10		MHz	V_{REF} = ±3.5 V; DAC loaded all 1s
Output Voltage Settling Time					V_{REF} = 10 V; R_{LOAD} = 100 Ω, DAC latch alternately loaded with 0s and 1s
Measured to ±16 mV of FS		50	100	ns	
Measured to ±4 mV of FS		55	110	ns	
Measured to ±1 mV of FS		90	160	ns	
Digital Delay		40	75	ns	Interface delay time
10% to 90% Rise/Fall Time		15	30	ns	Rise and fall time, V_{REF} = 10 V, R_{LOAD} = 100 Ω
Digital-to-Analog Glitch Impulse		2		nV-s	1 LSB change around major carry, V_{REF} = 0 V
Multiplying Feedthrough Error					DAC latch loaded with all 0s, V_{REF} = ±3.5
		70		dB	1 MHz
		48		dB	10 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Capacitance					
$I_{OUT}1$		12	17	pF	All 0s loaded
		10	12	pF	All 1s loaded
$I_{OUT}2$		22	25	pF	All 0s loaded
		10	12	pF	All 1s loaded
Digital Feedthrough		0.1		nV-s	Feedthrough to DAC output with $\overline{SYNC}$ high and alternate loading of all 0s and all 1s
Analog THD		81		dB	V_{REF} = 3.5 V p-p, all 1s loaded, f = 1 kHz
Digital THD					Clock = 1 MHz, V_{REF} = 3.5 V, C_{COMP} = 1.8 pF
50 kHz f_{OUT}		73		dB	
20 kHz f_{OUT}		74		dB	
Output Noise Spectral Density		25		nV/√Hz	@ 1 kHz
SFDR Performance (Wide Band)					Clock = 1 MHz, V_{REF} = 3.5 V
50 kHz f_{OUT}		75		dB	
20 kHz f_{OUT}		76		dB	
SFDR Performance (Narrow Band)					Clock = 1 MHz, V_{REF} = 3.5 V
50 kHz f_{OUT}		87		dB	
20 kHz f_{OUT}		87		dB	
Intermodulation Distortion		78		dB	Clock = 1 MHz, f_1 = 20 kHz, f_2 = 25 kHz, V_{REF} = 3.5 V
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			0.6	µA	T_A = 25°C, logic inputs = 0 V or V_{DD}
		0.4	5	µA	T = −40°C to +125°C , logic inputs = 0 V or V_{DD}
Power Supply Sensitivity[1]			0.001	%/%	ΔV_{DD} = ±5%

[1] Guaranteed by design and characterization, not subject to production testing.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V; temperature range for Y version: −40°C to +125°C; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	2.5 V to 5.5 V	4.5 V to 5.5 V	Unit	Test Conditions/Comments
f_{SCLK}	50	50	MHz max	Max clock frequency
t_1	20	20	ns min	SCLK cycle time
t_2	8	8	ns min	SCLK high time
t_3	8	8	ns min	SCLK low time
t_4[1]	13	13	ns min	$\overline{SYNC}$ falling edge to SCLK active edge setup time
t_5	5	5	ns min	Data setup time
t_6	3	3	ns min	Data hold time
t_7	5	5	ns min	$\overline{SYNC}$ rising edge to SCLK active edge
t_8	30	30	ns min	Minimum $\overline{SYNC}$ high time
t_9[2, 3]	80	45	ns typ	SCLK active edge to SDO valid
	120	65	ns max	

[1] Falling or rising edge as determined by control bits of serial word.
[2] Daisy-chain and readback modes cannot operate at maximum clock frequency. SDO timing specifications measured with load circuit, as shown in Figure 4.
[3] SDO operates with a VDD of 3.0 V to 5.5 V.

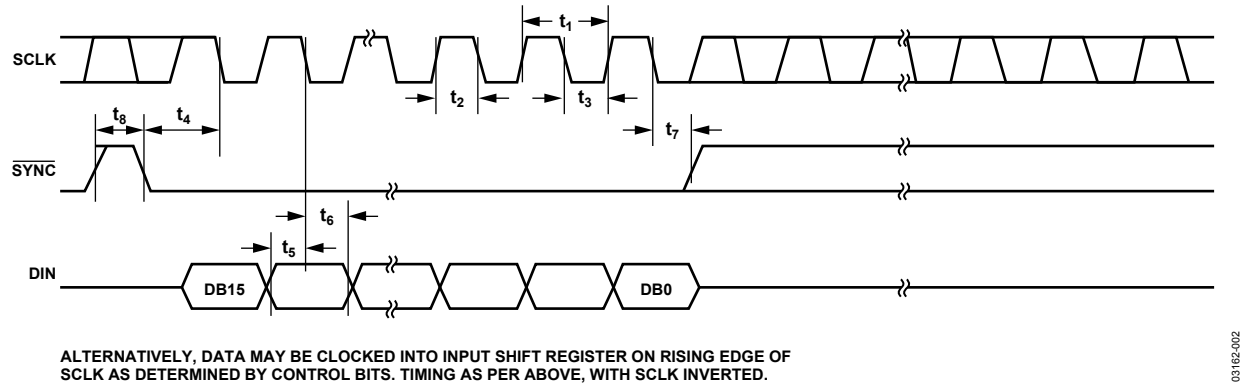


Figure 2. Standalone Mode Timing Diagram

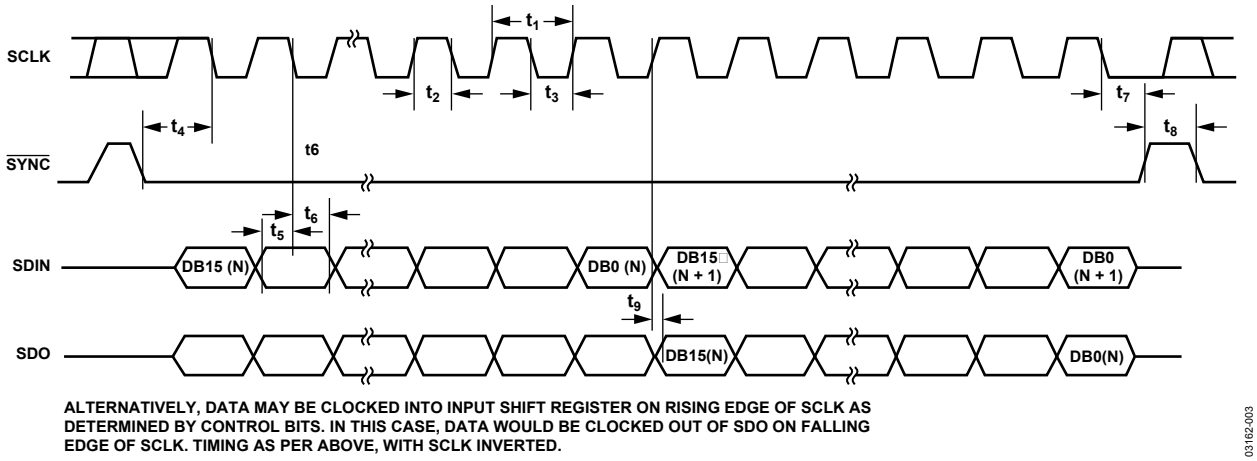


Figure 3. Daisy-Chain and Readback Modes Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Transient currents of up to 100 mA do not cause SCR latch-up.
T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{REF}, R_{FB} to GND	−12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	−0.3 V to V_{DD} + 0.3 V
Logic Inputs and Output[1]	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Extended Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
10-lead MSOP θ_{JA} Thermal Impedance	206°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

[1] Overvoltages at SCLK, $\overline{SYNC}$, and DIN are clamped by internal diodes.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

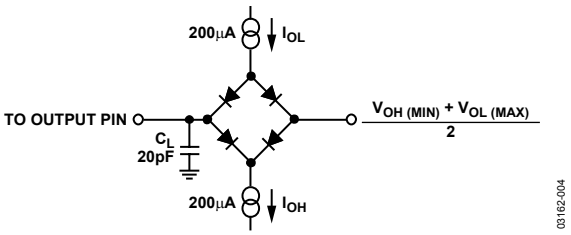


Figure 4. Load Circuit for SDO Timing Specifications

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

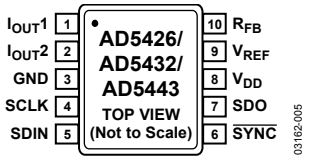


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$I_{OUT}1$	DAC Current Output.
2	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	GND	Digital Ground Pin.
4	SCLK	Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device may be configured such that data is clocked into the shift register on the rising edge of SCLK. The device can accommodate clock rates up to 50 MHz.
5	SDIN	Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, on power-up, data is clocked into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to rising edge.
6	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers, and the input shift register is enabled. Data is loaded to the mode, the serial interface counts clocks, and data is latched to the shift register on the 16th active clock edge.
7	SDO	Serial Data Output. This allows a number of parts to be daisy-chained. By default, data is clocked into the shift register on the falling edge and out via SDO on the rising edge of SCLK. Data is always clocked out on the alternate edge to loading data to the shift register. Writing the readback control word to the shift register makes the DAC register contents available for readback on the SDO pin, clocked out on the opposite edges to the active clock edge. SDO operates with a V_{DD} of 3.0 V to 5.5 V.
8	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
9	V_{REF}	DAC Reference Voltage Input.
10	R_{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.

TYPICAL PERFORMANCE CHARACTERISTICS

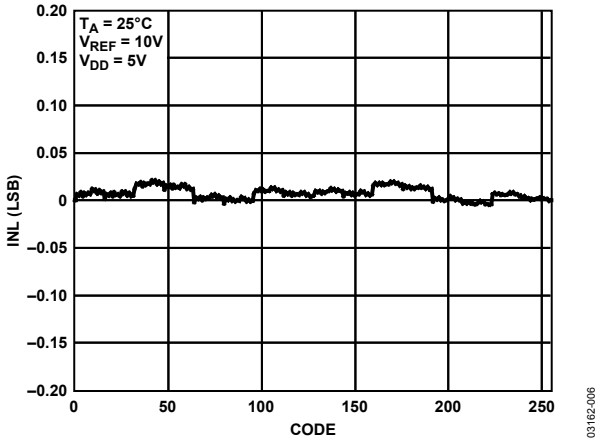


Figure 6. INL vs. Code (8-Bit DAC)

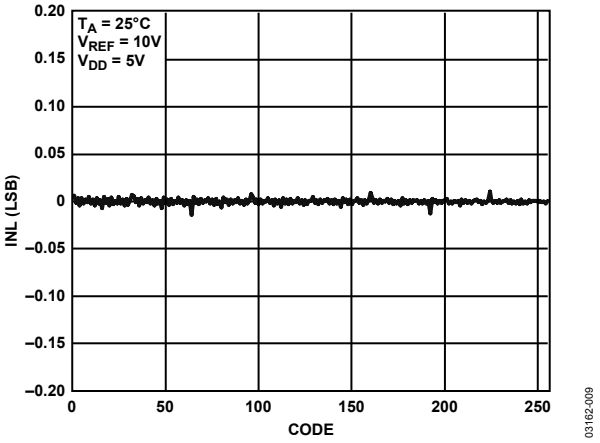


Figure 9. DNL vs. Code (8-Bit DAC)

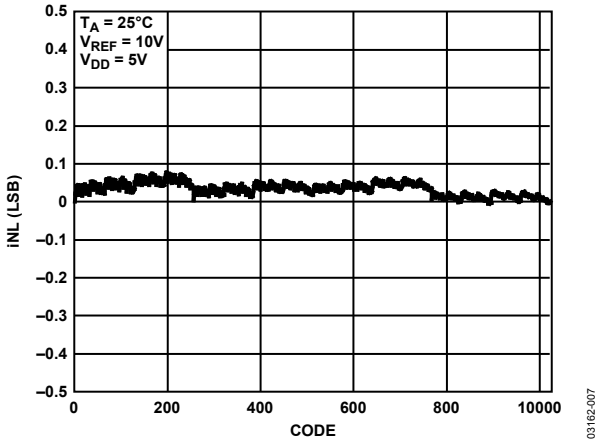


Figure 7. INL vs. Code (10-Bit DAC)

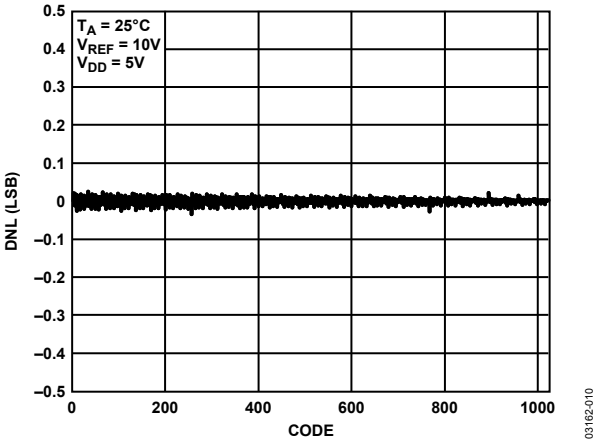


Figure 10. DNL vs. Code (10-Bit DAC)

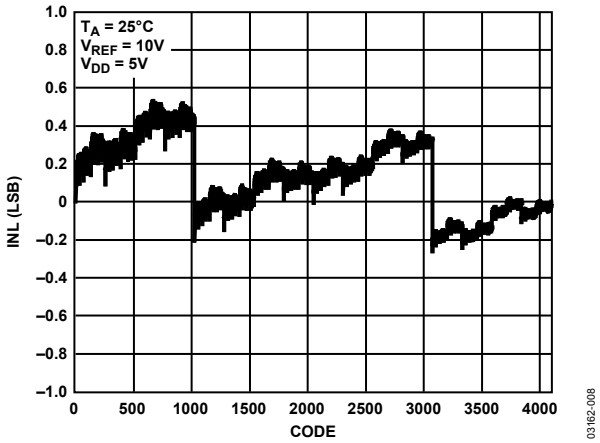


Figure 8. INL vs. Code (12-Bit DAC)

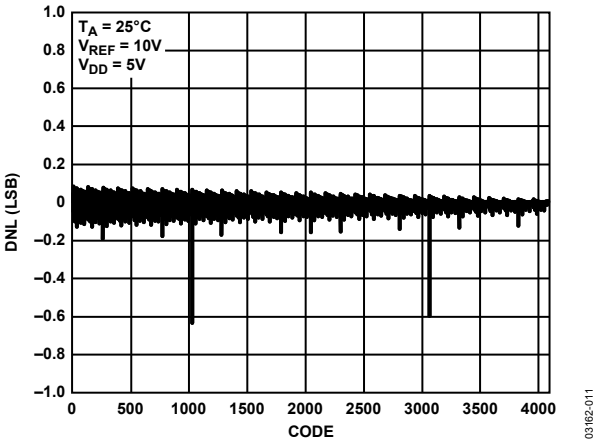


Figure 11. DNL vs. Code (12-Bit DAC)

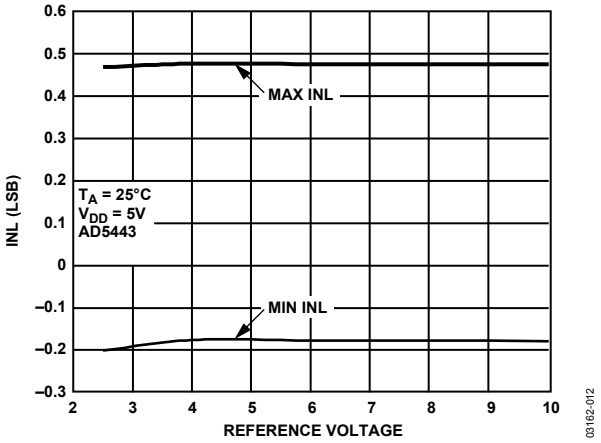


Figure 12. INL vs. Reference Voltage

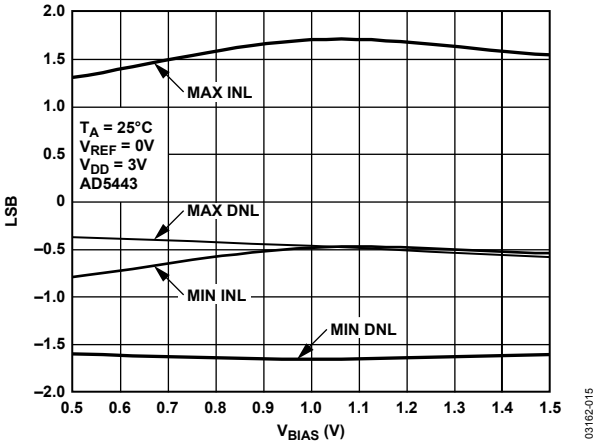


Figure 15. Linearity vs. VBIAS Voltage Applied to IOUT2

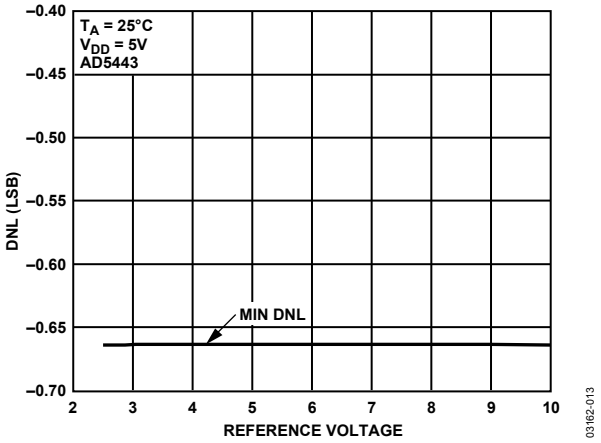


Figure 13. DNL vs. Reference Voltage

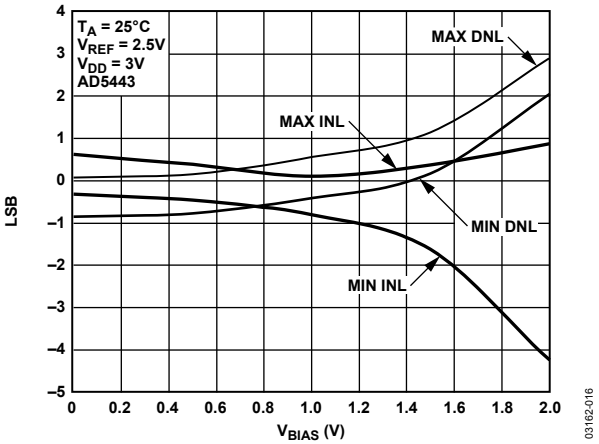


Figure 16. Linearity vs. VBIAS Voltage Applied to IOUT2

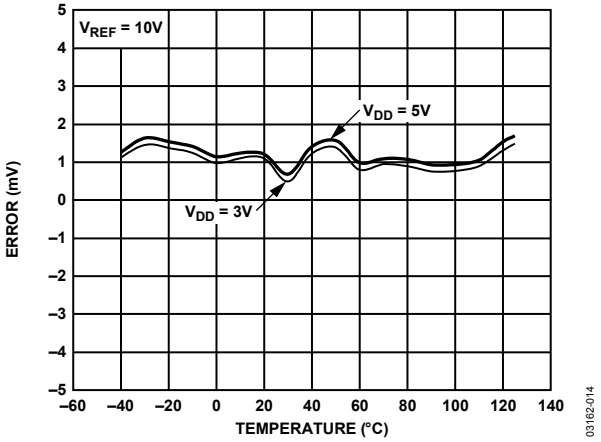


Figure 14. Gain Error vs. Temperature

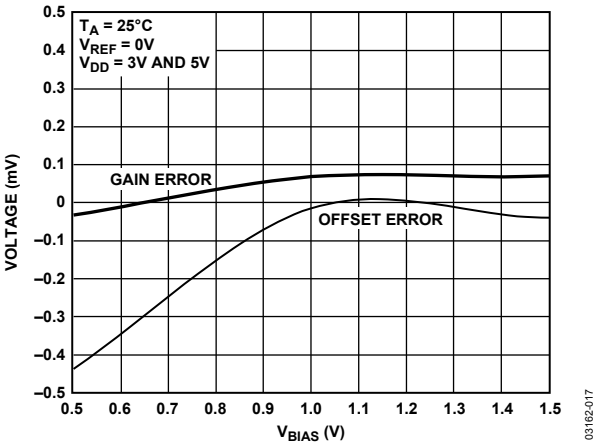


Figure 17. Gain and Offset Errors vs. VBIAS Voltage Applied to IOUT2

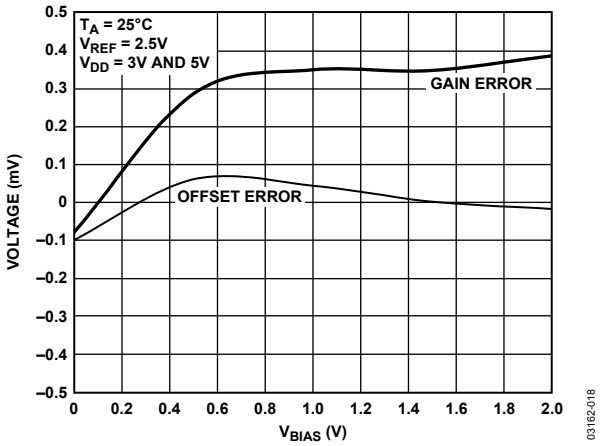


Figure 18. Gain and Offset Errors vs. VBIAS Voltage Applied to IOUT2

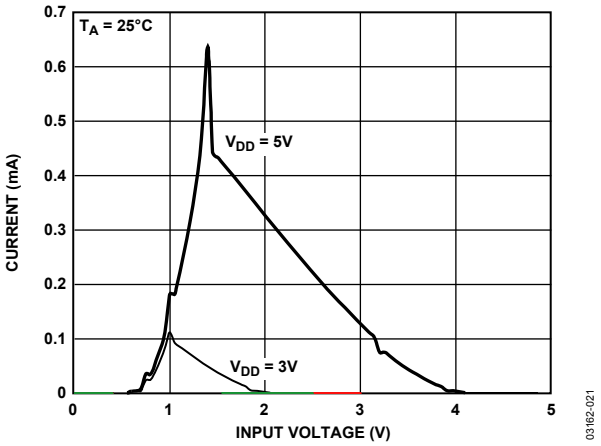


Figure 21. Supply Current vs. Logic Input Voltage, $\overline{SYNC}$ (SCLK), DATA = 0

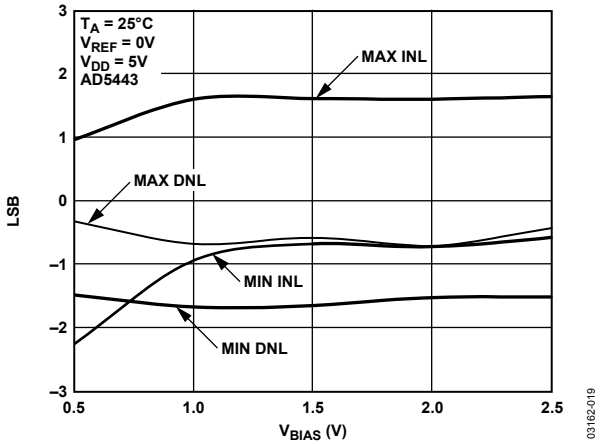


Figure 19. Linearity vs. VBIAS Voltage Applied to IOUT2

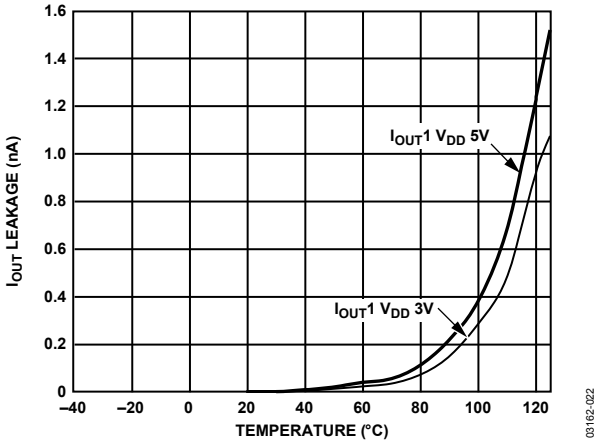


Figure 22. IOUT1 Leakage Current vs. Temperature

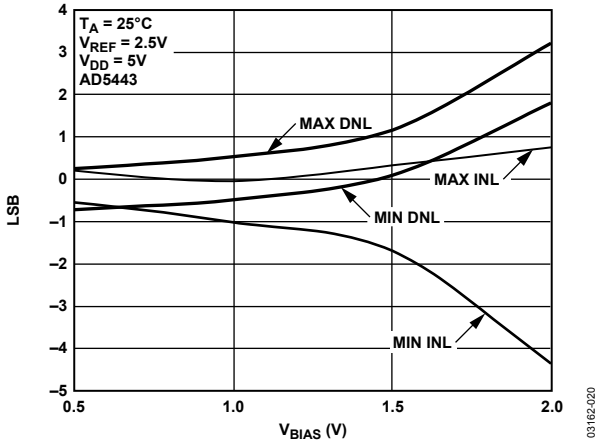


Figure 20. Linearity vs. VBIAS Voltage Applied to IOUT2

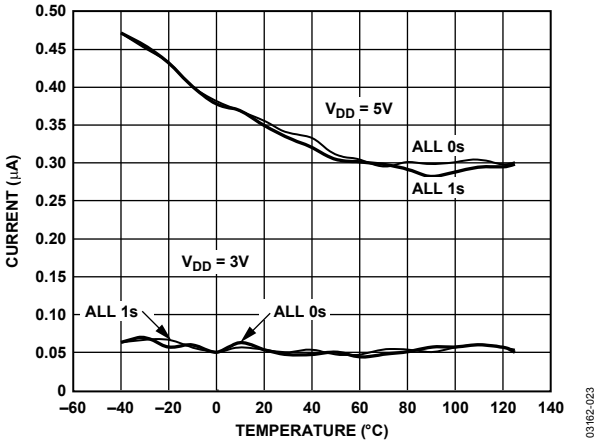


Figure 23. Supply Current vs. Temperature

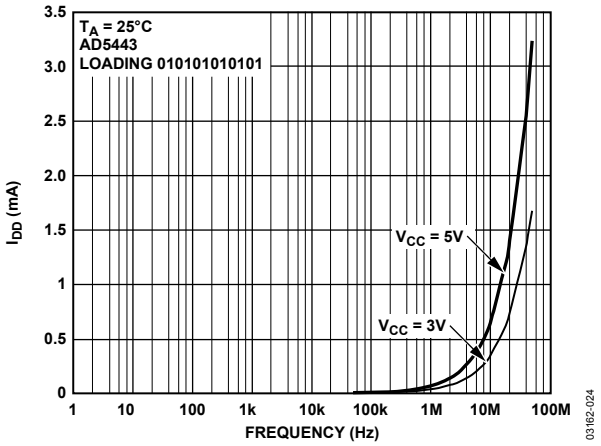


Figure 24. Supply Current vs. Update Rate

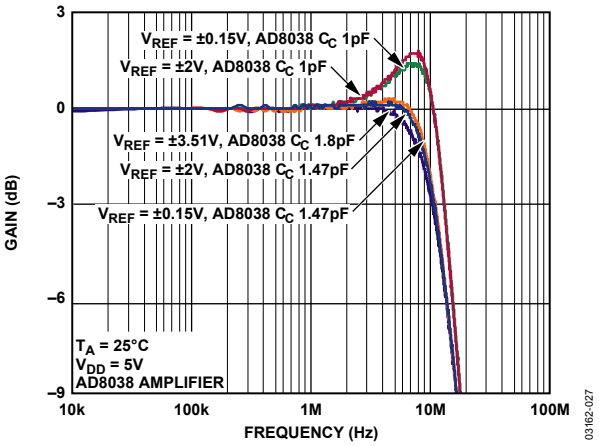


Figure 27. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

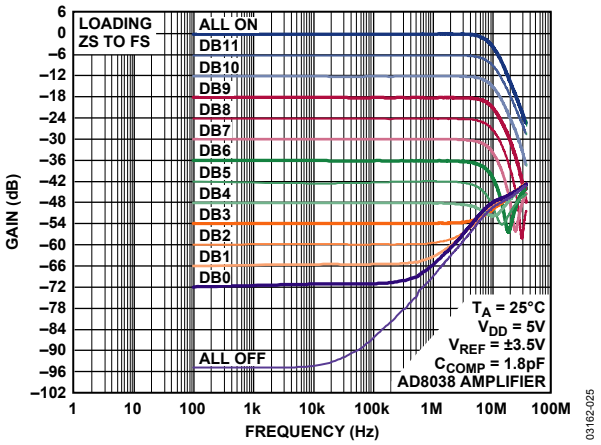


Figure 25. Reference Multiplying Bandwidth vs. Frequency and Code

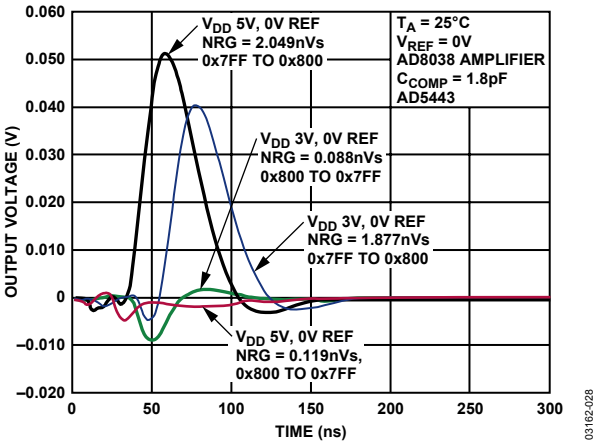


Figure 28. Midscale Transition VREF = 0 V

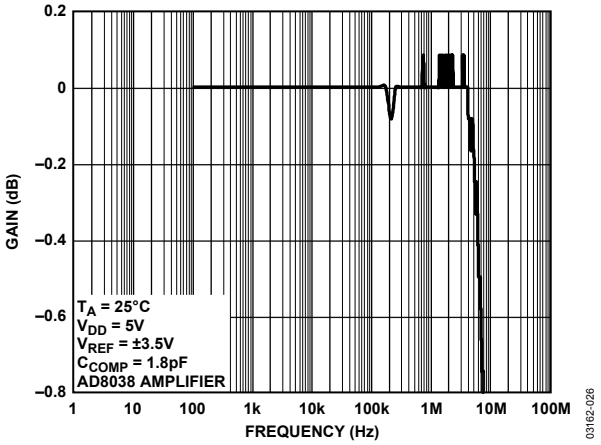


Figure 26. Reference Multiplying Bandwidth—All 1s Loaded

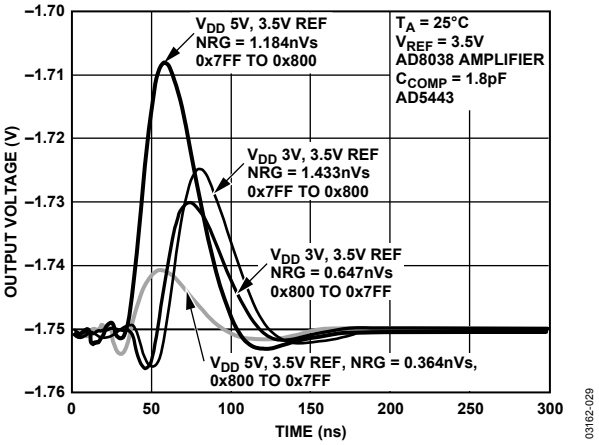


Figure 29. Midscale Transition VREF = 3.5 V

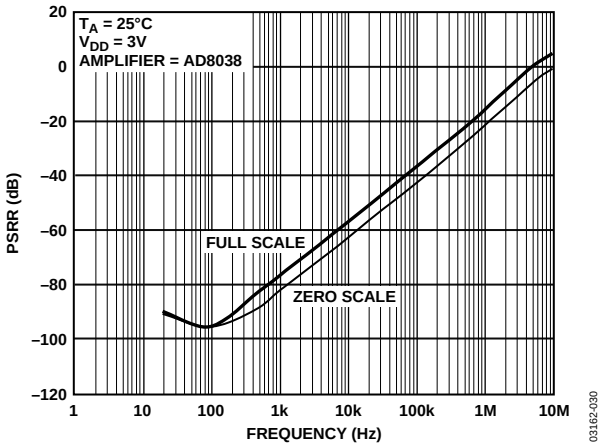


Figure 30. Power Supply Rejection vs. Frequency

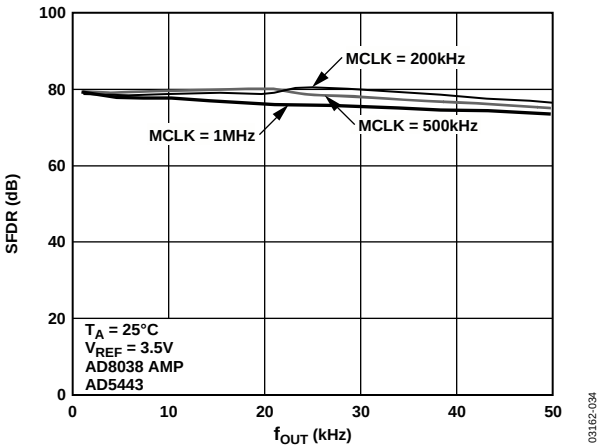


Figure 33. Wideband SFDR vs. f_{OUT} Frequency (AD5443)

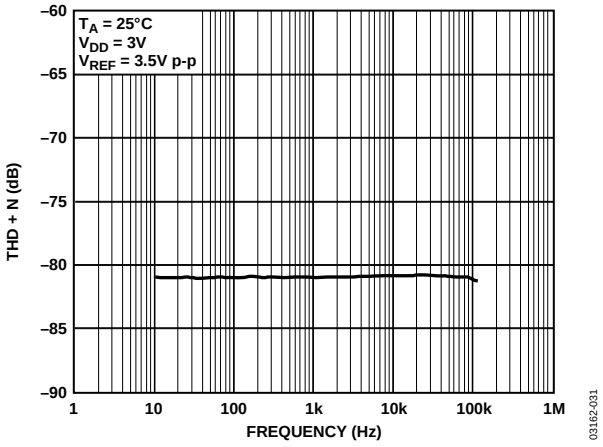


Figure 31. THD and Noise vs. Frequency

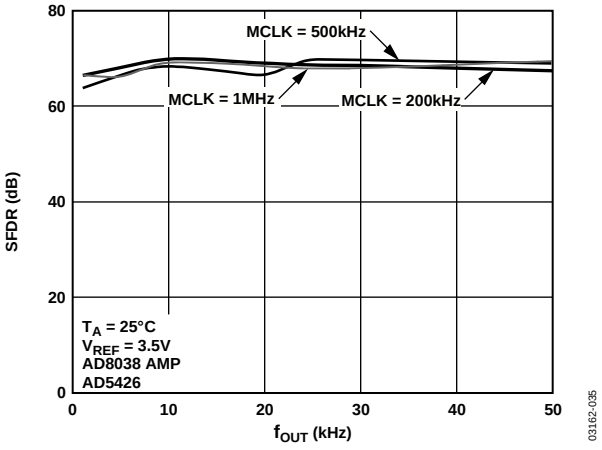


Figure 34. Wideband SFDR vs. f_{OUT} Frequency (AD5426)

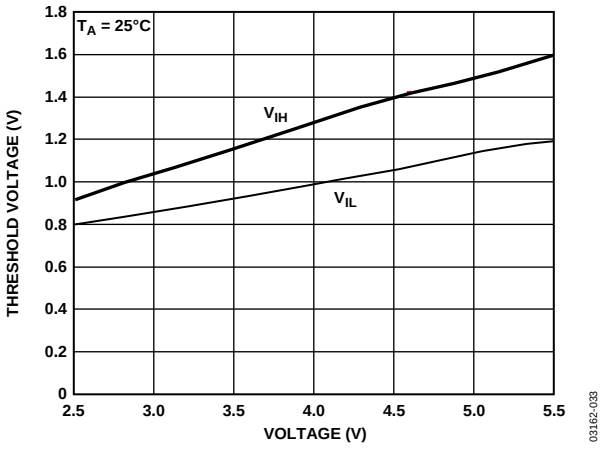


Figure 32. Threshold Voltages vs. Supply Voltage

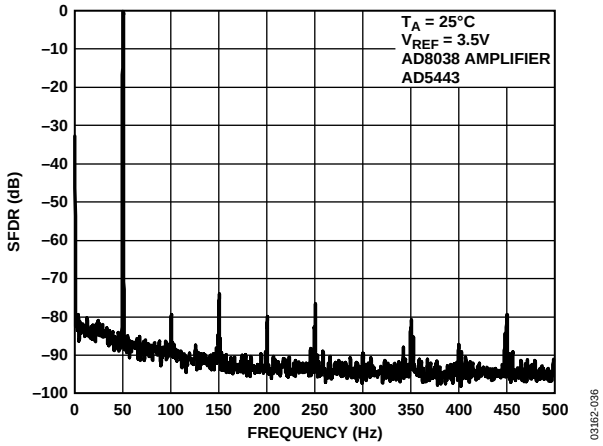


Figure 35. Wideband SFDR f_{OUT} = 50 kHz, Update = 1 MHz

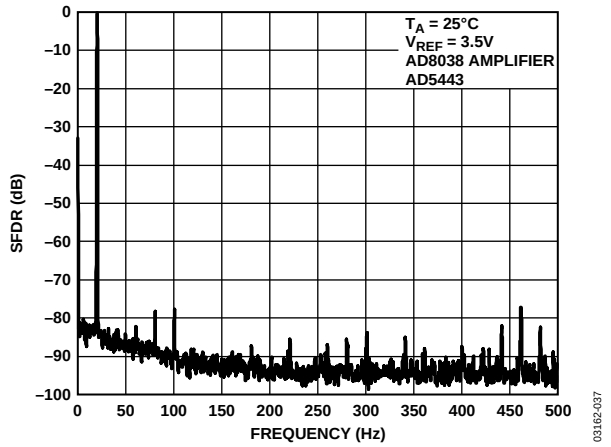


Figure 36. Wideband SFDR f_{OUT} = 20 kHz, Update = 1 MHz

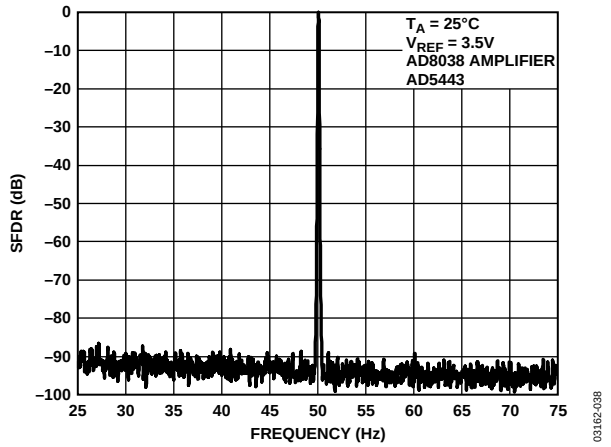


Figure 37. Narrowband (±50%) SFDR f_{OUT} = 50 kHz, Update = 1 MHz

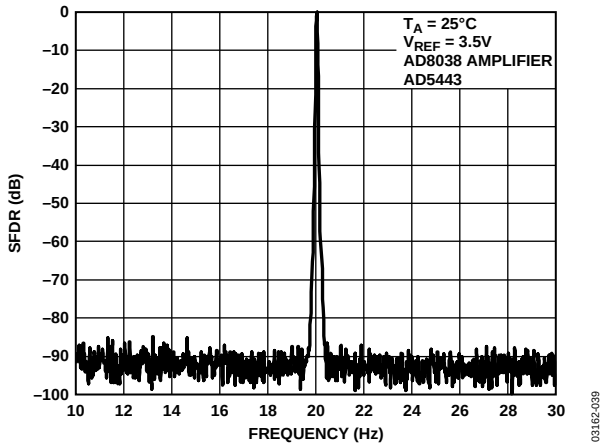


Figure 38. Narrowband (±50%) SFDR f_{OUT} = 20 kHz, Update = 1 MHz

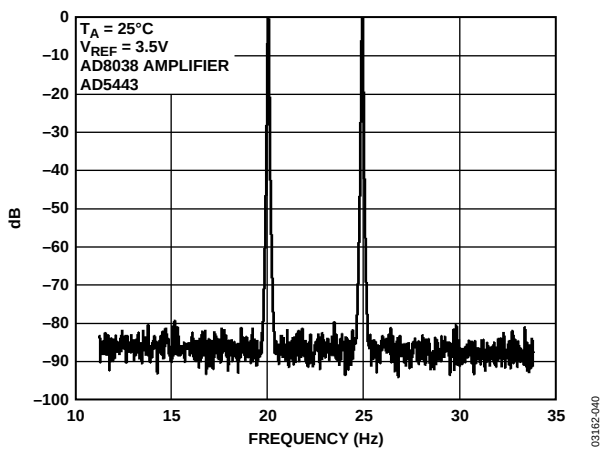


Figure 39. Narrowband (±50%) IMD f_{OUT} = 20 kHz, 25 kHz, Update = 1 MHz

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for 0 and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of −1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} − 1 LSB. Gain error of the DACs is adjustable to 0 with external resistance.

Output Leakage Current
Output leakage current is current that flows in the DAC ladder switches when these are turned off. For the $I_{OUT}1$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current flows in the $I_{OUT}2$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$ or $I_{OUT}2$ to AGND.

Output Current Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For these devices, it is specified with a 100 Ω resistor to ground.

The settling time specification includes the digital delay from $\overline{SYNC}$ rising edge to the full-scale output charge.

Digital-to-Analog Glitch Impulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-s or nV-s depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs may be capacitively coupled to show up as noise on the I_{OUT} pins and subsequently into the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal, when all 0s are loaded to the DAC.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second to fifth.

$$THD = 20 \log \frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1}$$

Digital Intermodulation Distortion
Second-order intermodulation distortion (IMD) measurements are the relative magnitude of the fa and fb tones generated digitally by the DAC and the second-order products at 2fa − fb and 2fb − fa.

Spurious-Free Dynamic Range (SFDR)
SFDR is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. It is the measure of the difference in amplitude between the fundamental and the largest harmonically or nonharmonically related spur from dc to full Nyquist bandwidth (half the DAC sampling rate, or $f_S/2$). Narrow band SFDR is a measure of SFDR over an arbitrary window size, in this case 50% of the fundamental. Digital SFDR is a measure of the usable dynamic range of the DAC when the signal is a digitally generated sine wave.

THEORY OF OPERATION

The AD5426, AD5432, and AD5443 are 8-, 10-, and 12-bit current output DACs consisting of a standard inverting R-2R ladder configuration. A simplified diagram for the 8-bit AD5426 is shown in Figure 40. The matching feedback resistor, R_{FB}, has a value of R. The value of R is typically 10 kΩ (minimum 8 kΩ and maximum 12 kΩ). If $I_{OUT}1$ and $I_{OUT}2$ are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant and nominally of value R. The DAC output (I_{OUT}) is code-dependent, producing various resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the DAC on the amplifiers inverting input node.

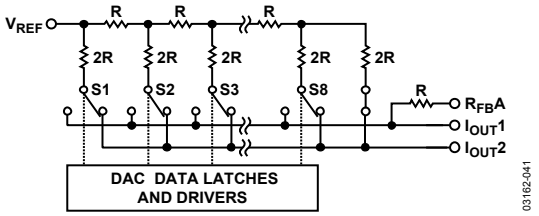


Figure 40. Simplified Ladder

Access is provided to the V_{REF}, R_{FB}, $I_{OUT}1$, and $I_{OUT}2$ terminals of the DAC, making the device extremely versatile and allowing it to be configured in several different operating modes. For example, it can be configured to provide a unipolar output, 4-quadrant multiplication in bipolar or single-supply modes of operation. Note that a matching switch is used in series with the internal R_{FB} feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} to achieve continuity.

CIRCUIT OPERATION

Unipolar Mode

Using a single op amp, these devices can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 41.

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times \frac{D}{2^n}$$

where D is the fractional representation of the digital word loaded to the DAC, and n is the number of bits.

D = 0 to 255 (8-bit AD5426)
= 0 to 1023 (10-bit AD5432)
= 0 to 4095 (12-bit AD5443)

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages.

These DACs are designed to operate with either negative or positive reference voltages. The V_{DD} power pin is used by only the internal digital logic to drive the DAC switches' on and off states.

These DACs are also designed to accommodate ac reference input signals in the range of −10 V to +10 V.

With a fixed 10 V reference, the circuit shown in Figure 41 gives a unipolar 0 V to −10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. Table 5 shows the relationship between digital code and expected output voltage for unipolar operation (AD5426, 8-bit device).

Table 5. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

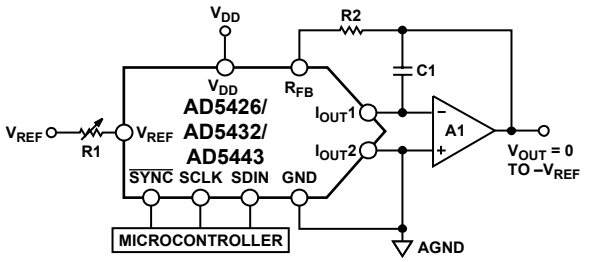


Figure 41. Unipolar Operation

Bipolar Operation

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can easily be accomplished by using another external amplifier and some external resistors, as shown in Figure 42. In this circuit, the second amplifier, A2, provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage results in full 4-quadrant multiplying operation. The transfer function of this circuit shows that both negative and positive output voltages are created as the input data, D, which is incremented from code zero ($V_{OUT} = -V_{REF}$) to midscale ($V_{OUT} = 0$ V) to full scale ($V_{OUT} = +V_{REF}$).

$$V_{OUT} = \left(V_{REF} \times \frac{D}{2^{n-1}} \right) - V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC and n is the resolution of the DAC.

D = 0 to 255 (8-bit AD5426)
= 0 to 1023 (10-bit AD5432)
= 0 to 4095 (12-bit AD5443)

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication.

Table 6 shows the relationship between digital code and the expected output voltage for bipolar operation (AD5426, 8-bit device).

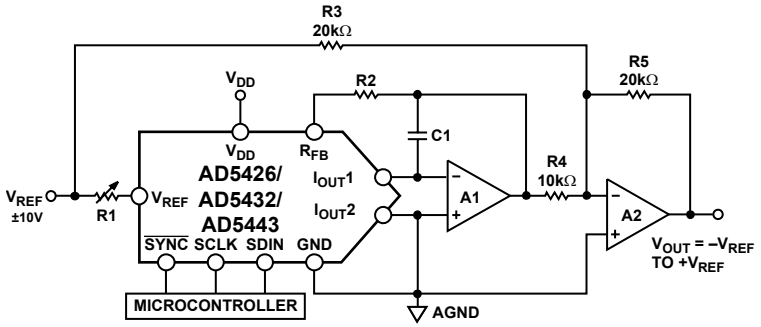
Table 6. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (127/128)
1000 0000	0
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible and proper PCB layout techniques must be employed. Since every code change corresponds to a step function, gain peaking may occur if the op amp has limited gain bandwidth product (GBP) and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response that can cause ringing or instability in closed-loop applications.

An optional compensation capacitor, C1, can be added in parallel with R_{FB} for stability, as shown in Figure 41 and Figure 42. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to 2 pF is generally adequate for compensation.



NOTES
1. R1 AND R2 ARE USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. ADJUST R1 FOR V_{OUT} = 0V WITH CODE 10000000 LOADED TO DAC.
2. MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R3 AND R4.
3. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED IF A1/A2 IS A HIGH SPEED AMPLIFIER.

03162-043

Figure 42. Bipolar Operation

SINGLE-SUPPLY APPLICATIONS

Current Mode Operation

These DACs are specified and tested to guarantee operation in single-supply applications. In the current mode circuit of Figure 43, $I_{OUT}2$ and hence $I_{OUT}1$ is biased positive by an amount applied to V_{BIAS}.

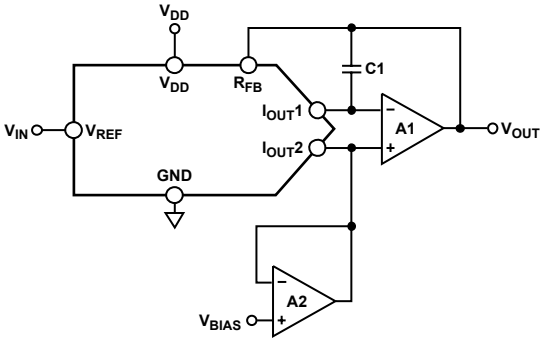


Figure 43. Single-Supply Current Mode Operation

In this configuration, the output voltage is given by

$$V_{OUT} = \{D \times (R_{FB}/R_{DAC}) \times (V_{BIAS} - V_{IN})\} + V_{BIAS}$$

As *D* varies from 0 to 255 (AD5426), 1023 (AD5432) or 4095 (AD5443), the output voltage varies from

$$V_{OUT} = V_{BIAS} \text{ to } V_{OUT} = 2\ V_{BIAS} - V_{IN}$$

V_{BIAS} should be a low impedance source capable of sinking and sourcing all possible variations in current at the $I_{OUT}2$ terminal without any problems.

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source drain drive voltage. As a result, their on resistance differs, which degrades the linearity of the DAC. See Figure 15 to Figure 20.

Voltage Switching Mode of Operation

Figure 44 shows these DACs operating in the voltage switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1$ pin, $I_{OUT}2$ is connected to AGND, and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance), thus an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. Therefore, the voltage input should be driven from a low impedance source.

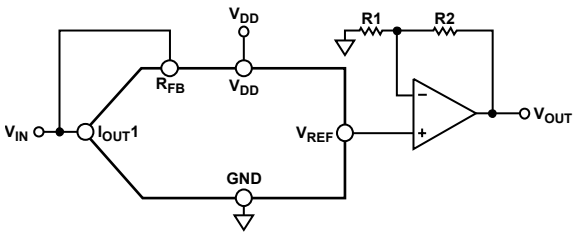


Figure 44. Single-Supply Voltage Switching Mode Operation

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source drain drive voltage. As a result, their on resistance differs, which degrades the linearity of the DAC.

Also, V_{IN} must not go negative by more than 0.3 V or an internal diode turns on, exceeding the maximum ratings of the device. In this type of application, the full range of multiplying capability of the DAC is lost.

ADDING GAIN

In applications where the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier or it can be achieved in a single stage. It is important to consider the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the R_{FB} resistor causes mismatches in the temperature coefficients, resulting in larger gain temperature coefficient errors. Instead, the circuit shown in Figure 45 is a recommended method of increasing the gain of the circuit. R1, R2, and R3 should all have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of greater than 1 are required.

Note that R_{FB} is much greater than R2||R3 and that a gain error percentage of $100 \times (R2||R3)/R_{FB}$ must be taken into consideration.

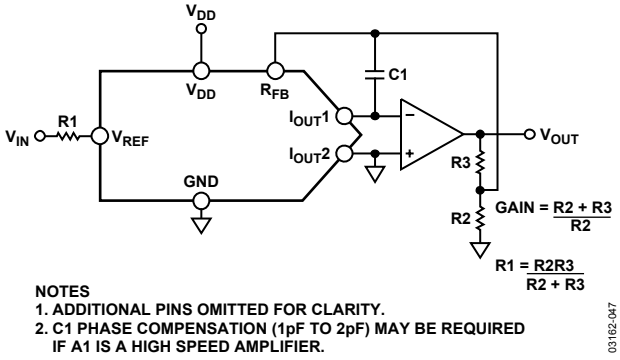


Figure 45. Increasing Gain of Current Output DAC

DACS USED AS A DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current-steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an op amp and R_{FB} is used as the input resistor as shown in Figure 46, then the output voltage is inversely proportional to the digital input fraction, D.

For $D = 1 - 2^{-n}$ the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/(1 - 2^{-N})$$

As D is reduced, the output voltage increases. For small values of D, it is important to ensure that the amplifier does not saturate and also that the required accuracy is met. For example, an 8-bit DAC driven with the binary code 0x10 (00010000), that is, 16 decimal, in the circuit of Figure 46 should cause the output voltage to be 16 × V_{IN}. However, if the DAC has a linearity specification of ±0.5 LSB, then D can in fact have the weight anywhere in the range 15.5/256 to 16.5/256 so that the possible output voltage will be in the range 15.5 V_{IN} to 16.5 V_{IN}—an error of +3% even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Since only a fraction D of the current into the VREF terminal is routed to the IOUT1 terminal, the output voltage has to change as follows:

$$Output\ Error\ Voltage\ due\ to\ DAC\ Leakage = (Leakage \times R)/D$$

where *R* is the DAC resistance at the V_{REF} terminal. For a DAC leakage current of 10 nA, R = 10 kΩ, and a gain (that is, 1/D) of 16, the error voltage is 1.6 mV.

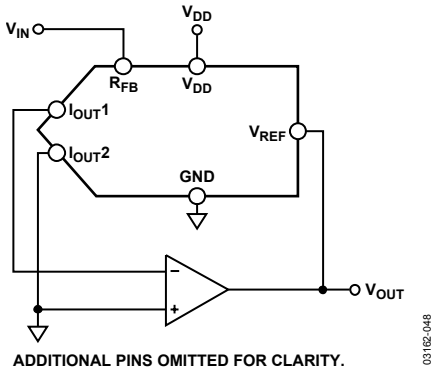


Figure 46. Current Steering DAC as a Divider or Programmable Gain Element

REFERENCE SELECTION

When selecting a reference for use with the AD5426 series of current output DACs, pay attention to the references output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but can also affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum system drift with temperature should be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. By choosing a precision reference with low output temperature coefficient this error source can be minimized.

Table 7 suggests some references available from Analog Devices that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic. In general, the input offset voltage should be a fraction (approximately <1/4) of an LSB to ensure monotonic behavior when stepping through codes.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor, R_{FB}. Most op amps have input bias currents low enough to prevent any significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage switching circuits since it produces a code-dependent error at the voltage output of the circuit. Most op amps have adequate common-mode rejection at an 8-, 10-, or 12-bit resolution.

Provided the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage switching DAC circuit is determined largely by the output op amp.

To obtain minimum settling time in this configuration, it is important to minimize capacitance at the V_{REF} of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design. Most single-supply circuits include ground as part of the analog signal range, which in turn requires an amplifier that can handle rail-to-rail signals. There is a large range of single-supply amplifiers available from Analog Devices.

Table 7. Suitable ADI Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Temp Drift (ppm/°C)	I_{SS} (mA)	Output Noise µV p-p	Package
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-23, SC70
ADR02	5	0.06	3	1	10	SOIC-8
ADR02	5	0.06	9	1	10	TSOT-23, SC70
ADR03	2.5	0.10	3	1	6	SOIC-8
ADR03	2.5	0.10	9	1	6	TSOT-23, SC70
ADR06	3	0.10	3	1	10	SOIC-8
ADR06	3	0.10	9	1	10	TSOT-23, SC70
ADR431	2.5	0.04	3	0.8	3.5	SOIC-8
ADR435	5	0.04	3	0.8	8	SOIC-8
ADR391	2.5	0.16	9	0.12	5	TSOT-23
ADR395	5	0.10	9	0.12	8	TSOT-23

Table 8. Suitable ADI Precision Op Amps

Part No.	Supply Voltage (V)	V_{OS} (Max) (µV)	I_B (Max) (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package
OP97	±2 to ±20	25	0.1	0.5	600	SOIC-8
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP, SOIC-8
AD8551	2.7 to 5	5	0.05	1	975	MSOP, SOIC-8
AD8603	1.8 to 6	50	0.001	2.3	50	TSOT
AD8628	2.7 to 6	5	0.1	0.5	850	TSOT, SOIC-8

Table 9. Suitable ADI High Speed Op Amps

Part No.	Supply Voltage (V)	BW @ A_{CL} (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Package
AD8065	5 to 24	145	180	1,500	6,000	SOIC-8, SOT-23, MSOP
AD8021	±2.5 to ±12	490	100	1,000	10,500	SOIC-8, MSOP
AD8038	3 to 12	350	425	3,000	750	SOIC-8, SC70-5
AD9631	±2 to ±6	320	1,300	10,000	7,000	SOIC-8

SERIAL INTERFACE

The AD5426/AD5432/AD5443 have an easy to use 3-wire interface that is compatible with SPI/QSPI/MICROWIRE and DSP interface standards. Data is written to the device in 16 bit words. This 16-bit word consists of 4 control bits and either 8 , 10 , or 12 data bits as shown in Figure 47, Figure 48, and Figure 49. The AD5443 uses all 12 bits of DAC data. The AD5432 uses 10 bits and ignores the 2 LSBs, while the AD5426 uses 8 bits and ignores the last 4 bits.

Low Power Serial Interface

To minimize the power consumption of the device, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{SYNC}}$. The SCLK and DIN input buffers are powered down on the rising edge of $\overline{\text{SYNC}}$. The $\overline{\text{SYNC}}$ of the AD5426/AD5432/AD5443 needs to be synchronous with the microprocessor control. Unfinished data frames are latched into the part and will affect the output.

DAC Control Bits C3 to C0

Control Bits C3 to C0 allow control of various functions of the DAC, as seen in Table 10. Default settings of the DAC on power-on are as follows: Data is clocked into the shift register on falling clock edges and daisy-chain mode is enabled. Device powers on with zero-scale load to the DAC register and I_{OUT} lines.

The DAC control bits allow the user to adjust certain features on power-on, for example, daisy-chaining may be disabled if not in use, active clock edge may be changed to rising edge, and DAC output may be cleared to either zero scale or midscale. The user may also initiate a readback of the DAC register contents for verification purposes.

Table 10. DAC Control Bits

C3	C2	C1	C0	Function Implemented
0	0	0	0	No operation (power-on default)
0	0	0	1	Load and update
0	0	1	0	Initiate readback
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Daisy-chain disable
1	0	1	0	Clock data to shift register on rising edge
1	0	1	1	Clear DAC output to zero scale
1	1	0	0	Clear DAC output to midscale
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

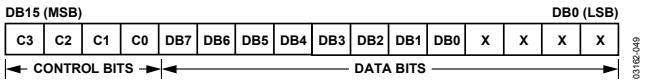


Figure 47. AD5426 8-Bit Input Shift Register Contents

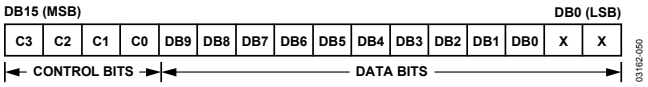


Figure 48. AD5432 10-Bit Input Shift Register Contents

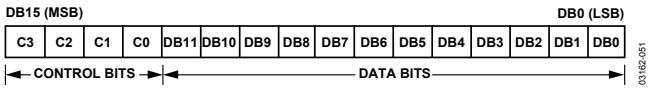


Figure 49. AD5443 12-Bit Input Shift Register Contents

$\overline{\text{SYNC}}$ Function

$\overline{\text{SYNC}}$ is an edge-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while $\overline{\text{SYNC}}$ is low. To start the serial data transfer, $\overline{\text{SYNC}}$ should be taken low observing the minimum $\overline{\text{SYNC}}$ falling to SCLK falling edge setup time, t_4.

Daisy-Chain Mode

Daisy-chain is the default power-on mode. Note that the SDO line operates with a V_{DD} of 3.0 V to 5.5 V. To disable the daisy chain function, write 1001 to the control word. In daisy-chain mode, the internal gating on SCLK is disabled. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK (this is the default, use the control word to change the active edge) and is valid for the next device on the falling edge (default). By connecting this line to the D_{IN} input on the next device in the chain, a multidevice interface is constructed. Sixteen clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal 16 N where N is the total number of devices in the chain. See the timing diagram in Figure 4.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ should be taken high. This prevents any further data being clocked into the input shift register. A burst clock containing the exact number of clock cycles may be used and $\overline{\text{SYNC}}$ taken high some time later. After the rising edge of $\overline{\text{SYNC}}$, data is automatically transferred from each device's input shift register to the addressed DAC.

When control bits = 0000, the device is in no operation mode. This may be useful in daisy-chain applications where the user does not want to change the settings of a particular DAC in the chain. Simply write 0000 to the control bits for that DAC and the following data bits will be ignored. To re-enable the daisy-chain mode, if disabled, a power recycle is required.

Standalone Mode

After power-on, write 1001 to the control word to disable daisy-chain mode. The first falling edge of $\overline{\text{SYNC}}$ resets a counter that counts the number of serial clocks, ensuring the correct number of bits are shifted in and out of the serial shift registers. A rising edge on $\overline{\text{SYNC}}$ during a write causes the write cycle to be aborted.

After the falling edge of the 16th SCLK pulse, data is automatically transferred from the input shift register to the DAC. For another serial transfer to take place, the counter must be reset by the falling edge of $\overline{\text{SYNC}}$.

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5426/AD5432/AD5443 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close to the device as possible.

The DAC should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching. Low ESR, 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A micro-strip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize on high frequency performance, the I-to-V amplifier should be located as close to the device as possible.

OVERVIEW OF THE AD5426/AD5432/AD5443 AND RELATED DACs

Table 11.

Part No.	Resolution	No. DACs	INL (LSB)	Interface	Package	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz serial
AD5450	8	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz serial
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5451	10	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz serial
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5444	12	1	±0.5	Serial	RM-8	50 MHz serial interface
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 50 MHz serial
AD5405	12	2	±1	Parallel	CP-40	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5452	12	1	±0.5	Serial	RJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5446	14	1	±1	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz serial clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width

OUTLINE DIMENSIONS

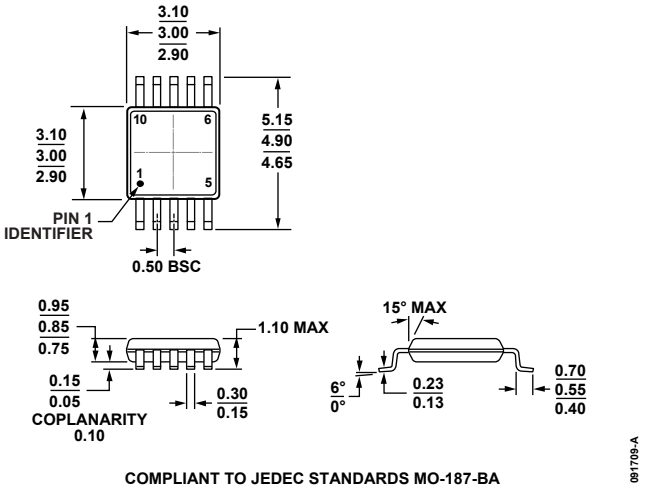


Figure 50. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bit)	INL (LSB)	Temperature Range	Package Description	Package Option	Branding
AD5426YRM	8	±0.25	−40°C to +125°C	10-Lead MSOP	RM-10	D1Q
AD5426YRM-REEL7	8	±0.25	−40°C to +125°C	10-Lead MSOP	RM-10	D1Q
AD5426YRMZ	8	±0.25	−40°C to +125°C	10-Lead MSOP	RM-10	D6W
AD5426YRMZ-REEL	8	±0.25	−40°C to +125°C	10-Lead MSOP	RM-10	D6W
AD5426YRMZ-REEL7	8	±0.25	−40°C to +125°C	10-Lead MSOP	RM-10	D6W
AD5432YRMZ	10	±0.5	−40°C to +125°C	10-Lead MSOP	RM-10	D1R#
AD5432YRMZ-REEL	10	±0.5	−40°C to +125°C	10-Lead MSOP	RM-10	D1R#
AD5432YRMZ-REEL7	10	±0.5	−40°C to +125°C	10-Lead MSOP	RM-10	D1R#
AD5443YRM	12	±1	−40°C to +125°C	10-Lead MSOP	RM-10	D1S
AD5443YRM-REEL	12	±1	−40°C to +125°C	10-Lead MSOP	RM-10	D1S
AD5443YRM-REEL7	12	±1	−40°C to +125°C	10-Lead MSOP	RM-10	D1S
AD5443YRMZ	12	±1	−40°C to +125°C	10-Lead MSOP	RM-10	D1S#
AD5443YRMZ-REEL	12	±1	−40°C to +125°C	10-Lead MSOP	RM-10	D1S#
AD5443YRMZ-REEL7	12	±1	−40°C to +125°C	10-Lead MSOP	RM-10	D1S#
EV-AD5443/46/53SDZ				Evaluation Board		

[1] Z = RoHS Compliant Part, # denotes RoHS compliant product may be top or bottom marked.