REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	35	36	37	38	39															
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

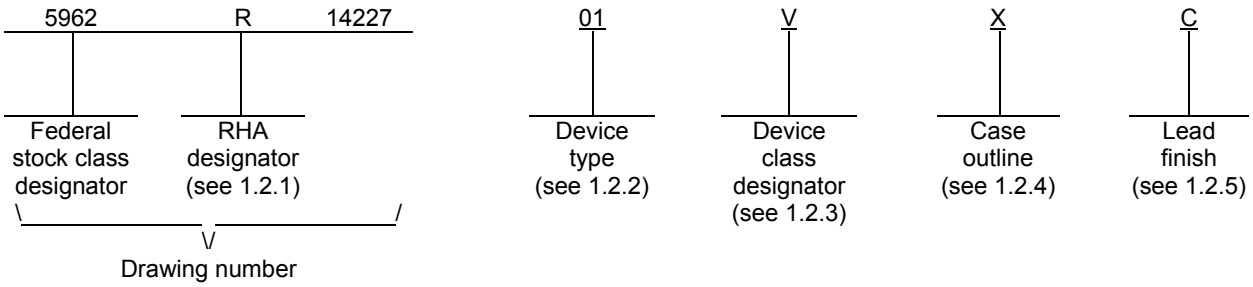
REV STATUS	REV														
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY RAJESH PITHADIA	
	APPROVED BY CHARLES F. SAFFLE	MICROCIRCUIT, DIGITAL-LINEAR, 14 BIT, 125 MSPS ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 17-10-11	
	REVISION LEVEL	SIZE: A; CAGE CODE: **67268**; **5962-14227**
		SHEET 1 OF 39

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD9246	Radiation hardened, 14-bit, 125 million samples per second (MSPS), 1.8 V analog-to-digital converter (ADC)

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Quad flat pack with brazed lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Analog power supply (AV_{DD}) to analog ground (AGND)	-0.3 V to +2.0 V
Digital output driver supply (DRV_{DD}) to digital ground (DGND)	-0.3 V to +3.9 V
AGND to DGND	-0.3 V to +0.3 V
AV_{DD} to DRV_{DD}	-3.9 V to +2.0 V
Digital outputs (D_0 through D_{13}) to DGND	-0.3 V to DRV_{DD} + 0.3 V
Digital clock output (DCO) to DGND	-0.3 V to DRV_{DD} + 0.3 V
Out of range indicator (OR) to DGND	-0.3 V to DRV_{DD} + 0.3 V
Positive clock input (+CLK) to AGND	-0.3 V to +3.9 V
Negative clock input (-CLK) to AGND	-0.3 V to +3.9 V
Positive analog input (+V_{IN}) to AGND	-0.3 V to AV_{DD} + 0.2 V
Negative analog input (-V_{IN}) to AGND	-0.3 V to AV_{DD} + 0.2 V
Voltage reference (V_{REF}) to AGND	-0.3 V to AV_{DD} + 0.2 V
Reference mode selection (SENSE) to AGND	-0.3 V to AV_{DD} + 0.2 V
Positive differential reference (REFT) to AGND	-0.3 V to AV_{DD} + 0.2 V
Negative differential reference (REFB) to AGND	-0.3 V to AV_{DD} + 0.2 V
Serial data input/output (SDIO) / duty cycle stabilizer (DCS) to DGND	-0.3 V to DRV_{DD} + 0.3 V
Power down function selection (PDWN) to AGND	-0.3 V to +3.9 V
Serial port interface chip select (CSB) to AGND	-0.3 V to +3.9 V
Serial port interface clock (SCLK) / data format selection pin (DFS) to AGND	-0.3 V to +3.9 V
Output enable (OEB) to AGND	-0.3 V to +3.9 V
Storage temperature range	-65°C to +125°C
Power dissipation (P_D)	1158 mW 2/
Lead temperature (soldering 10 seconds)	+300°C
Junction temperature (T_J)	150°C
Thermal resistance, junction-to-case (θ_{JC})	10°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	16°C/W 3/

1.4 Recommended operating conditions.

Analog supply voltage (AV_{DD})	1.7 V to 1.9 V
Digital output driver supply voltage (DRV_{DD})	1.8 V to 3.3 V
Conversion rate, duty cycle stabilizer (DCS) enabled	20 MSPS to 125 MSPS
Conversion rate, DCS disabled	10 MSPS to 125 MSPS
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Maximum internal power dissipation is specified so that T_J does not exceed +150°C with T_A = +125°C where exposed paddle is soldered to ground.

3/ Measurement taken under absolute worst case conditions of still air chamber while mounted above the printed circuit board (PCB) to minimize PCB mounting heat sinking effects whereas exposed paddle is soldered to the ground plane.

1.5 Nominal operating performance characteristics. 4/

Analog input capacitance	10 pF 5/
Clock input voltage range	AV_{DD} - 0.3 V to AV_{DD} + 1.6 V
Clock differential input voltage	0.2 V_{PP} to 6 V_{PP}
Clock input common mode range	1.1 V to AV_{DD}
Temperature drift: offset error	±15 ppm/°C
Temperature drift: gain error	±95 ppm/°C
Input referred noise (V_{REF} = 1.0 V)	1.3 LSB rms
Differential clock input capacitance	4 pF 5/
Logic input capacitance (CSB, SCLK/DFS, OEB, PDWN)	2 pF 5/
Logic input capacitance (SDIO/DCS)	5 pF 5/
Pipeline delay (latency)	12 cycles
Aperture delay (T_A)	0.8 ns
Aperture uncertainty (jitter, T_J)	0.1 ps rms
Wake-up time	350 µs
Out of range recovery time	3 cycles

1.6 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rad(Si)/s)	100 krad(Si) 6/

4/ Unless otherwise specified, AVDD = 1.8 V; DRVDD = 2.5 V, f_S = 125 MSPS, 1.5 V_{PP} differential input, 0.75 V internal reference; AIN = −1.0 dBFS, DCS enabled. See manufacturer's datasheet for details on Ain options, reference and timing modes and diagrams, and other product application details.

5/ Input capacitance refers to the effective capacitance between pin and AGND.

6/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate sensitivity (ELDRs) effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC Solid State Technology Association

JEDEC JEP 163 - Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits.

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic inputs. (SCLK/DFS, OEB, PDWN)							
High logic input voltage 5/	V_{IH}	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	1,2,3	01	1.1		V
		M,D,P,L,R	1		1.1		
Low logic input voltage 5/	V_{IL}	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	1,2,3	01		0.7	V
		M,D,P,L,R	1			0.7	
High logic input current 5/	I_{IH}	AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	40	140	µA
		M,D,P,L,R	1		40	140	
Low logic input current 5/	I_{IL}	AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	-10	10	µA
		M,D,P,L,R	1		-10	10	
Logic inputs. (CSB)							
High logic input voltage 5/	V_{IH}	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	1,2,3	01	1.1		V
		M,D,P,L,R	1		1.1		
Low logic input voltage 5/	V_{IL}	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	1,2,3	01		0.7	V
		M,D,P,L,R	1			0.7	
High logic input current 5/	I_{IH}	AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	1	100	µA
		M,D,P,L,R	1		1	100	
Low logic input current 5/	I_{IL}	AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	-140	-40	µA
		M,D,P,L,R	1		-140	-40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic inputs. (SDIO/DCS)							
High logic input voltage 5/	V_{IH}	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	1,2,3	01	1.1		V
		M.D,P,L,R	1		1.1		
Low logic input voltage 5/	V_{IL}	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	1,2,3	01		0.7	V
		M.D,P,L,R	1			0.7	
High logic input current 5/	I_{IH}	AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	-12	10	µA
		M.D,P,L,R	1		-12	10	
Low logic input current 5/	I_{IL}	AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	-12	10	µA
		M.D,P,L,R	1		-12	10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Digital outputs, DCO, OR, SDIO								
High logic output voltage 6/ digital outputs, DCO, OR	V_{OH}	AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V		1,2,3	01	3.2		V
		I_{OH} = 50 µA	M.D,P,L,R	1		3.2		
		AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V		1,2,3		3.1		
		I_{OH} = 1.0 mA	M.D,P,L,R	1		3.1		
High logic output voltage 6/ SDIO	V_{OH}	AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V		1,2,3	01	3.1		V
		I_{OH} = 50 µA	M.D,P,L,R	1		3.1		
		AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V		1,2,3		3.05		
		I_{OH} = 1.0 mA	M.D,P,L,R	1		3.05		
High logic output voltage digital outputs, DCO, OR, SDIO	V_{OH}	AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V		1,2,3	01	2.4		V
		I_{OH} = 50 µA	M.D,P,L,R	1		2.4		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V		1,2,3		2.3		
		I_{OH} = 1.0 mA	M.D,P,L,R	1		2.3		
		AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V		1,2,3		1.7		
		I_{OH} = 50 µA	M.D,P,L,R	1		1.7		
		AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V		1,2,3		1.6		
		I_{OH} = 1.0 mA	M.D,P,L,R	1		1.6		
Low logic output voltage digital outputs, DCO, OR. SDIO	V_{OL}	DRV_{DD} = 1.8 V, 2.5 V, 3.3 V,		1,2,3	01		0.05	V
		I_{OH} = 50 µA	M.D,P,L,R	1			0.05	
		DRV_{DD} = 1.8 V, 2.5 V, 3.3 V,		1,2,3			0.2	
		I_{OH} = 0.5 mA	M.D,P,L,R	1			0.2	
Digital outputs, DCO, OR								
Low logic input current	I_{IL}	AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,		1,2,3	01	-10	10	µA
		OEB disabled	M.D,P,L,R	1		-10	10	
High logic input current	I_{IH}	AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,		1,2,3	01	-10	10	µA
		OEB disabled	M.D,P,L,R	1		-10	10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Accuracy.							
Resolution	RES		4,5,6	01	14		Bits
Integral nonlinearity negative	INLN	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,	4	01	-6		LSB
			5,6		-8		
		M,D,P,L,R	4		-6		
Integral nonlinearity positive	INLP	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4	01		6	LSB
			5,6			8	
		M,D,P,L,R	4			6	
Differential nonlinearity negative	DNLN	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4,5,6	01	-0.8		LSB
		M,D,P,L,R	4		-0.8		
Differential nonlinearity positive	DNLP	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4,6	01		1.8	LSB
			5			2.2	
		M,D,P,L,R	4			1.8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Accuracy - continued							
Offset error	OE	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4,5,6	01	-2.5	2.5	%FSR
		M,D,P,L,R	4		-2.5	2.5	
Gain error	GE	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4,5,6	01	-5	5	%FSR
		M,D,P,L,R	4		-5	5	
Analog input.							
V_{REF} voltage error	V_{error}	V_{REF} = 1.0 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	-35	+35	mV
		M,D,P,L,R	1		-35	+35	
V_{REF} load regulation, 1.0 mA	LDreg	V_{REF} = 1.0V, I_Vreg = 1.0 mA, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	-13	+13	mV
		M,D,P,L,R	1		-13	+13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power interface.							
Core supply current, nominal condition	I_{AVDD}	DC, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2	01	100	200	mA
			3		100	250	
		M,D,P,L,R	1		100	200	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	1,2,3		150	350	
		M,D,P,L,R	1		150	350	
		f_{IN} = 2.4 MHz, OEoff, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3		100	300	
		M,D,P,L,R	1		100	300	
		Power down, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3			5	
		M,D,P,L,R	1			5	
		f_{IN} = 2.4 MHz, Power standby, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3		10	100	
		M,D,P,L,R	1		10	100	
IO supply current, nominal condition	I_{DRVDD}	DC, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3	01		5	mA
		M,D,P,L,R	1			5	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, f_{IN} = 2.4 MHz	1,2,3			175	
		M,D,P,L,R	1			175	
		f_{IN} = 2.4 MHz, 6/ 8/ 5 pF load per data pin, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3			20	
		f_{IN} = 2.4 MHz, OEoff, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	1,2,3			5	
		M,D,P,L,R	1			5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power interface - continued.							
IO supply current, nominal condition	I_DRV_{DD}	Power down, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3	01		5	mA
		M,D,P,L,R	1			5	
		f_{IN} = 2.4 MHz, Power standby, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3			5	
		M,D,P,L,R	1			5	
Power, nominal condition	power	DC, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3	01		425	mW
		M,D,P,L,R	1			425	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	1,2,3			910	
		M,D,P,L,R	1			910	
		f_{IN} = 2.4 MHz, 6/ 8/ 5 pF load per data pin, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3			680	
		f_{IN} = 2.4 MHz, OEoff, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	1,2,3			560	
		M,D,P,L,R	1			560	
		Power down, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3			25	
		M,D,P,L,R	1			25	
		Power standby, 7/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	1,2,3			200	
		f_{IN} = 2.4 MHz M,D,P,L,R	1			200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power interface - continued.								
Core supply current, minimal condition	I_AV_{DD}	DC, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V		1,2	01	100	200	mA
				3		100	250	
			M,D,P,L,R	1		100	200	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V		1,2,3		150	350	
			M,D,P,L,R	1		150	350	
		OEoff, 7/ AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, f_{IN} = 2.4 MHz		1,2,3		100	300	
			M,D,P,L,R	1		100	300	
		Power down, AV_{DD} = 1.7 V, 7/ DRV_{DD} = 1.8 V		1,2,3			5	
			M,D,P,L,R	1			5	
		Power standby, 7/ AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, f_{IN} = 2.4 MHz		1,2,3		10	100	
			M,D,P,L,R	1		10	100	
IO supply current, minimal condition	I_DRV_{DD}	DC, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V		1,2,3	01		5	mA
			M,D,P,L,R	1			5	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V		1,2,3			175	
			M,D,P,L,R	1			175	
		f_{IN} = 2.4 MHz,, no load, 6/ 8/ AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V		1,2,3			15	
		OEoff, f_{IN} = 2.4 MHz, 7/ AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V		1,2,3			5	
			M,D,P,L,R	1			5	
		Power down, AV_{DD} = 1.7 V, 7/ DRV_{DD} = 1.8 V		1,2,3			5	
			M,D,P,L,R	1			5	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.7 V, 7/ DRV_{DD} = 1.8 V		1,2,3			5	
			M,D,P,L,R	1			5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power interface - continued.							
Power, minimal condition	Power	DC, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V	1,2,3	01		425	mW
		M,D,P,L,R	1			425	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	1,2,3			800	
		M,D,P,L,R	1			800	
		f_{IN} = 2.4 MHz, 6/ 8/ no load, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V	1,2,3			622	
		OEoff, 7/ AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	1,2,3			560	
		f_{IN} = 2.4 MHz M,D,P,L,R	1			560	
		Power down, 7/ AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V	1,2,3			25	
		M,D,P,L,R	1			25	
		Power standby, 7/ AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	1,2,3			200	
		f_{IN} = 2.4 MHz M,D,P,L,R	1			200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power interface - continued.							
Core supply current, maximum condition	I_AV_{DD}	DC, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2	01	100	200	mA
			3		100	250	
		M,D,P,L,R	1		100	200	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,	1,2,3		150	350	
		M,D,P,L,R	1		150	350	
		OEoff, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,	1,2,3		100	300	
		f_{IN} = 2.4 MHz M,D,P,L,R	1		100	300	
		Power down, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,	1,2,3			5	
		M,D,P,L,R	1			5	
		Power standby, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,	1,2,3		10	100	
		f_{IN} = 2.4 MHz M,D,P,L,R	1		10	100	
IO supply current, maximum condition	I_DRV_{DD}	DC, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01		5	mA
		M,D,P,L,R	1			5	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,	1,2,3			175	
		M,D,P,L,R	1			175	
		f_{IN} = 2.4 MHz, 6/ 8/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V, no load	1,2,3			25	
		f_{IN} = 2.4 MHz, OEoff, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,	1,2,3			5	
		M,D,P,L,R	1			5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power interface - continued.								
IO supply current maximum condition	I_DRV_{DD}	Power down, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V		1,2,3	01		5	mA
			M,D,P,L,R	1			5	
		f_{IN} = 2.4 MHz, Power standby, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V		1,2,3			5	
			M,D,P,L,R	1			5	
Power, maximum condition	Power	DC, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V		1,2,3	01		425	mW
			M,D,P,L,R	1			425	
		f_{IN} = 2.4 MHz, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V		1			975	
				2			950	
				3			1000	
			M,D,P,L,R	1			975	
		f_{IN} = 2.4 MHz, no load, 6/ 8/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V		1,2,3			748	
		OEoff, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,		1,2,3			560	
		f_{IN} = 2.4 MHz	M,D,P,L,R	1			560	
		Power down, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V		1,2,3			25	
			M,D,P,L,R	1			25	
		Power standby, 7/ AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V,		1,2,3			200	
		f_{IN} = 2.4 MHz	M,D,P,L,R	1			200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
Signal to noise ratio	SNR	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4	01	66		dBc
			5		57		
			6		66.5		
		M.D,P,L,R	4		66		
		f_{IN} = 2.4 MHz, 6/ 9/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		68.4		
			5		67		
			6		69.3		
		f_{IN} = 70 MHz, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V	4		65		
			5		57		
			6		65		
		M.D,P,L,R	4		65		
		f_{IN} = 70 MHz, 6/ 9/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		67.5		
			5		66.6		
			6		67.5		
		f_{IN} = 100 MHz 6/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		65		
			5		63.5		
			6		62.5		
		f_{IN} = 170 MHz 6/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		62.5		
			5		63.9		
			6		65.3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance – continued.							
Signal to noise and distortion	SINAD	f_{IN} = 2.4 MHz,	4	01	65.5		dBc
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5		56		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,					
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V,	6		64		
		AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V,					
		AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V					
		M,D,P,L,R	4		65.5		
		f_{IN} = 2.4 MHz, 6/ 9/	4		67.9		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5		65.5		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	6		69.2		
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V					
		f_{IN} = 70 MHz	4		64		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5		56		
		AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V	6		64		
		M,D,P,L,R	4		64		
		f_{IN} = 70 MHz, 6/ 9/	4		66.4		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5		65.2		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,					
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V	6		66.7		
		f_{IN} = 100 MHz 6/	4		64.5		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5, 6		63		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,					
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V					
		f_{IN} = 170 MHz 6/	4		62		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5		62.7		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	6		64.8		
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V					

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance – continued.							
Effective number of bits	ENOB	f_{IN} = 2.4 MHz	4	01	10.4		Bits
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5		9		
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6		10.3		
		M,D,P,L,R	4		10.4		
		f_{IN} = 2.4 MHz, 6/ 9/	4		11		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5		10.5		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6		11.1		
		f_{IN} = 70 MHz	4		10		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5		9		
		AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V	6		10		
		M,D,P,L,R	4		10		
		f_{IN} = 70 MHz 6/ 9/	4		10.6		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5		10.4		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6		10.6		
		f_{IN} = 100 MHz 6/	4		10.4		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5		10.1		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6		10.2		
		f_{IN} = 170 MHz 6/	4		10		
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5		10.1		
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6		10.4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance – continued.							
Second harmonic distortion	HD2	f_{IN} = 2.4 MHz,	4	01		-72	dBc
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-59	
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-70	
		M,D,P,L,R	4			-72	
		f_{IN} = 2.4 MHz, 6/ 9/	4			-76.7	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-70.7	
		AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-81.5	
		f_{IN} = 70 MHz,	4			-65	
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-59	
		AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V	6			-65	
		M,D,P,L,R	4			-65	
		f_{IN} = 70 MHz, 6/ 9/	4			-74	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-69.8	
		AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-75	
		f_{IN} = 100 MHz 6/	4			-75	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-67.8	
		AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-75	
		f_{IN} = 170 MHz 6/	4			-70	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-67.7	
		AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-71.6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance – continued.							
Third harmonic distortion	HD3	f_{IN} = 2.4 MHz,	4	01		-72	dBc
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-59	
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-70	
		M,D,P,L,R	4			-72	
		f_{IN} = 2.4 MHz, 6/ 9/	4			-78.7	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-81.3	
		AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-81.7	
		f_{IN} = 70 MHz,	4			-65	
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	5			-59	
		AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V	6			-65	
		M,D,P,L,R	4			-65	
		f_{IN} = 70 MHz, 6/ 9/	4			-73.9	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5			-75.8	
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-77.1	
		f_{IN} = 100 MHz 6/	4			-74	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5			-77	
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-76	
		f_{IN} = 170 MHz 6/	4			-74.3	
		AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V,	5			-79.6	
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6			-76	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance – continued.							
Spurious free dynamic range	SFDR	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V,	4	01	72		dBc
			5		59		
		AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	6		70		
		M,D,P,L,R	4		72		
		f_{IN} = 2.4 MHz, 6/ 9/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		75.5		
			5		70.6		
			6		78.5		
		f_{IN} = 70 MHz, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V	4		65		
			5		59		
			6		65		
		M,D,P,L,R	4		65		
		f_{IN} = 70 MHz, 6/ 9/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		71.3		
			5		69.1		
			6		73.3		
		f_{IN} = 100 MHz, 6/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		72		
			5		66.8		
			6		72.5		
		f_{IN} = 170 MHz, 6/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		70		
			5		67.5		
			6		71		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance – continued.							
Worst other spur	WoSpur	f_{IN} = 2.4 MHz, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4	01		-75	dBc
			5			-61	
			6			-75	
		M.D,P,L,R	4			-75	
		f_{IN} = 2.4 MHz, 6/ 9/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4			-87.9	
			5			-84.6	
			6			-85.2	
		f_{IN} = 70 MHz, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V	4			-70	
			5			-61	
			6			-70	
		M.D,P,L,R	4			-70	
		f_{IN} = 70 MHz, 6/ 9/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4			-86.9	
			5			-83.3	
			6			-86.4	
		f_{IN} = 100 MHz, 6/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4			-86	
			5			-84	
			6			-85	
		f_{IN} = 170 MHz, 6/ AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4			-83.4	
			5			82.7	
			6			-85	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance – continued.							
Two tone spurious free dynamic range	SFDR2	fIN = 29 MHz at -7 dBFS, fIN = 32 MHz at -7 BFS AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4	01	67		dBFS
			5		59		
			6		60		
		fIN = 169 MHz at -7 dBFS, fIN = 172 MHz at -7 BFS AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	4		67		
			5		62		
			6		69		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing characteristics.		See figures 4 and 5.					
Clock (CLK) period 10/	t_{CLK}	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	9,10,11	01	8		ns
		M,D,P,L,R	9		8		
Clock (CLK) input resistance	R_{IN}	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	1,2,3	01	8	15	kΩ
		M,D,P,L,R	1		8	15	
Clock (CLK) minimum differential V_{IN}	$minV_{INdiff}$	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	9,10,11	01	0.2		V
		M,D,P,L,R	9		0.2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.		See figures 4 and 5.					
Clock (CLK) maximum differential VIN	maxVINdiff	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, Vin Comm = Vdd / 2	9,10,11	01		3.4	V
		M,D,P,L,R	9			3.4	
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V Vin Comm = Vdd / 2	9,10,11			3.2	
		M,D,P,L,R	9			3.2	
		AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V Vin Comm = Vdd / 2	9,10,11			3.6	
		M,D,P,L,R	9			3.6	
Clock (CLK) minimum common mode V_{IN}	minVINcomm	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V, AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	9,10,11	01	0.6		V
		VinDiff = 0.2 M,D,P,L,R	9		0.6		
Clock (CLK) maximum common mode V_{IN}	maxVINcomm	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01		1.6	V
		VinDiff = 0.2 M,D,P,L,R	9			1.6	
		AV_{DD} = 1.7 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.7 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.7 V, DRV_{DD} = 3.3 V	9,10,11			1.5	
		VinDiff = 0.2 M,D,P,L,R	9			1.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.		See figures 4 and 5.					
Clock (CLK) maximum common mode V_{IN}	$maxV_{INcomm}$	AV_{DD} = 1.9 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.9 V, DRV_{DD} = 2.5 V, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V	9,10,11	01		1.7	V
		VinDiff = 0.2 M,D,P,L,R	9			1.7	
CLK pulse	tPW	DCS enabled 8/	9,10,11	01	2.4	5.6	ns
		M,D,P,L,R	9		2.4	5.6	
		DCS disabled 8/	9,10,11		3.6	4.4	
		M,D,P,L,R	9		3.6	4.4	
Data propagation delay	tPD	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V,	9,11	01	4.1	7.5	ns
		AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	10		4.1	9	
		M.D,P,L,R	9		4.1	7.5	
Data clock output (DCO) propagation delay	tDCO	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V,	9,11	01	3.6	6.5	ns
		AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	10		3.6	8.5	
		M.D,P,L,R	9		3.6	6.5	
Setup time	tS	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	2.0		ns
		M.D,P,L,R	9		2.0		
Hold time	tH	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	3.0		ns
		M.D,P,L,R	9		3.0		
SCLK period 10/	tSCLK	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	40		ns
		M.D,P,L,R	9		40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.		See figures 4 and 5.					
SCLK pulse width high time	tSCLK_HI	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	16		ns
		M,D,P,L,R	9		16		
SCLK pulse width low time	tSCLK_LO	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	16		ns
		M,D,P,L,R	9		16		
SDIO to SCLK setup time	tSCLK_DS	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	5		ns
		M,D,P,L,R	9		5		
SDIO to SCLK hold time	tSCLK_DH	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	3		ns
		M,D,P,L,R	9		3		
CSB to SCLK setup time	tSCLK_CS	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	5		ns
		M,D,P,L,R	9		5		
CSB to SCLK hold time (t_H)	tSCLK_CH	AV_{DD} = 1.8 V, DRV_{DD} = 1.8 V, AV_{DD} = 1.8 V, DRV_{DD} = 3.3 V	9,10,11	01	3		ns
		M,D,P,L,R	9		3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ The device supplied to this drawing has been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the "R" level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ This device may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A.

3/ Unless otherwise specified AV_{DD} = 1.8 V; DRV_{DD} = 2.5 V, f_S = 125 MSPS, 1.5 V_{PP} differential input, (differential clock required) 0.75 V internal reference, (R1 = 2 kΩ, R2 = 1 kΩ); AIN = −1.0 dBFS, DCS enabled. OEB = PWDN = low (external) where exposed paddle is soldered to ground.

4/ See manufacturer's datasheet for more details on Ain options, reference and timing modes and diagrams, and other product application details. Also refer to section 6.7 Application notes.

5/ DCS functional tested by applying DCO signal to low pass filter. Filter output voltages determine DCO duty cycle.

6/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots. Not tested post radiation.

7/ OEB = high used for OEB off test.
External control condition used for current limit tests (OE = PWDN = high). Internal control conditions tested functionally as part of digital patterns, modes register setting: PWDN bit = full, internal power down bits = standby.
Modes register setting: PWDN bit = standby, internal power down bits = normal power up. They are tested as input conditions and thus are guaranteed as 100% production tested.

8/ Parameter Tested without loads on Data output pins. Production testing connects Dout pins to long capacitive traces which increases I_DRVdd. I_DRVdd in normal applications is much smaller.

9/ Parameter guaranteed but not production tested at these conditions due to hardware limitations in test environment.

10/ Differential clock required, minimum period specifications guaranteed by testing at maximum frequency: tCLK minimum limits guaranteed by SNR tests at 125 MHz (8 ns period = 125 MHz CLK frequency). tSCLK minimum limits guaranteed by tSCLK_Hi, tSCLK_LO, tSCLK_DS, tSCLK_DH, tSCLK_CS, and tSCLK_CH, tests at 25 MHz (40ns period = 25 MHz SCLK frequency).

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

Case outline X

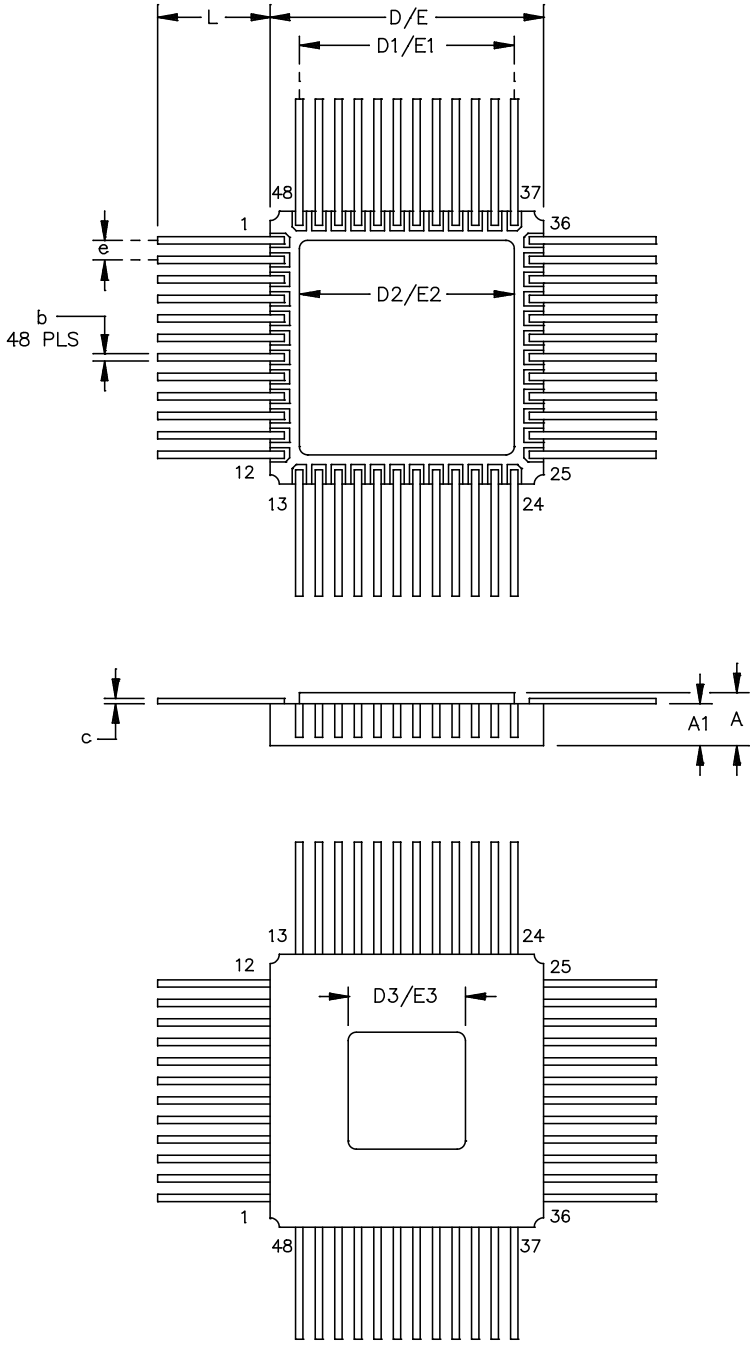


FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.0850	.1047	2.16	2.66
A1	.0709	.0866	1.80	2.2
b	.0079	.0118	0.20	0.30
c	.0079	.0118	0.20	0.30
D/E	.5547	.5717	14.09	14.52
D1/E1	.4349	.4451	11.046	11.306
D2/E2	.4450	.4501	11.303	11.455
D3/E3	.2311	.2413	5.87	6.13
e	.03685	.04315	0.936	1.096
L	.2650	.2850	6.731	7.239

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Pin 1 indicated by 0.27 mm (.0106 inch) tab on braze pad.

FIGURE 1. Case outline - continued.

Device type		01	
Case outline		X	
Terminal number	Terminal symbol	Terminal type	Description
1	D2	Digital output	Data output bits.
2	D3	Digital output	Data output bits.
3	D4	Digital output	Data output bits.
4	D5	Digital output	Data output bits.
5	D6	Digital output	Data output bits.
6	D7	Digital output	Data output bits.
7	DRGND	Power	Digital output ground.
8	DRVDD	Power	Digital output driver supply.
9	D8	Digital output	Data output bits.
10	D9	Digital output	Data output bits.
11	D10	Digital output	Data output bits.
12	D11	Digital output	Data output bits.
13	D12	Digital output	Data output bits.
14	D13(MSB)	Digital output	Data output bits.
15	OR	Digital output	Out of range indicator.
16	DRGND	Power	Digital output ground.
17	DRVDD	Power	Digital output driver supply.
18	SDIO/DCS	Digital I/O	Serial port interface (SPI) data input/output (serial port mode); duty cycle stabilizer select (external pin mode).
19	SCLK/DFS	Digital input	Serial port interface clock (serial port mode); data format select pin (external pin mode).
20	CSB	Digital input	Serial port interface chip select (active low).
21	AGND	Power	Analog ground.
22	AVDD	Power	Analog power supply.
23	AGND	Power	Analog ground.
24	AVDD	Power	Analog power supply.

FIGURE 2. Terminal connections.

Device type		01	
Case outline		X	
Terminal number	Terminal symbol	Terminal type	Description
25	SENSE	Analog input	Reference mode selection.
26	VREF	Analog I/O	Voltage reference input/output.
27	REFB	Analog output	Negative differential reference.
28	REFT	Analog output	Positive differential reference.
29	AGND	Power	Analog ground.
30	$+V_{IN}$	Analog input	Positive analog input.
31	$-V_{IN}$	Analog input	Negative analog input.
32	AGND	Power	Analog ground.
33	AV_{DD}	Power	Analog power supply.
34	CML	Analog output	Common mode level bias output.
35	RBIAS	Analog output	External bias resistor connection.
36	PDWN	Analog input	Power down function selection.
37	AGND	Power	Analog ground.
38	CLK+	Digital input	Positive clock input. (Differential clock required).
39	CLK-	Digital input	Negative clock input. (Differential clock required).
40	AV_{DD}	Power	Analog power supply.
41	AGND	Power	Analog ground.
42	AV_{DD}	Power	Analog power supply.
43	OEB	Digital input	Output enable (active low).
44	DCO	Digital output	Data clock output.
45	D0 (LSB)	Digital output	Data output bits.
46	D1	Digital output	Data output bits.
47	DRGND	Power	Digital output ground.
48	DRV_{DD}	Power	Digital output driver supply.
PAD (SEE NOTE)		Power	Exposed paddle electrically connected to ground.

NOTE: It is required that the exposed paddle be soldered to the AGND plane to achieve the best electrical and thermal performance.

FIGURE 2. Terminal connections - continued.

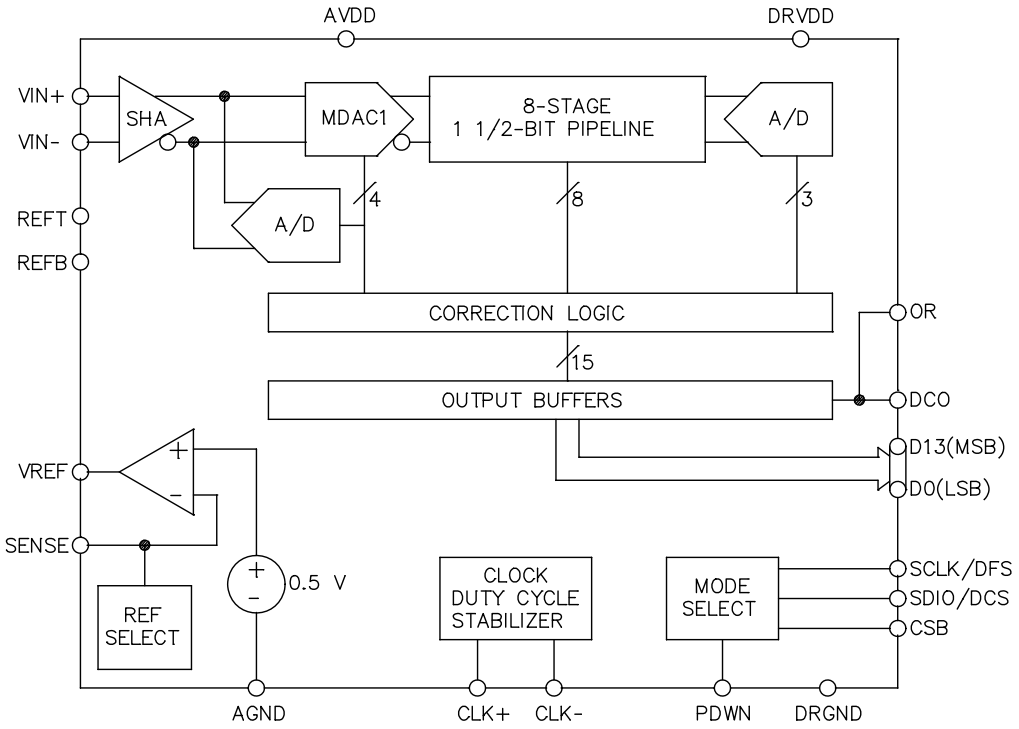


FIGURE 3. Block diagram.

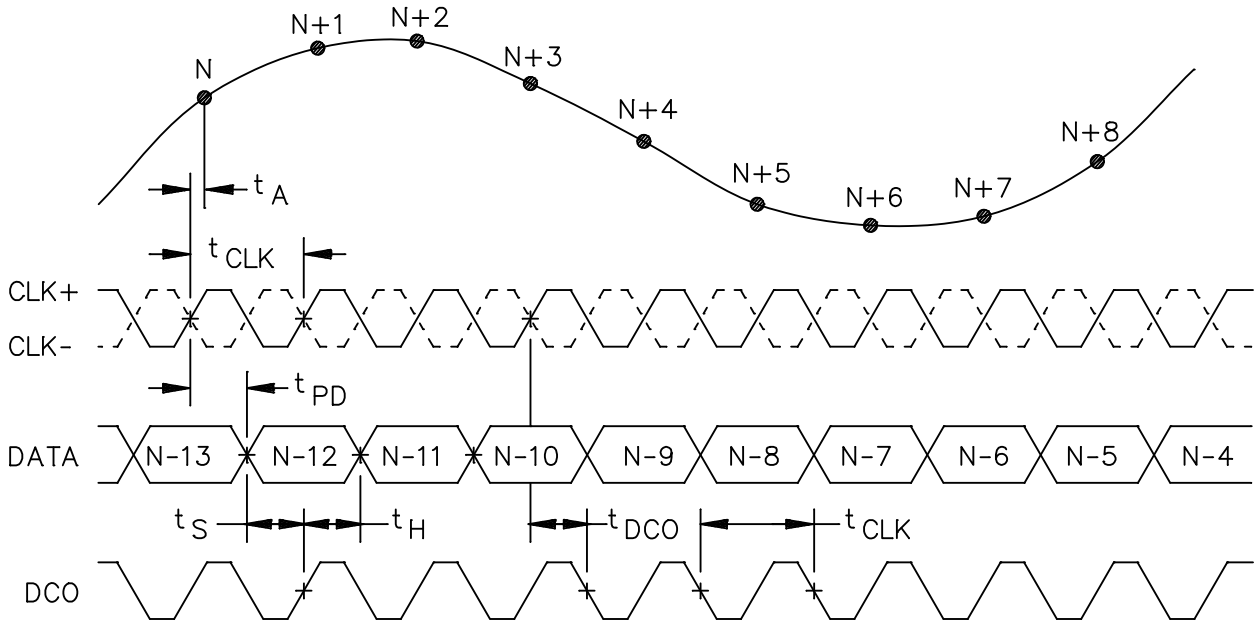


FIGURE 4. Timing waveforms.

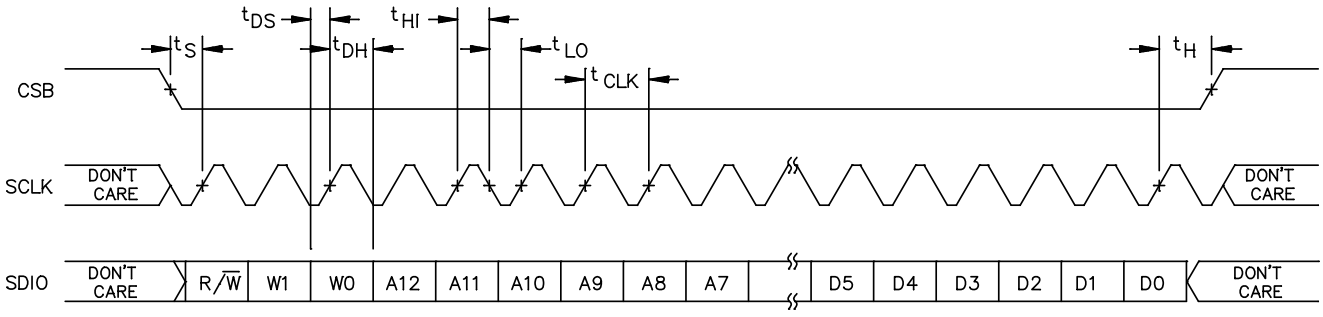


FIGURE 5. Serial port interface timing diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test shall be performed in accordance with method 1015 of MIL-STD-883. Burn-in test duration, test condition and test temperature, or approved alternatives shall be specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535 and JEDEC JEP163. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For static burn-in I, all inputs shall be connected to GND or low.

c. For static burn-in II, all inputs shall be connected to high through resistors to the supply voltage (VCC).

d. Unless otherwise specified in the QM plan, for devices class V dynamic burn-in shall be performed with test condition D, method 1015 of MIL-STD-883.

e. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 4, 5, and 6 are tested as part of device initial characterization and after design and process changes or with subsequent wafer lots as indicated in Table I.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Condition D dynamic burn-in test performed. (see 4.2.1) 5/	Required	Required
Final electrical parameters (see 4.2)	1,2,3, 1/ 4,5,6,9,10,11	1,2,3, 1/ 2/ 3/ 4/ 4,5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3, 2/ 4,5,6,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3, 2/ 3/ 4,5,6,9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 9,10,11	1,2,3, 2/ 4,5,6,9,10,11
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9 2/

1/ PDA applies to subgroup 1. For device class V, PDA applies to subgroups 1 and 7 (see 4.2.2).
2/ See table I for parameters tested or characterized for subgroups 4, 5, and 6.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see table I).
4/ Parameters marked with note 8/ in Table I are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
5/ Dynamic burn-in test shall be performed per TM 1015 with test condition D (see MIL-PRF-38535 and JEDEC JEP163).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/

Parameters	Symbol	Conditions	Limit	Units
Analog supply current	IQADD	AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	±5	mA
Digital output driver supply current	IQDRVDD	AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	±6	mA
Offset error	OE	AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	±0.4	%FSR
Gain error	GE	AV_{DD} = 1.8 V, DRV_{DD} = 2.5 V	±1	%FSR
Input current, high input voltage	I_{IH}	CSB pin, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V, V_{IN} = 3.3V	±2	µA
Input current, low input voltage	I_{IL}	CSB pin, AV_{DD} = 1.9 V, DRV_{DD} = 3.3 V, V_{IN} = 0.0V	±2	µA

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ Unless otherwise specified, the characteristics, test methods, conditions and limits shall be corresponding to the test defined in TABLE I (electrical performance characteristics). The drift values shall not be exceeded for each characteristic specified in table I.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Application notes.

6.7.1 General description. This device is a monolithic, dual supply (1.8 V core, 1.8 V to 3.3 V IO), 14-bit, / 125 MSPS analog-to-digital converter (ADC), featuring a high performance sample-and-hold amplifier (SHA) and on-chip voltage reference. The device uses a multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 125 MSPS data rates and guarantees no missing codes over the full operating temperature range.
The wide bandwidth, with differential SHA, allows a variety of user-selectable input ranges and offsets, including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate.
A differential clock input controls all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in offset binary, Gray code, or twos complement formats. A data output clock (DCO) is provided to ensure proper latch timing with receiving logic.

6.7.2 Clock input drive configuration. Single-ended clock input configuration shall not be used as it risks a reliability issue.

6.7.3 Reference configuration. A voltage reference of V_{REF} = 0.75 V (which has a span of 1.5 V) is the only V_{REF} tested for performance specification. External reference mode (SENSE pin = AVDD) may be used with 0.75 V applied to the V_{REF} pin (External reference mode uses V_{REF} as a voltage input).

Programmable reference mode (with 0.2 V < SENSE pin voltage < V_{REF} voltage, a condition causes by a resistive voltage divider between V_{REF}, SENSE and ground pins) may be used to cause V_{REF} = 0.75 V (which has a span of 1.5 V). With this V_{REF} mode, the V_{REF} voltage and span can be changed by SPI port programing. Only the V_{REF} = 0.75 V (which has a span of 1.5 V) shall be used (by writing SPI programing register OxC0 with Bit 7 and 6 = 01). If not programed, the default condition would be V_{REF} = 1.0 V and span = 2.0 V.

The V_{REF} mode where SENSE pin is tied to V_{REF} pin shall not be used.

6.7.4 Evaluation board. Operation of and requirements for the evaluation board is available from the manufacturer.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-10-11

Approved sources of supply for SMD 5962-14227 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1422701VXC	24355	AD9246AF/QMLR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Greensboro, NC 27409-9605

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.