LTC1416 (400ksps) and LTC1419 (800ksps) 14-Bit A/D Converter Demo Board

DESCRIPTION

The LTC®1416/LTC1419 are, respectively, 2µs, 400ksps and 1µs, 800 ksps sampling A/D converters. The LTC1416 draws 70mW and the LTC1419 draws 150mW. The LTC1416/LTC1419 demo board provides the user with a way to evaluate the LTC1416 and LTC1419 high speed A/D converters. In addition, the LTC1416/LTC1419 demo board is intended to illustrate the layout and bypassing techniques required to obtain optimum performance from these parts. The LTC1416/LTC1419 demo board is designed to be easy to use and requires only ±7V to ±15V supplies, a conversion-start signal and an analog input signal (single-ended or differential). As shown in the Board Photo, the LTC1416/LTC1419 are very space efficient solutions for A/D users. By combining a 14-bit A/D, sample-and-hold and reference into a single SSOP package, all the data acquisition circuitry, including the bypass capacitors, can be placed in an area of only 0.5 inch^2.

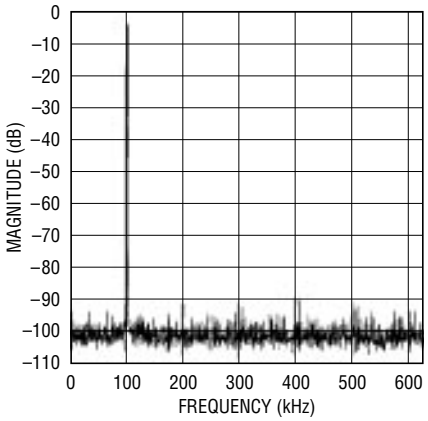
This manual describes how to use the demo board. Included are timing diagrams, power supply requirements and analog input range information. Additionally, a schematic, parts list, drawings and dimensions of all the PC board layers are included. An explanation of the layout and bypass strategies used in this board is also included, so that anyone designing a PC board using the LTC1416/LTC1419 will be able to get the maximum performance from the device. The LTC1416/LTC1419 are intended for applications in telecommunications, digital signal processing, imaging, or any high speed, high resolution data acquisition application. **Gerber files for this circuit board are available. Call the LTC factory.**

Some key features of this demo board include:

- Proven 400ksps (LTC1416) and 800ksps (LTC1419) 14-bit ADC surface mount layout
- Actual ADC footprint is only 0.5 inch^2 including bypass capacitors
- 80dB SINAD and 90dB THD at 200kHz (LTC1416) and 80dB SINAD and 86dB THD at 400kHz (LTC1419) inputs

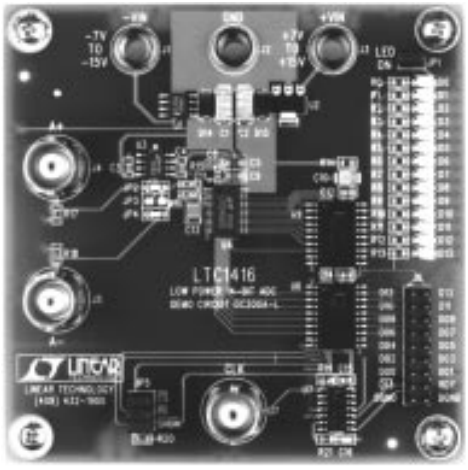
TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

4096 Point FFT of LTC1419 Demo Board



DC200 TA01

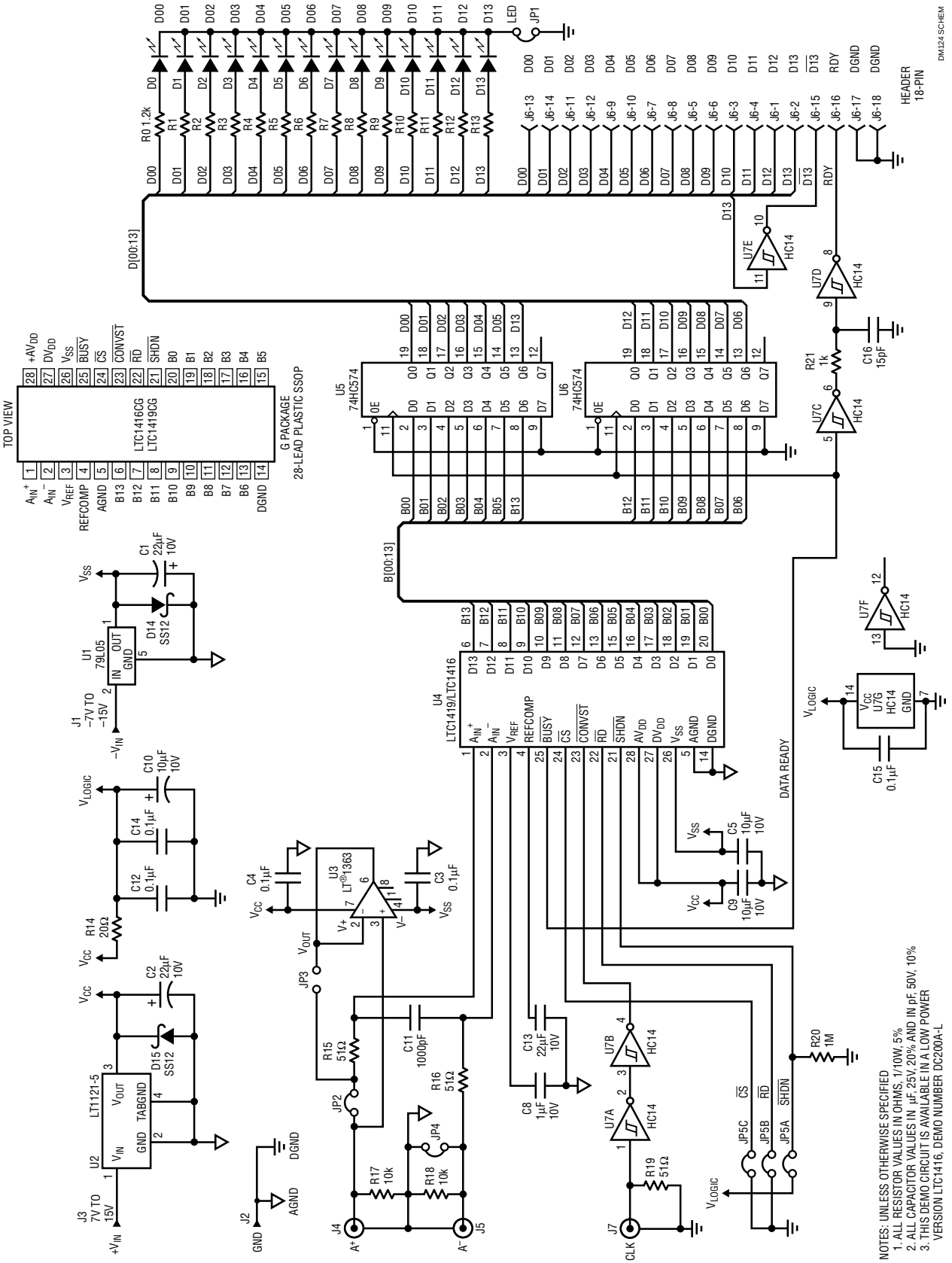
Component Side



DC200 BdPhoto

PACKAGE AND SCHEMATIC DIAGRAMS

LTC1416/LTC1419 Demonstration Board Features Analog Input Signal Buffer, 400ksps/800ksps, Parallel Data Output 14-bit ADC, Data Latches and LED Binary Data Display. Latched Conversion Data is Available on the 18-Pin Header, J6



PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1, C2	2	TAJC226M010R	22uF 10V 20% Tantalum Capacitor	AVX	207-282-5111
C3, C4, C12, C14, C15	5	08053C104MAT1A	0.1uF 25V 20% X7R Capacitor	AVX	803-946-0362
C5, C9	2	1206ZG106ZAT1A	10uF 10V Y5V Capacitor	AVX	803-946-0362
C8	1	0603ZG105ZAT1A	1uF 10V Y5V Capacitor	AVX	803-946-0362
C10	1	TAJB106M010R	10uF 10V 20% Tantalum Capacitor	AVX	207-282-5111
C11	1	06033A102KAT1A	1000pF 25V 10% NPO Capacitor	AVX	803-946-0362
C13	1	1210ZG226ZAT1A	22uF 10V Y5V Capacitor	AVX	803-946-0362
C16	1	08055A150KAT1A	15pF 50V 10% NPO Capacitor	AVX	803-946-0362
D0 to D13	14	LN1251C-(TR)	2.1V 15mA Red SMT LED	Panasonic	201-348-5217
D14, D15	2	SS12-PKG11	20V 1A SMA Schottky Diode	General Inst	516-847-3000
J1, J2, J3	3	575-4	Standard Banana Jack Connector	Keystone	718-956-8900
J4, J5, J7	3	112404	50Ω BNC, PCB-Vertical Connector	Connex	805-378-6464
J6	1	PZC09DFAN	18-Pin 2-Row 0.100cc Header Connector	Sullins	760-744-0125
JP1	1	PZC02SAAN	2-Pin 0.100cc 0.025sq Jumper	Sullins	760-744-0125
JP2, JP3, JP4	3	JL-100-25-T	0.100cc 22-AWG Wire Jumper	Samtec	800-726-8329
JP5	1	PZC03DFAN	6-Pin 2-Row 0.100cc 0.025sq Jumper	Sullins	760-744-0125
R0 to R13	14	CR10-122JM	1.2k 1/10W 5% Chip Resistor	TAD	714-255-9123
R14	1	CR10-200JM	20Ω 1/10W 5% Chip Resistor	TAD	714-255-9123
R15, R16	2	RR0816Q510D	51Ω 1/16W 0.5% Thin Film Chip Resistor	Thin Film Tech	507-625-8445
R17, R18	2	CR10-103JM	10k 1/10W 5% Chip Resistor	TAD	714-255-9123
R19	1	CR10-510JM	51Ω 1/10W 5% Chip Resistor	TAD	714-255-9123
R20	1	CR10-105JM	1M 1/10W 5% Chip Resistor	TAD	714-255-9123
R21	1	CR10-102JM	1k 1/10W 5% Chip Resistor	TAD	714-255-9123
U1	1	MC79L05ACDR1	79L05 –5V SO-8 Regulator IC	Motorola	602-655-3005
U2	1	LT1121CST-5	5V SOT-224 Regulator IC	LTC	408-432-1900
U3	1	LT1363CS8	SO-8 Op Amp IC	LTC	408-432-1900
U4	1	LTC1416CG	SSOP-28 14-Bit ADC IC	LTC	408-432-1900
U5, U6	2	MC74HC574ADW	SOL-20 Flip-Flop Octal D IC	Motorola	602-655-3005
U7	1	MC74HC14AD	SO-14 Hex-Inv Schmitt IC	Motorola	602-655-3005
	4	SSC02SYAN	0.100cc Shunt	Sullins	800-726-8329
	4		#4-40 1/4" Screw	Any	
	4	1902C	Nylon Hex #4-40 1/2" Standoff	Keystone	718-956-8900

QUICK START GUIDE

This demonstration board is easily set up for evaluating the LTC1416/LTC1419. Follow the procedure below for proper operation.

1. Connect a –7V to –15V supply (J1), 7V to 15V supply (J3), 0V or ground (J2), input test signal generator (J4) and conversion clock source (J7) to the board as shown in Figure 1. As delivered, the board is configured for a ±2.5V input referenced to ground (JP2 and JP4 are shorted). Differential inputs can be converted by removing the shorting connector on JP4. The demonstration board also includes an LT1363 input buffer amplifier operating with a gain of 1. The input signal can be buffered by removing the shorting connector from JP2 and placing it on JP3.
2. The LTC1416/LTC1419 demo board includes an input filter with a cutoff frequency of 1.56MHz. For lower input frequencies, best results are obtained by using an optional filter. The TTE J3449-100k-500-20 is a

QUICK START GUIDE

100kHz lowpass filter and works well for frequencies below 100kHz. At the Nyquist frequency of 200kHz, the TTE LE1182T-200k-400-720B 200kHz lowpass or TTE Q70T-200k-30k-400-720B 200kHz bandpass filters work well. The signal generator and filter should produce < –96dB THD.

3. Adjust the magnitude of the input signal to within 10mV of negative and positive full scale. This ensures that the maximum SINAD is achieved without the risk of overdriving the input and producing unwanted distortion. The conversion clock frequency can be set within the range of 0kHz to 400kHz.
4. The conversion results can be observed in several ways. The onboard LEDs indicate the state of each data bit. This is useful for giving a preliminary indication that the conversions are taking place and verifying results when converting DC signals. The 14-bit parallel output data is available on header J6. This allows monitoring of each bit and can be connected to a logic analyzer, DSP or oscilloscope. The data format is two's complement. Offset binary format is also available by using $\overline{D13}$ instead of D13.
5. Dynamic performance can be measured by using an FFT-based analyzer. By synchronizing the analog input signal's frequency to the conversion rate, or using a windowing function, accurate SINAD, THD or other dynamic characteristics can be evaluated.

OPERATION

OPERATING THE BOARD

Powering the Board

To use the demo board, apply ±7V to ±15V at 200mA to the banana jacks J1 and J3, and 0V (GND) to J2. Be careful to observe the correct polarity. Internal regulators provide ±5V to the LTC1416/LTC1419. An LT1121-5 regulator (U2) provides 5V for analog and digital circuitry; –5V is provided for the A/D and buffer by the MC79L05 regulator (U1).

The Analog Input

The LTC1416/LTC1419 have a unique feature not found on previous ADCs: differential inputs with good common mode rejection from DC to over 10MHz. Although this feature is extremely valuable for rejecting noise and measuring differential signals, the board can also be used to evaluate the LTC1416/LTC1419 in single-ended mode (with the "–" input grounded). This board allows evaluation in either mode.

Differential (bipolar) analog signals are applied to the LTC1416/LTC1419 demo board using BNC connectors J4 (noninverting + input) and J5 (inverting – input). The analog signal input range is ±2.5V.

The LTC1416/LTC1419 A_{IN}^+ (noninverting) and A_{IN}^- (inverting) inputs have a common mode range of V_{SS} to V_{DD}. The full-scale differential between the signals applied to A_{IN}^+ and A_{IN}^- is ±2.5V. For example, when a 1.5V signal is applied to the A_{IN}^- input, the negative-to-positive full-scale input range of A_{IN}^+ is –1V to 4V, corresponding to an output code of 1000 0000 0000 to 0111 1111 1111.

The demo board is delivered with jumpers JP2 and JP4 closed. This configures the board for a ±2.5V input signal centered around ground and applied to J4 (A_{IN}^+).

The board includes a recommended lowpass filter (R15 and R16, and C11) across the differential inputs. With the component values shown, the cutoff frequency (f_S) is:

$$\frac{1}{2\pi(102\Omega)(1000pF)} = 1.56MHz$$

These values can be altered to meet other circuit and input signal requirements. For lower bandwidth input signals, increase the value of C11. For undersampling applications that take advantage of the input circuitry's wide bandwidth, decrease the capacitance of C11.

The best way to observe the performance of the LTC1416/LTC1419 is to drive it directly from a low impedance signal source. However, since some applications involve high

OPERATION

output impedance sources, the board also has provisions for an onboard LT1363 high speed operational amplifier. The LT1363, operating as a noninveting buffer, provides the LTC1416/LTC1419 with a fast settling, low impedance signal that allows the input voltage to settle fully between conversions. The buffer is recommended if the source impedance of the input signal is greater than 930Ω. The LT1363 demonstrates how to properly drive the LTC1416/LTC1419. When using the LT1363, open JP2 and close JP4 and JP3.

Optimum performance is achieved using a signal source that has low output impedance, is low noise and has low distortion. Signal generators, such as the B & K Type 1051 Sine Generator, give excellent results. Further, this generator can be configured to operate referenced to a master clock signal, as shown in Figure 1.

Applying the Conversion Start Signal

A conversion is initiated by a falling edge on the $\overline{\text{CONVST}}$ input (BNC J7). The $\overline{\text{CONVST}}$ input uses TTL or CMOS levels. As shown in Figure 2, $\overline{\text{CONVST}}$ should remain low until the conversion is completed or returned high within 420ns of the negative going edge, as shown in Figure 3. During a conversion, transitions on the $\overline{\text{CONVST}}$ input can cause errors in the D_{OUT} output.

Reading the Output Data

The ADC data outputs are buffered by the two 74HC574 latches and are available on connector J6. The latches drive the LEDs and connector J6. In a practical circuit, latches are not required unless the ADC is tied to a noisy data bus. (Refer to the LTC1416 or LTC1419 data sheet for details on different digital interface modes.)

The output data format of the LTC1416/LTC1419 is two's complement. The data can be converted to offset binary by using $\overline{\text{D13}}$ instead of D13. Offset binary is used when an FFT is to be performed on the sampled data. A Data Ready line (J6, Pin 16) is provided to latch the D_{OUT} word. D_{OUT} is valid on the rising edge of Data Ready. Two ground lines are provided on the connector and should be connected to the receiving system.

The LTC1416/LTC1419 D_{OUT} word can be acquired with a logic analyzer. Conversion data can be stored on a disk and easily transferred to a PC by using a logic analyzer that has a PC compatible floppy drive (such as an HP1663A). Once the data is transfered to a PC, use programs such as MathCAD or Excel to calculate FFTs. Use the FFTs to obtain LTC1416/LTC1419 AC specifications, such as signal-to-noise ratio and total harmonic distortion.

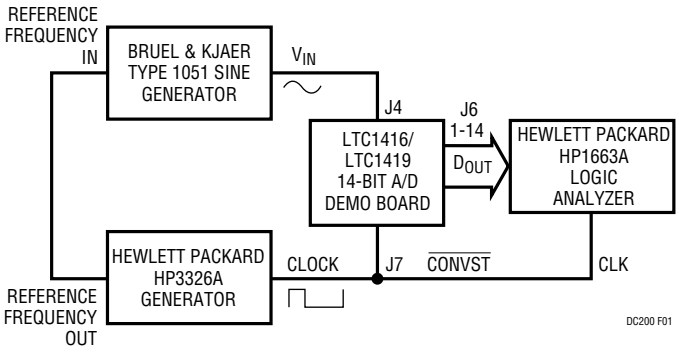


Figure 1. Typical Setup for LTC1419 Demo Board

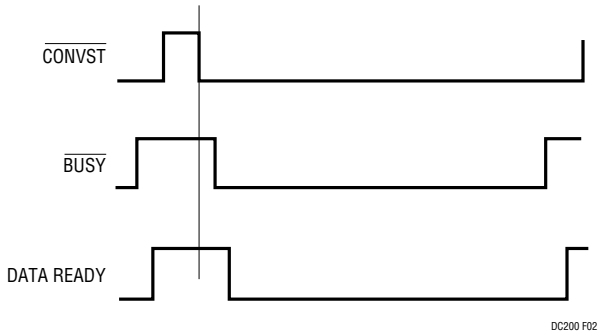


Figure 2. Timing Diagram

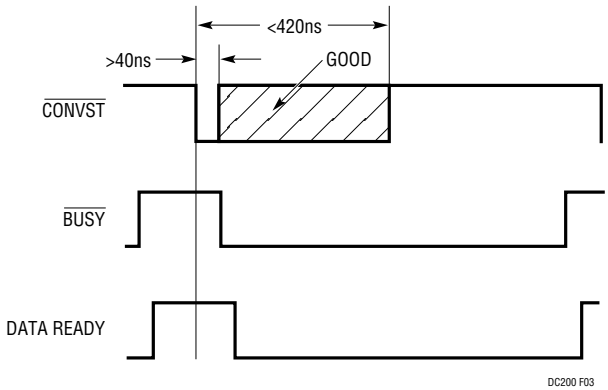


Figure 3. Alternative Timing Diagram

OPERATION

LEDs D0 to D13 provide a visual display of the LTC1416/LTC1419 digital output word. D0 and D13 display the logic state of the LSB and MSB, respectively. Remove jumper JP1 to disable the LEDs, reducing supply consumption up to 37mA.

Driving $\overline{CS}$, $\overline{RD}$ and $\overline{SHDN}$ Pins

Jumpers for $\overline{SHDN}$, $\overline{RD}$ and $\overline{CS}$ (JP5A to JP5C) are shorted for normal operation. The jumpers can be removed and these lines externally driven if desired. See the LTC1416 or LTC1419 data sheet for details on driving these lines.

LAYOUT

A well-designed printed circuit board layout incorporating the LTC1416/LTC1419 uses separate analog and digital ground planes. Except for connecting them near U4's Pin 14, completely isolate the ground planes from each other. Additionally, they should not overlap if they are on different printed circuit board layers. Connecting the LTC1416/LTC1419 analog (AGND) and digital (DGND) pins to the analog ground plane ensures the lowest noise operation.

The demonstration board layout (section titled "PCB Layout and Film") shows the best way to configure and connect the ground planes. To ensure maximum ground plane efficiency, especially for the analog ground plane, it is important to minimize plane-breaking traces.

POWER SUPPLY CONNECTIONS AND BYPASSING

Analog and digital positive supply pins, AV_{DD} and DV_{DD} respectively, are connected at the device and to the 5V supply with a single trace. The negative supply pin (V_{SS}) is connected to the –5V supply. The best performance is achieved by careful attention to proper bypassing. Bypass AV_{DD} and DV_{DD} together to the analog ground plane with a 10µF monolithic ceramic capacitor. Bypass V_{SS} to the analog ground plane with its own 10µF monolithic ceramic capacitor.

The internal voltage reference requires a 22µF monolithic ceramic capacitor connected between the REFCOMP pin and the analog ground plane. This bypass capacitor is necessary because the LTC1416/LTC1419 internal reference requires a bypass capacitor of at least 1µF for stable operation. Reference noise can be reduced even further by using a 1µF monolithic ceramic capacitor connected between the V_{REF} pin and the analog ground plane.

As with all high accuracy, high resolution circuits, the best performance is achieved by minimizing the lead lengths of the bypass capacitors.

Table 1. Functional Description of User-Configurable Jumpers

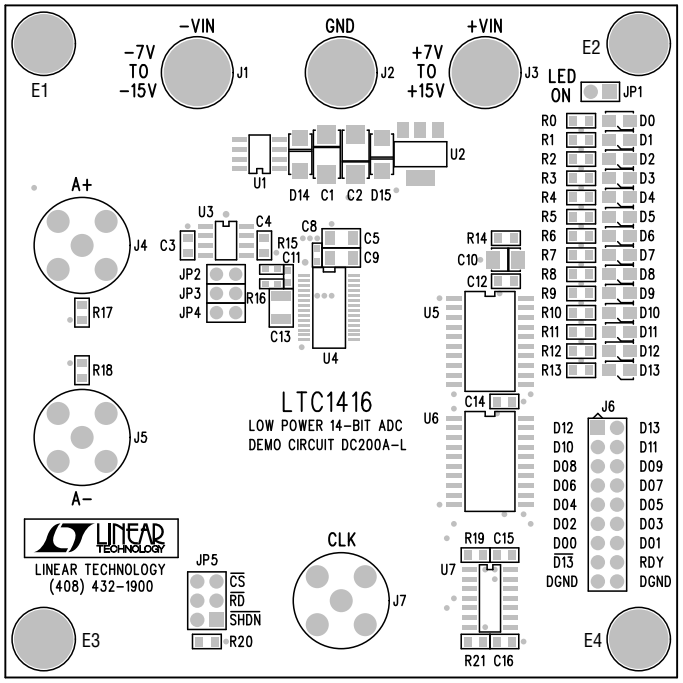
JUMPER	JUMPER NAME	JUMPER CONNECTION
JP1	LED Enable	Shorting Enables LED Operation. Opening Disables LED Operation
JP2	A_{IN}^+	Shorted for Unbuffered Operation. Open When Using the Noninverting Input Buffer. See JP3
JP3	Noninverting Input Buffer Bypass	Open for Normal Operation. Short for Buffered Input Signals and Open JP2
JP4	A_{IN}^-	Shorted for Single-Ended Operation. Open for Differential Input Signals
JP5A	$\overline{SHDN}$	Shorted for Normal Operation. Open to Externally Drive the $\overline{SHDN}$ Pin with a Logic Low for Shutdown Mode or with a Logic High for Normal Operation
JP5B	$\overline{RD}$	Shorted for Normal Operation. Open to Externally Drive the $\overline{RD}$ Pin
JP5C	$\overline{CS}$	Shorted for Normal Operation. Open to Externally Drive the $\overline{CS}$ Pin

OPERATION

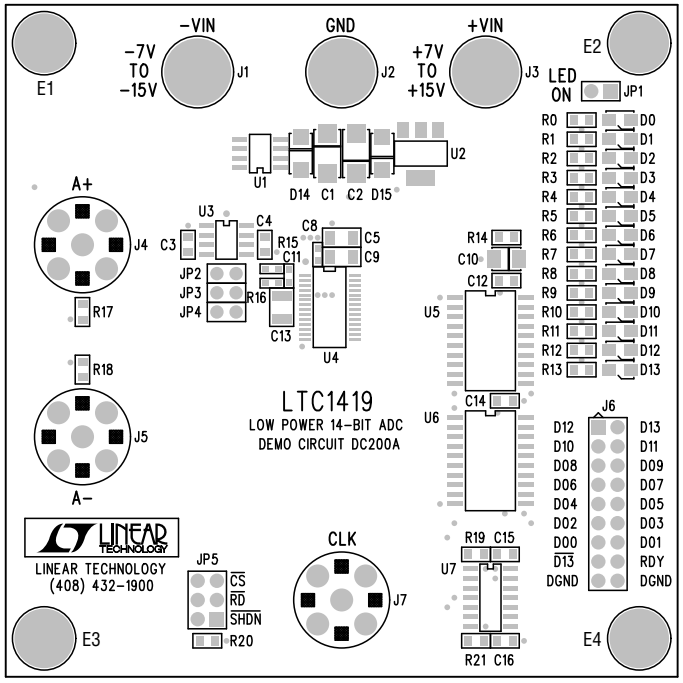
Table 2. Input and Output Pin Functional Description

INPUT/OUTPUT PIN	FUNCTION
E1	AGND (Mounting Hole)
E2	DGND (Mounting Hole)
E3	DGND (Mounting Hole)
E4	DGND (Mounting Hole)
J1	Negative Supply Voltage: −7V to −15V at 100mA
J2	Supply Ground
J3	Positive Supply Voltage: 7V to 15V at 100mA
J4	A_{IN}^+, Noninverting Input: ±2.5V, Referenced to A_{IN}^-. Input Voltage Range: V_{SS} to AV_{DD} (DV_{DD})
J5	A_{IN}^-, Inverting Input: ±2.5V, Referenced to A_{IN}^+. Input Voltage Range: V_{SS} to AV_{DD} (DV_{DD})
J6-1	D12
J6-2	D13 (MSB)
J6-3	D10
J6-4	D11
J6-5	D08
J6-6	D09
J6-7	D06
J6-8	D07
J6-9	D04
J6-10	D05
J6-11	D02
J6-12	D03
J6-13	D00
J6-14	D01
J6-15	$\overline{D13}$ (MSB)
J6-16	RDY Output (End of Conversion)
J6-17, 18	Digital Ground
J7	Convert Start: 0V to 5V

PCB LAYOUT AND FILM

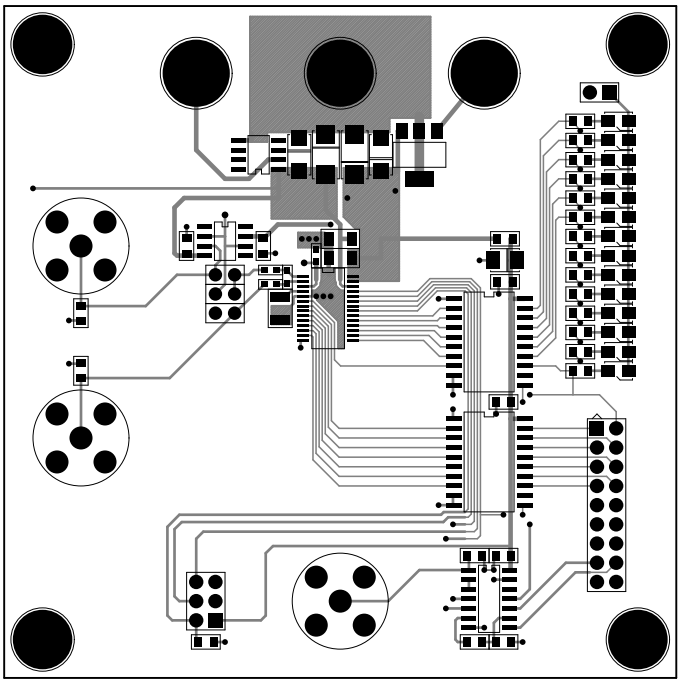


LTC1416 Component Side Silkscreen

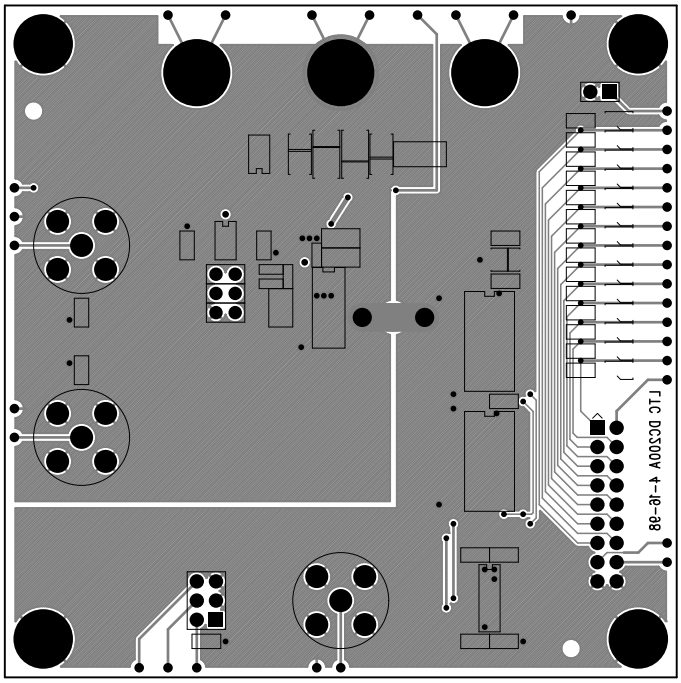


LTC1419 Component Side Silkscreen

PCB LAYOUT AND FILM

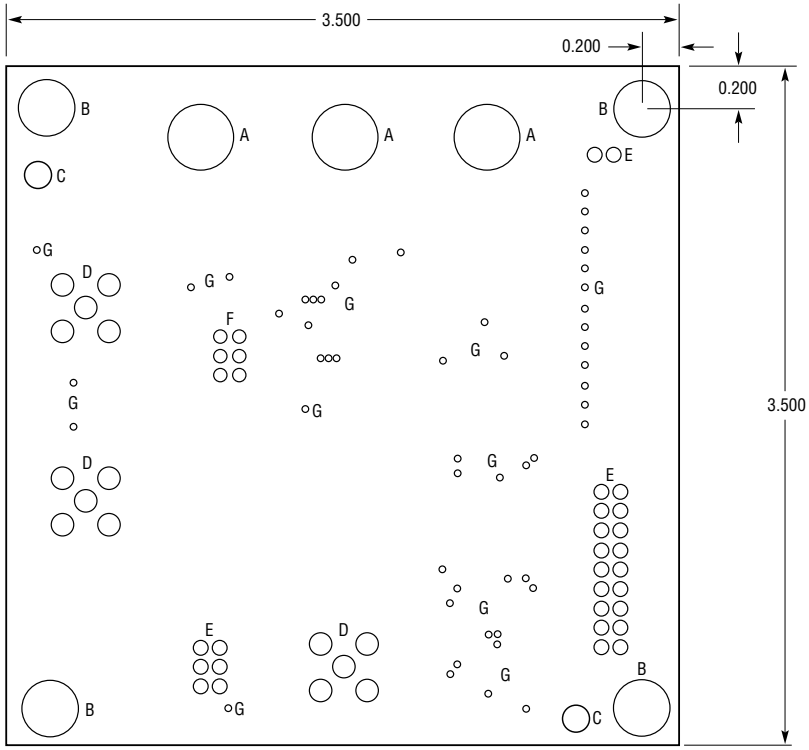


Component Side



Solder Side

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED
1. WORKMANSHIP SHALL BE IN ACCORDANCE WITH IPC-A-600E
2. ALL DIMENSIONS ARE IN INCHES, ±0.003
   FINISHED HOLE SIZES ARE +0.003/–0
3. FINISHED MATERIAL IS FR4, 0.062" THICK, 2 OZ Cu, 2 LAYERS
   PLATED HOLE WALL THICKNESS IS 0.001 MINIMUM
   INTERNAL LAYERS ARE 1 OZ Cu
4. PROCESS/PLATING SMOBC
5. SOLDERMASK BOTH SIDES USING GLOSSY GREEN LPI
6. SILKSCREEN COMPONENT SIDE USING WHITE NONCONDUCTIVE INK

HOLE CHART FOR SINGLE IMAGE

SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	0.209	3	YES
B	0.120	4	YES
C	0.070	2	NO
D	0.052	15	YES
E	0.040	26	YES
F	0.031	6	YES
G	0.015	52	YES
	TOTAL HOLES	108	

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