# 46 dBm (40 W), 0.9 GHz to 1.6 GHz, GaN Power Amplifier

Data Sheet **ADPA1105**

## FEATURES

**Output power with $P_{IN}$ = 19 dBm: 46 dBm typical**
**Small signal gain: 34.5 dB typical at 0.9 GHz to 1.4 GHz**
**Power gain with $P_{IN}$ = 19 dBm: 27 dB typical**
**Bandwidth: 0.9 GHz to 1.6 GHz**
**PAE with $P_{IN}$ = 19 dBm: 60% typical at 0.9 GHz to 1.4 GHz**
**Supply voltage: $V_{DD}$ = 50 V at 400 mA on 10% duty cycle**
**32-Lead, 5 mm × 5 mm, LFSCP_CAV package**

## APPLICATIONS

**Weather radar**
**Marine radar**
**Military radar**

## FUNCTIONAL BLOCK DIAGRAM

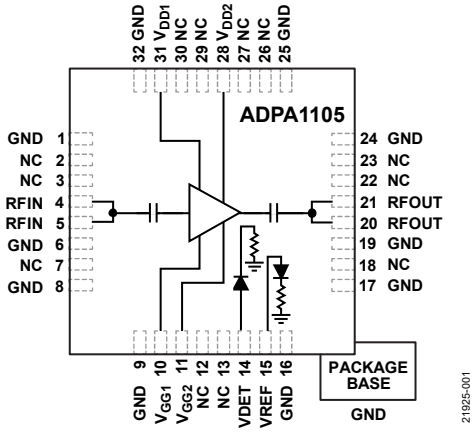


*Figure 1.*

## GENERAL DESCRIPTION

The ADPA1105 is a gallium nitride (GaN), broadband power amplifier that delivers 46 dBm (40 W) with 60% typical power added efficiency (PAE) across a bandwidth of 0.9 GHz to 1.4 GHz. The ADPA1105 provides ±0.5 dB gain flatness across a bandwidth of 0.9 GHz to 1.4 GHz.

The ADPA1105 is ideal for pulsed applications such as wireless infrastructure, radar, public mobile radio, and general-purpose amplifications.

The ADPA1105 comes in a 32-lead, lead frame chip scale package, premolded cavity (LFCSP_CAV).

**Rev. 0** **Document Feedback**


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**Technical Support** **www.analog.com**

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## REVISION HISTORY

**10/2020—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

$T_A$ = 25°C, supply voltage ($V_{DD}$) = 50 V, $I_{DQ}$ = 400 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 0.9 GHz to 1.4 GHz, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | | 0.9 | | 1.4 | GHz | |
| GAIN | | | | | | |
| Small Signal Gain | | 32 | 34.5 | | dB | |
| Gain Flatness | | | ±0.5 | | dB | |
| RETURN LOSS | | | | | | |
| Input | | | 16 | | dB | |
| Output | | | 9 | | dB | |
| POWER | | | | | | |
| Output Power ($P_{OUT}$) | | | | | | |
| Input Power ($P_{IN}$) = 19 dBm | | 44 | 46 | | dBm | |
| Power Gain | | | | | | |
| $P_{IN}$ = 19 dBm | | 25 | 27 | | dB | |
| PAE | | | | | | |
| $P_{IN}$ = 19 dBm | | | 60 | | % | |
| TARGET QUIESCENT CURRENT | $I_{DQ}$ | | 400 | | mA | Adjust the gate control voltage ($V_{GG1}$, $V_{GG2}$) to be between −4 V and 0 V to achieve an $I_{DQ}$ = 400 mA typical value |

$T_A$ = 25°C, $V_{DD}$ = 50 V, $I_{DQ}$ = 400 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 1.4 GHz to 1.6 GHz, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | | 1.4 | | 1.6 | GHz | |
| GAIN | | | | | | |
| Small Signal Gain | | 30.5 | 32.5 | | dB | |
| Gain Flatness | | | ±0.9 | | dB | |
| RETURN LOSS | | | | | | |
| Input | | | 11 | | dB | |
| Output | | | 14 | | dB | |
| POWER | | | | | | |
| $P_{OUT}$ | | | | | | |
| $P_{IN}$ = 19 dBm | | 44 | 46 | | dBm | |
| Power Gain | | | | | | |
| $P_{IN}$ = 19 dBm | | 25 | 27 | | dB | |
| PAE | | | | | | |
| $P_{IN}$ = 19 dBm | | | 57 | | % | |
| TARGET QUIESCENT CURRENT | $I_{DQ}$ | | 400 | | mA | Adjust the gate control voltage ($V_{GG1}$, $V_{GG2}$) to be between −4 V and 0 V to achieve an $I_{DQ}$ = 400 mA typical value |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Drain Bias Voltage ($V_{DD1}$, $V_{DD2}$) | 55 V dc |
| Gate Bias Voltage ($V_{GG1}$, $V_{GG2}$) | −5 V to 0 V dc |
| Radio Frequency Input Power (RFIN) | 30 dBm |
| Maximum Drain Bias | |
| Pulse Width | 500 µs |
| Duty Cycle | 20% |
| Drain Bias Pulse Width = 100 µs at 10% Duty Cycle | |
| Maximum Pulsed Power Dissipation ($P_{DISS}$), Base Temperature ($T_{BASE}$) = 85°C, Derate 473 mW/°C Above 85°C | 54.5 W |
| Nominal Pulsed Peak Channel Temperature, $P_{IN}$ = 19 dBm, $P_{DISS}$ = 33.6 W at 0.9 GHz | 155.9°C |
| Drain Bias Pulse Width = 200 µs at 20% Duty Cycle | |
| Maximum Pulsed Power Dissipation ($P_{DISS}$) (Base Temperature ($T_{BASE}$) = 85°C, Derate 355 mW/°C Above 85°C) | 40.8 W |
| Nominal Pulsed Peak Channel Temperature $P_{IN}$ = 19 dBm, $P_{DISS}$ = 33.6 W at 0.9 GHz[1] | 179.7°C |
| Maximum Channel Temperature | 200°C |
| Maximum Peak Reflow Temperature | 260°C |
| Storage Temperature Range | −60°C to +125°C |
| Operating Temperature Range | −40°C to +85°C |

[1] Worst case frequency for $P_{DISS}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to the PCB thermal design is required.

$\theta_{JC}$ is the junction to case thermal resistance (°C/W) of the device.

**Table 4. Thermal Resistance**

| Package Type[1] | $\theta_{JC}$ | Unit |
|---|---|---|
| CG-32-2 | | |
| Drain Bias Pulse Width = 100 µs[2] | 2.11 | °C/W |
| Drain Bias Pulse Width = 200 µs[3] | 2.82 | °C/W |

[1] The $\theta_{JC}$ value was determined by measuring $\theta_{JC}$ under the following conditions: the heat transfer is solely because of the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.
[2] At 10% duty cycle.
[3] At 20% duty cycle.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

### *ESD Ratings for ADPA1105*

**Table 5. ADPA1105, 32-Lead LFCSP_CAV**

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | 250 | 1A |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

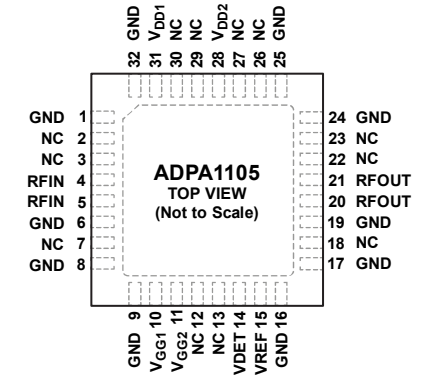


*Figure 2. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 6, 8, 9, 16, 17, 19, 24, 25, 32 | GND | The GND pins must be connected to RF and dc ground. See Figure 6 for the interface schematic. |
| 2, 3, 7, 12, 13, 18, 22, 23, 26, 27, 29, 30 | NC | The NC pins are not connected internally. However, all data shown is measured with the NC pins connected to RF and dc ground externally. |
| 4, 5 | RFIN | RF Input. The RFIN pins are ac-coupled and are matched to 50 Ω. See Figure 3 for the interface schematic. |
| 10 | $V_{GG1}$ | Gate Control, First Stage Gate Bias. See Figure 3 for the interface schematic. |
| 11 | $V_{GG2}$ | Gate Control, Second Stage Gate Bias. See Figure 4 for the interface schematic. |
| 14 | VDET | Detector Diode to Measure RF Output Power. Output power detection via VDET requires the application of a dc bias voltage through an external series resistor. Used in combination with the VREF pin, the difference in voltage (VREF − VDET) is a temperature compensated dc voltage that is proportional to the RF output power. |
| 15 | VREF | Reference Diode for Temperature Compensation of VDET RF Output Power Measurements. VREF requires the application of a dc bias voltage through an external series resistor. |
| 20, 21 | RFOUT | RF Output. The RFOUT pins are ac-coupled and are matched to 50 Ω. See Figure 4 for the interface schematic. |
| 28 | $V_{DD2}$ | Amplifier Power Supply Voltage, Second Stage Drain Bias. See Figure 4 for the interface schematic. |
| 31 | $V_{DD1}$ | Amplifier Power Supply Voltage, First Stage Drain Bias. See Figure 3 for the interface schematic. |
| | EPAD | Exposed Pad. The exposed pad must be connected to RF and dc ground. |

## INTERFACE SCHEMATICS

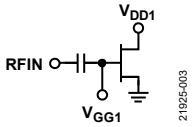


*Figure 3. RFIN, $V_{GG1}$, and $V_{DD1}$ Interface*

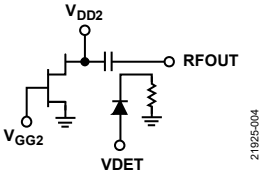


*Figure 4. RFOUT, $V_{GG2}$, $V_{DD2}$, and VDET Interface*

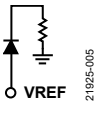


*Figure 5. VREF Interface*


*Figure 6. GND Interface*

# TYPICAL PERFORMANCE CHARACTERISTICS

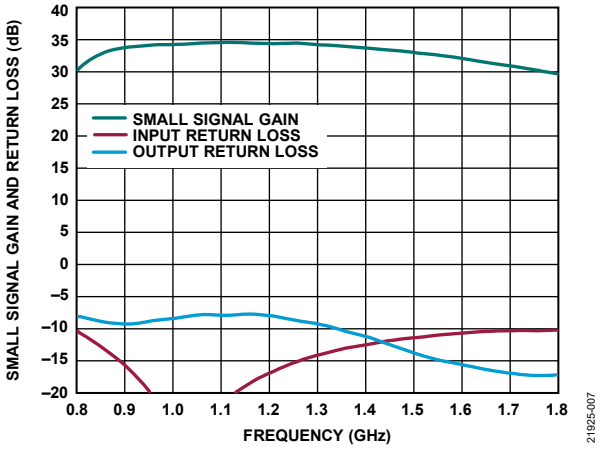


Figure 7. Small Signal Gain and Return Loss vs. Frequency

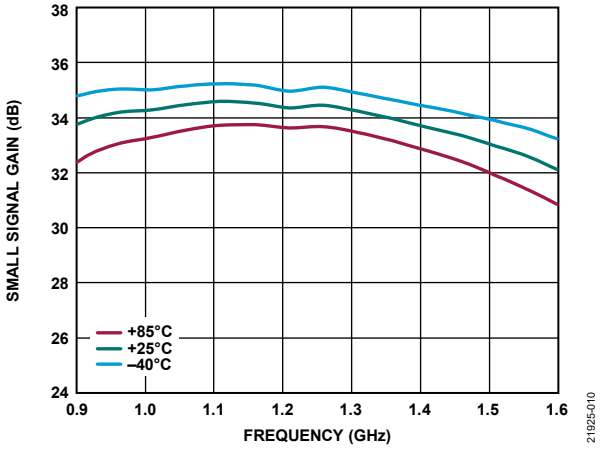


Figure 10. Small Signal Gain vs. Frequency at Various Temperatures

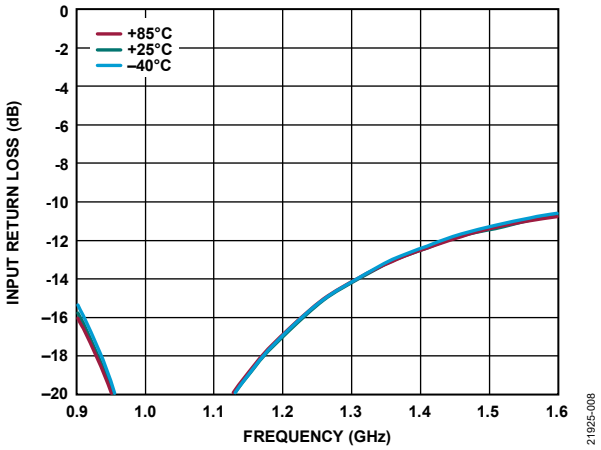


Figure 8. Input Return Loss vs. Frequency at Various Temperatures

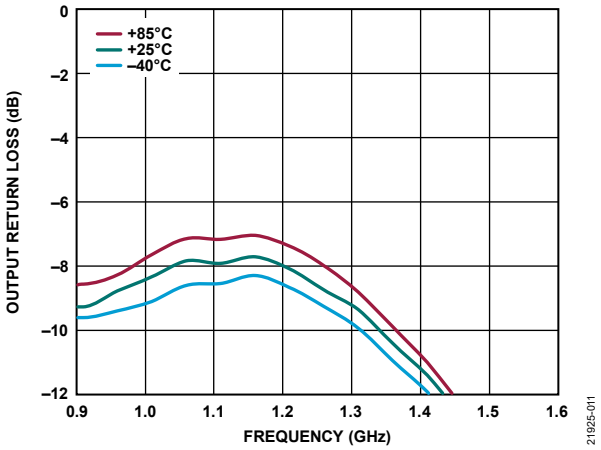


Figure 11. Output Return Loss vs. Frequency at Various Temperatures

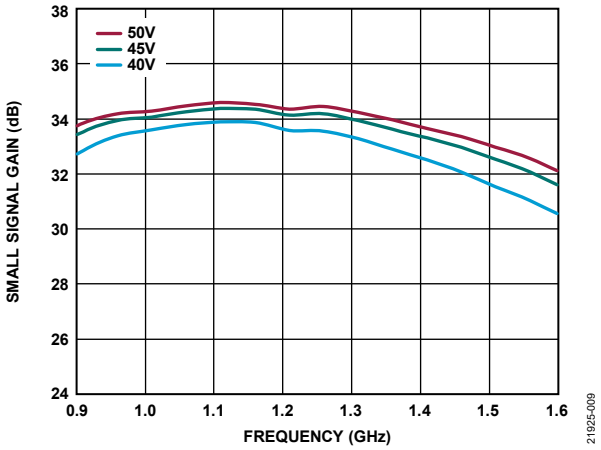


Figure 9. Small Signal Gain vs. Frequency at Various Supply Voltages, $I_{DQ}$ = 400 mA

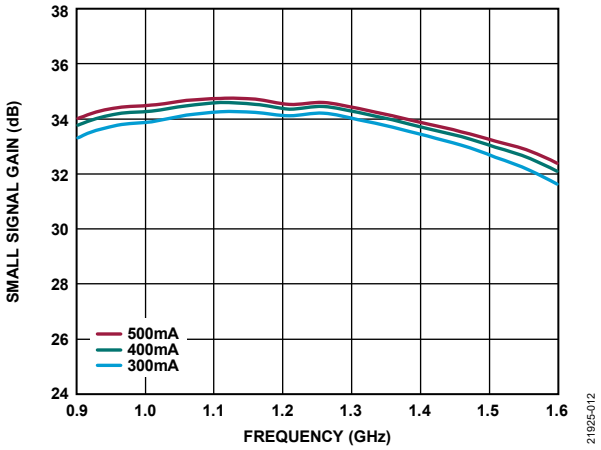


Figure 12. Small Signal Gain vs. Frequency at Various $I_{DQ}$, $V_{DD1}$ and $V_{DD2}$ = 50 V

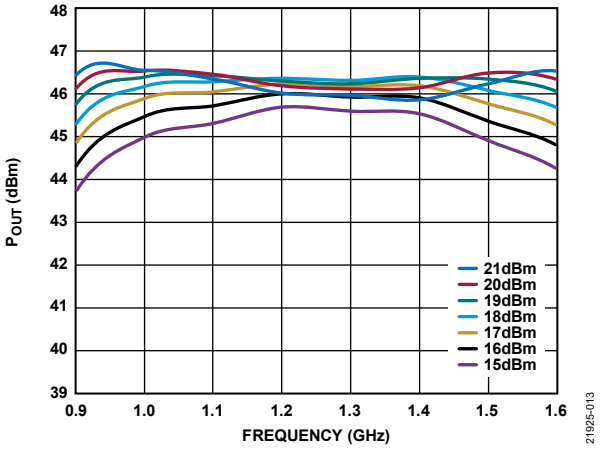


Figure 13. Output Power ($P_{OUT}$) vs. Frequency at Various $P_{IN}$ Levels

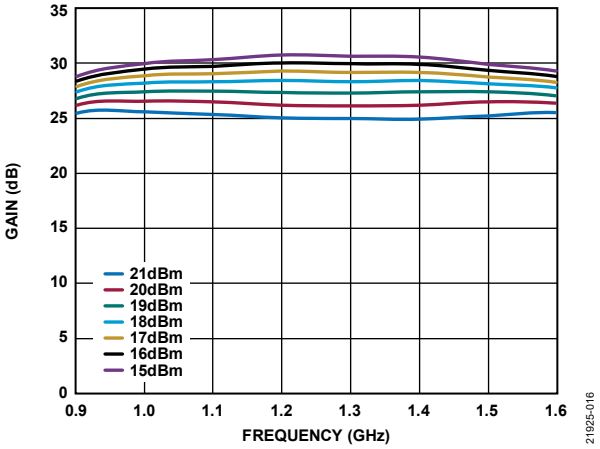


Figure 16. Gain vs. Frequency at Various $P_{IN}$ Levels

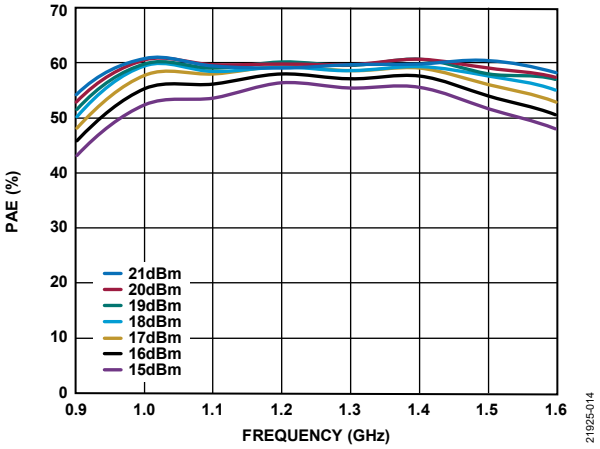


Figure 14. PAE vs. Frequency at Various $P_{IN}$ Levels

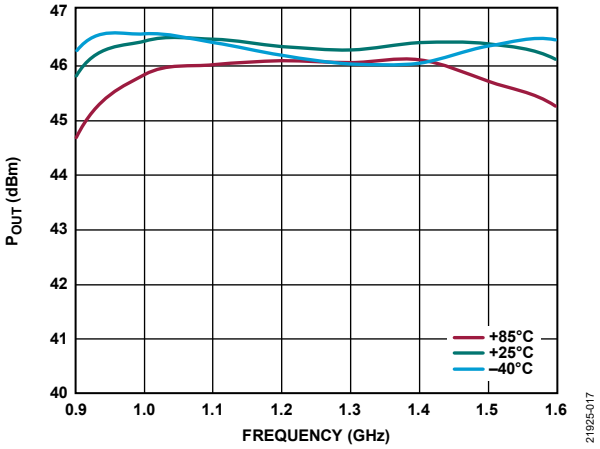


Figure 17. $P_{OUT}$ vs. Frequency at Various Temperatures, $P_{IN}$ = 19 dBm

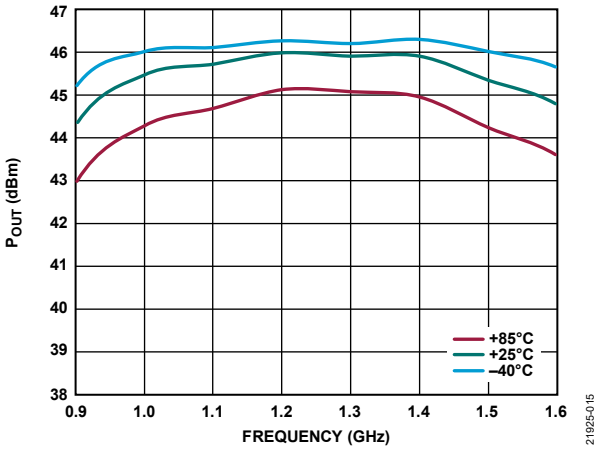


Figure 15. $P_{OUT}$ vs. Frequency at Various Temperatures, $P_{IN}$ = 16 dBm

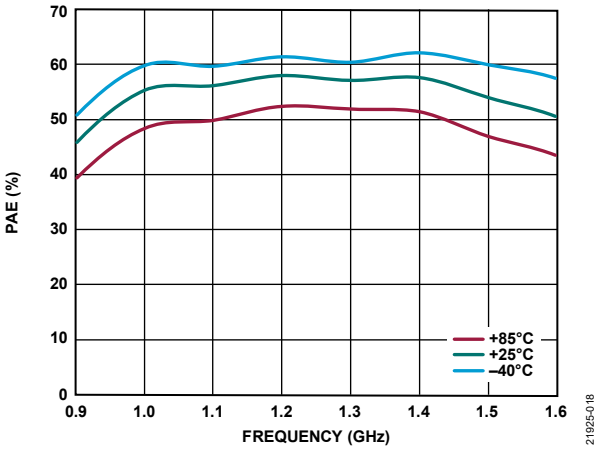


Figure 18. PAE vs. Frequency at Various Temperatures, $P_{IN}$ = 16 dBm

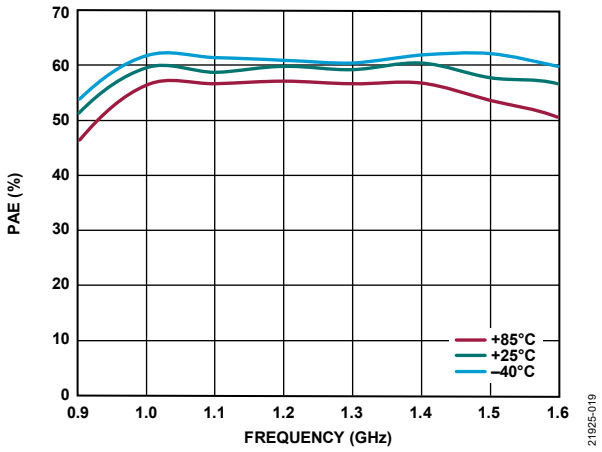


Figure 19. PAE vs. Frequency at Various Temperatures, $P_{IN}$ = 19 dBm

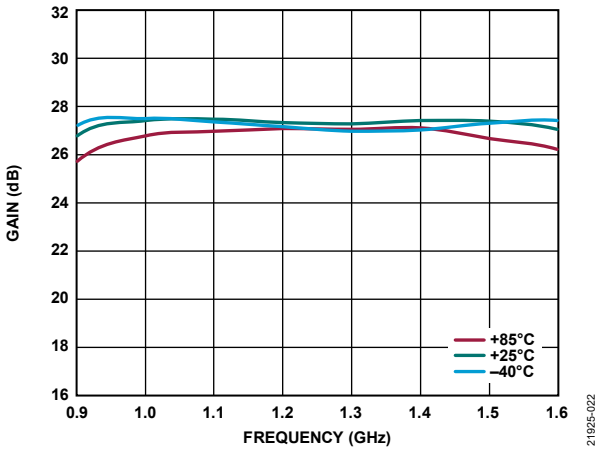


Figure 22. Gain vs. Frequency at Various Temperatures, $P_{IN}$ = 19 dBm

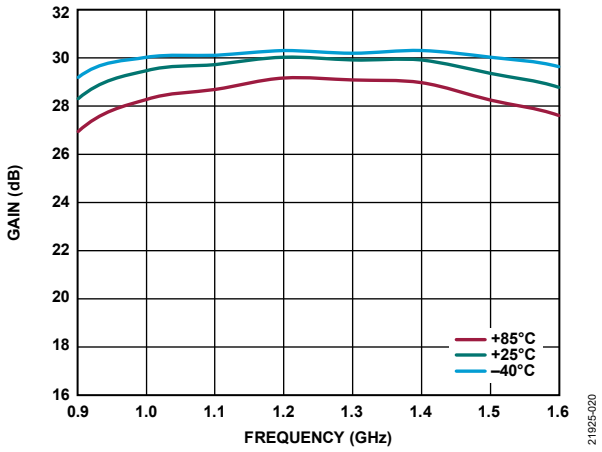


Figure 20. Gain vs. Frequency at Various Temperatures, $P_{IN}$ = 16 dBm

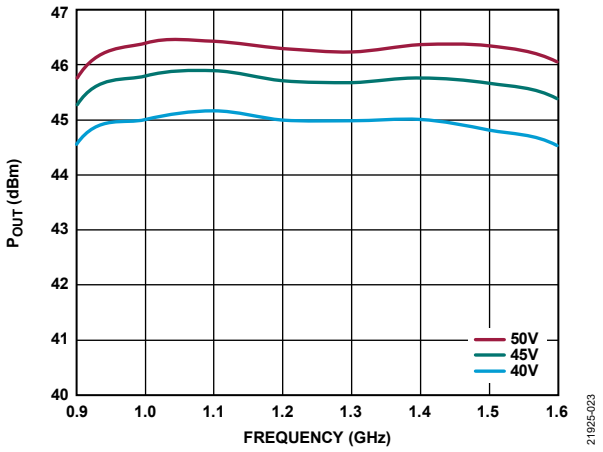


Figure 23. $P_{OUT}$ vs. Frequency at Various Supply Voltages, $P_{IN}$ = 19 dBm, $I_{DQ}$ = 400 mA

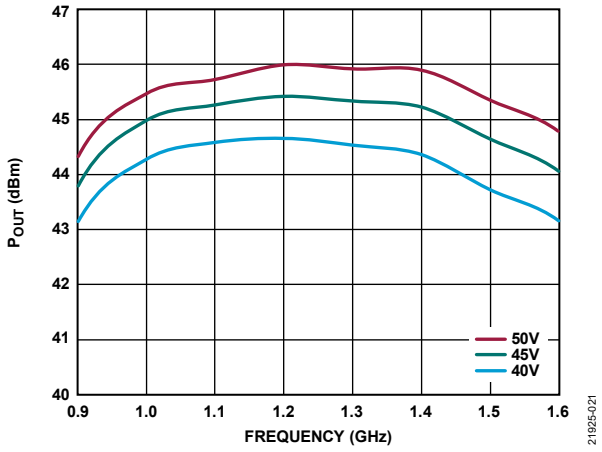


Figure 21. $P_{OUT}$ vs. Frequency at Various Supply Voltages, $P_{IN}$ = 16 dBm, $I_{DQ}$ = 400 mA

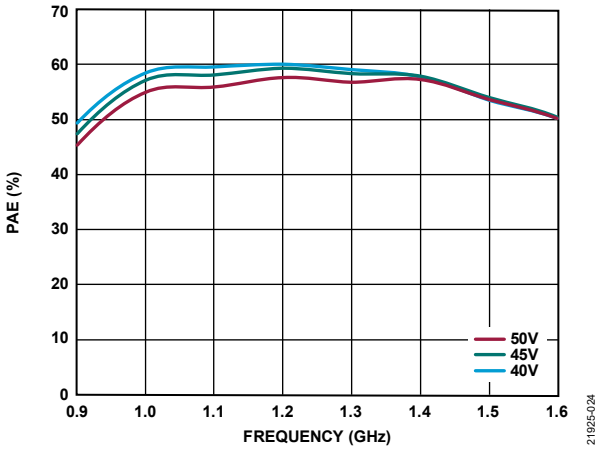


Figure 24. PAE vs. Frequency at Various Supply Voltages, $P_{IN}$ = 16 dBm, $I_{DQ}$ = 400 mA

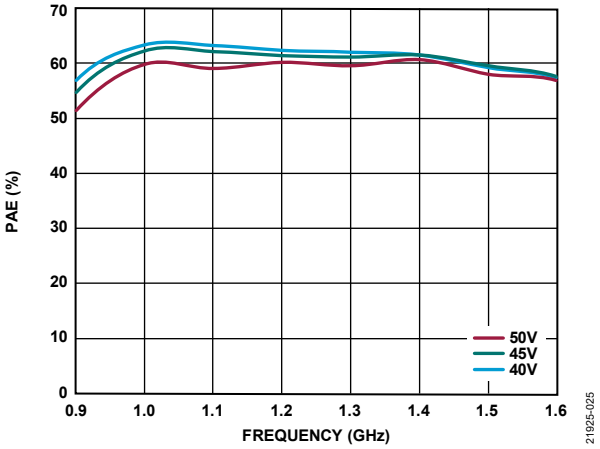


Figure 25. PAE vs. Frequency at Various Supply Voltages, $P_{IN}$ = 19 dBm, $I_{DQ}$ = 400 mA

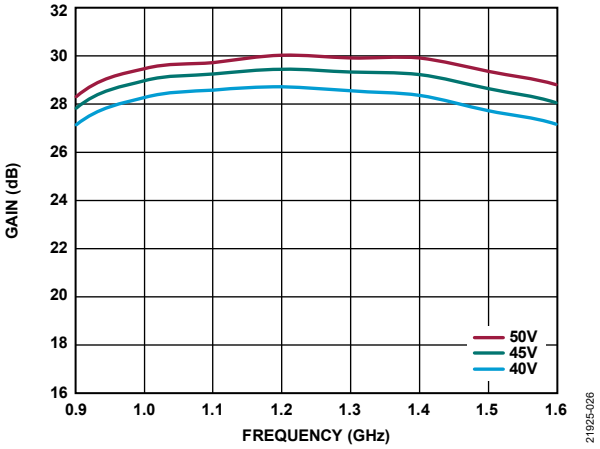


Figure 26. Gain vs. Frequency at Various Supply Voltages, $P_{IN}$ = 16 dBm, $I_{DQ}$ = 400 mA

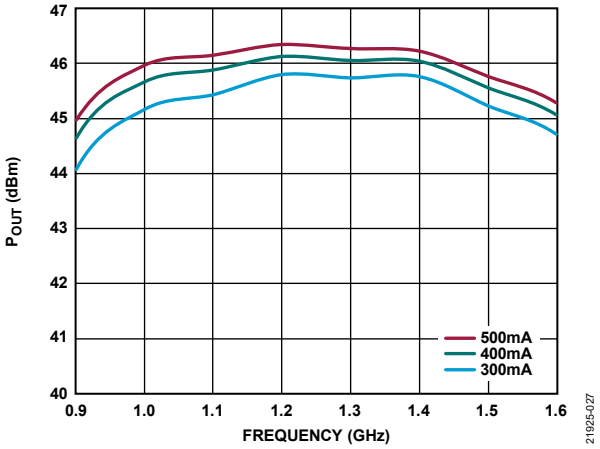


Figure 27. $P_{OUT}$ vs. Frequency at Various $I_{DQ}$ Supply Currents, $P_{IN}$ = 16 dBm, $V_{DD}$ = 50 V

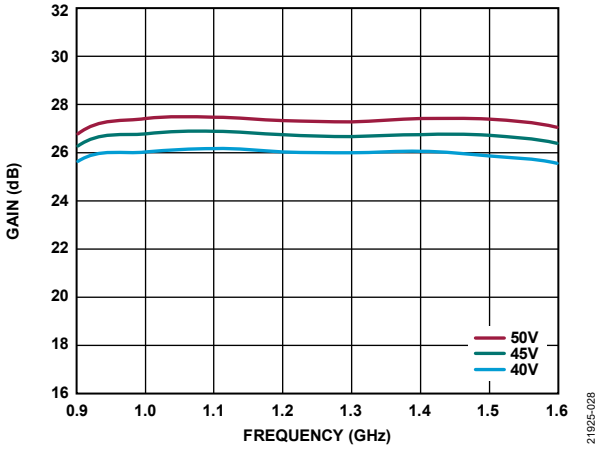


Figure 28. Gain vs. Frequency at Various Supply Voltages, $P_{IN}$ = 19 dBm, $I_{DQ}$ = 400 mA

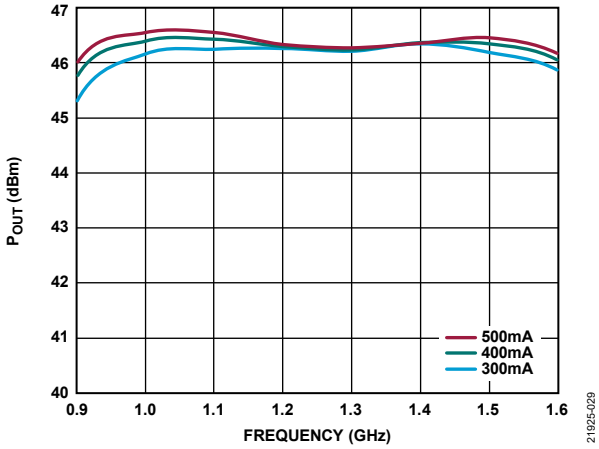


Figure 29. $P_{OUT}$ vs. Frequency at Various $I_{DQ}$ Supply Currents, $P_{IN}$ = 19 dBm, $V_{DD}$ = 50 V

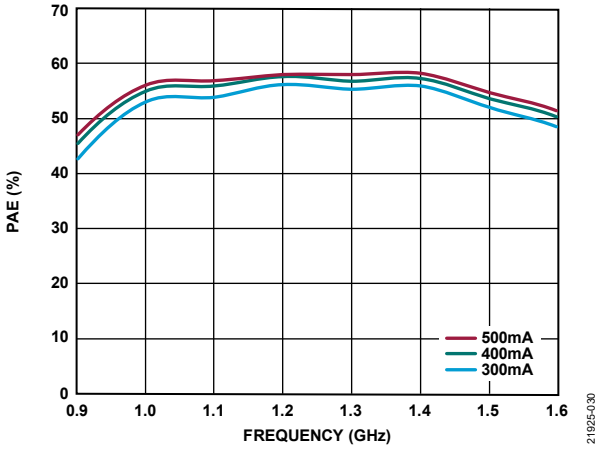


Figure 30. PAE vs. Frequency at Various $I_{DQ}$ Supply Currents, $P_{IN}$ = 16 dBm, $V_{DD}$ = 50 V

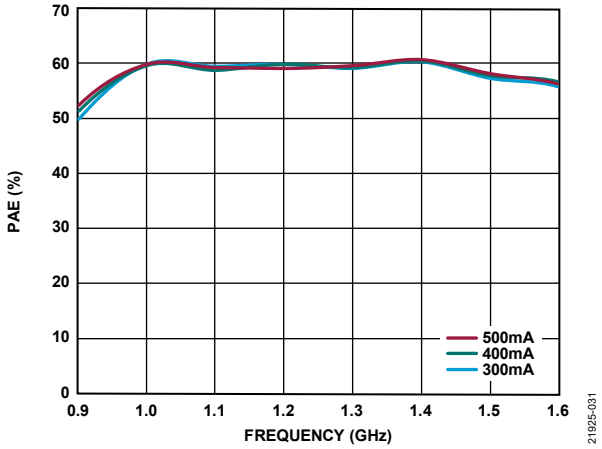


Figure 31. PAE vs. Frequency at Various $I_{DQ}$ Supply Currents, $P_{IN}$ = 19 dBm, $V_{DD}$ = 50 V

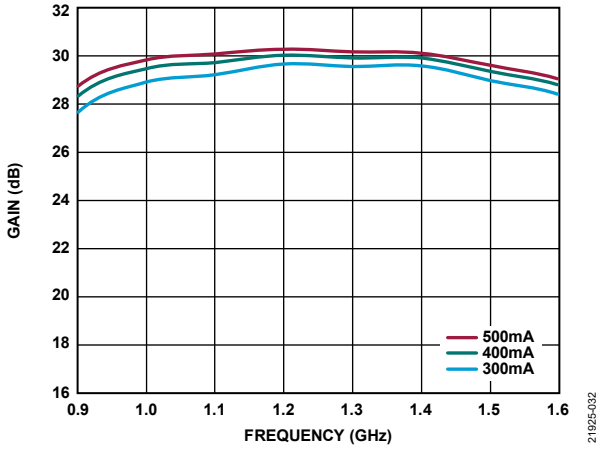


Figure 32. Gain vs. Frequency at Various $I_{DQ}$ Supply Currents, $P_{IN}$ = 16 dBm, $V_{DD}$ = 50 V

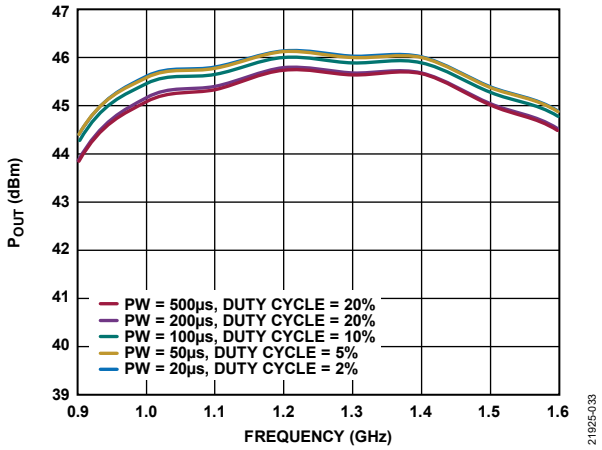


Figure 33. $P_{OUT}$ vs. Frequency at Various Pulse Widths (PW) and Duty Cycles, $P_{IN}$ = 16 dBm

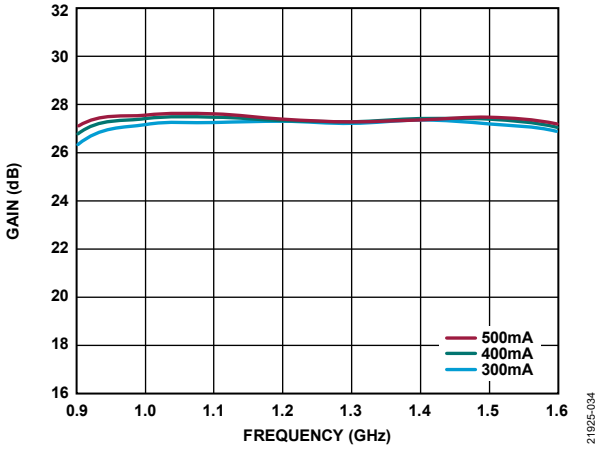


Figure 34. Gain vs. Frequency at Various $I_{DQ}$ Currents, $P_{IN}$ = 19 dBm

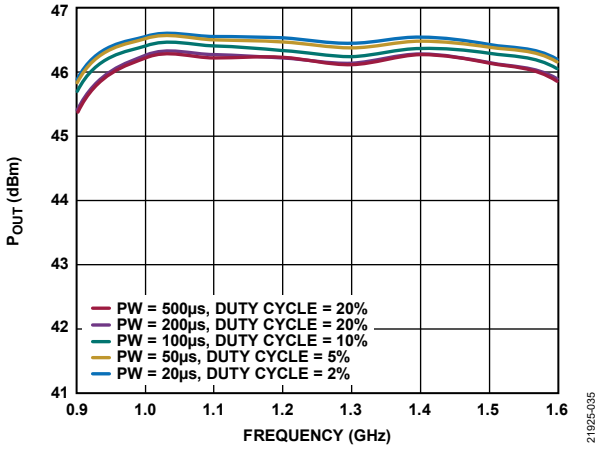


Figure 35. $P_{OUT}$ vs. Frequency at Various Pulse Widths and Duty Cycles, $P_{IN}$ = 19 dBm

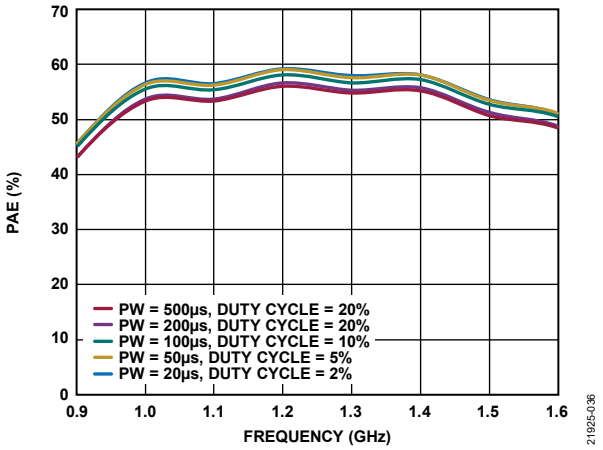


Figure 36. PAE vs. Frequency at Various Pulse Widths and Duty Cycles, $P_{IN}$ = 16 dBm

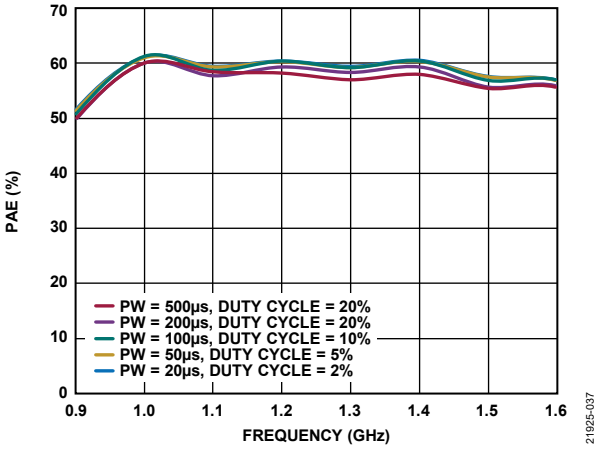


Figure 37. PAE vs. Frequency at Various Pulse Widths and Duty Cycles, $P_{IN}$ = 19 dBm

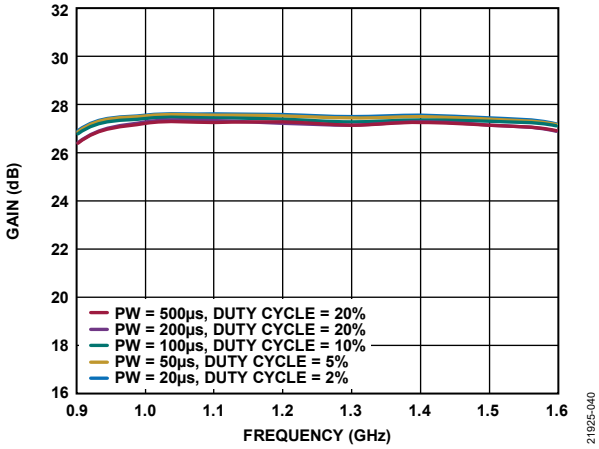


Figure 40. Gain vs. Frequency at Various Pulse Widths and Duty Cycles, $P_{IN}$ = 19 dBm

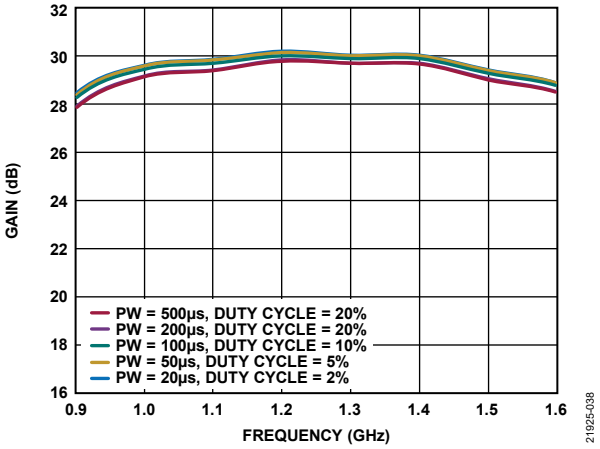


Figure 38. Gain vs. Frequency at Various Pulse Widths and Duty Cycles, $P_{IN}$ = 16 dBm

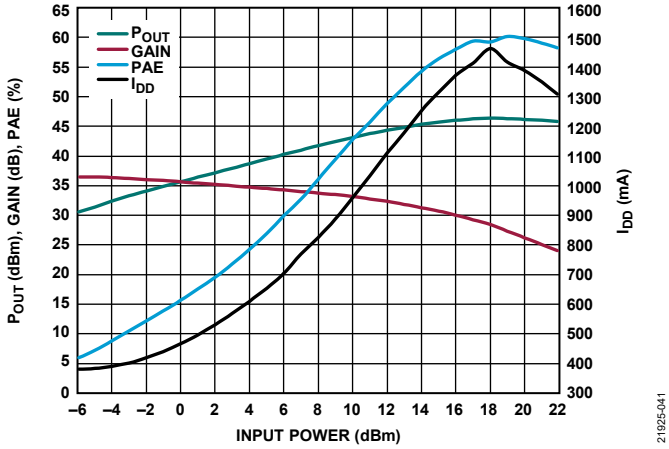


Figure 41. $P_{OUT}$, Gain, PAE, and $I_{DD}$ vs. Input Power at 1.2 GHz

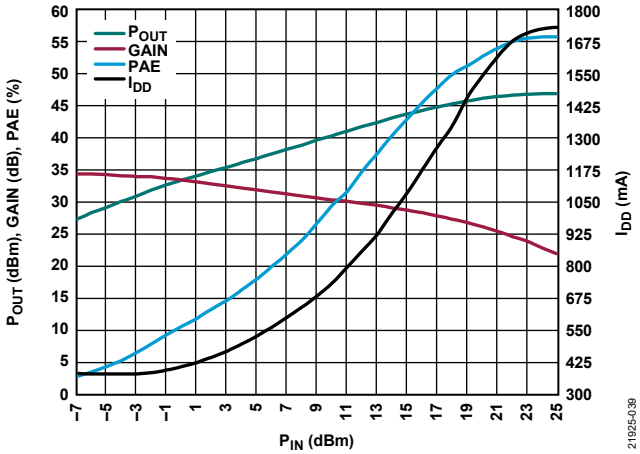


Figure 39. $P_{OUT}$, Gain, PAE, and Supply Current ($I_{DD}$) vs. $P_{IN}$ at 0.9 GHz

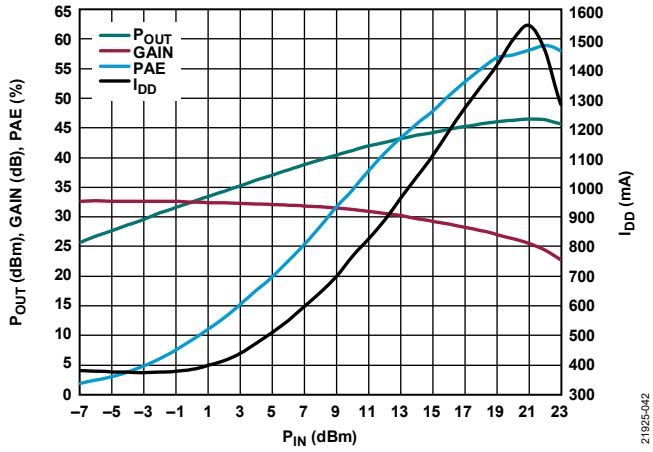


Figure 42. $P_{OUT}$, Gain, PAE, and $I_{DD}$ vs. $P_{IN}$ at 1.6 GHz

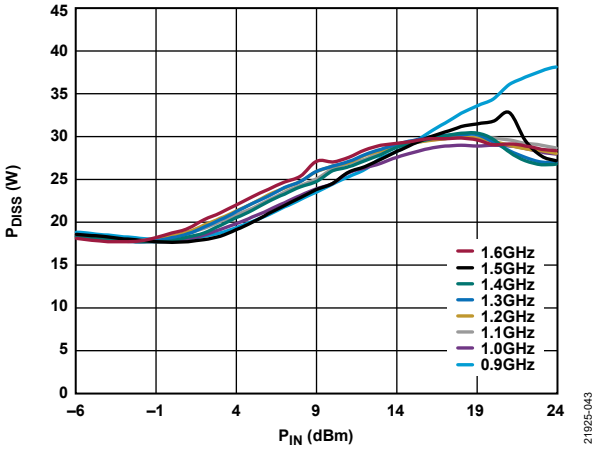


Figure 43. $P_{DISS}$ vs. $P_{IN}$, Drain Bias Pulse Width = 100 µs at 10% Duty Cycle, $T_{BASE}$ = 85°C

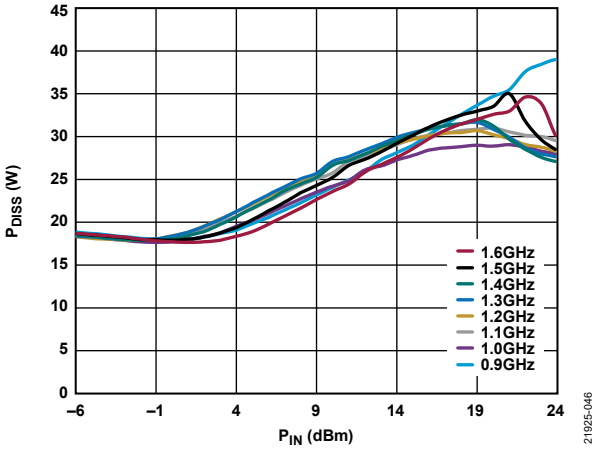


Figure 46. $P_{DISS}$ vs. $P_{IN}$, Drain Bias Pulse Width = 200 µs at 20% Duty Cycle, $T_{BASE}$ = 85°C

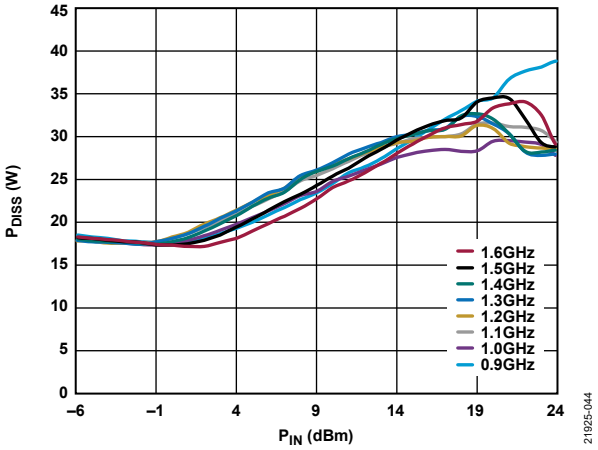


Figure 44. $P_{DISS}$ vs. $P_{IN}$, Drain Bias Pulse Width = 20 µs at 2% Duty Cycle, $T_{BASE}$ = 85°C

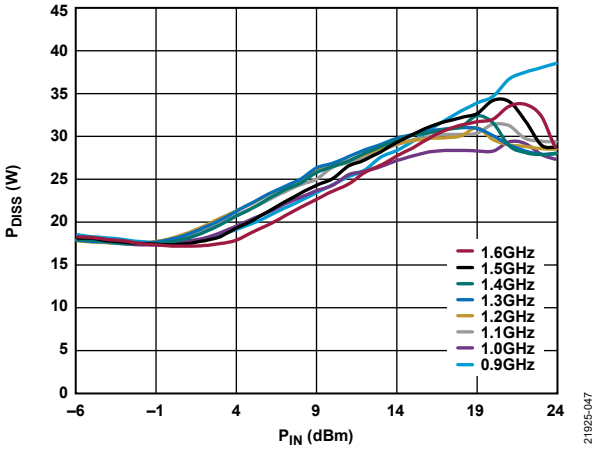


Figure 47. $P_{DISS}$ vs. $P_{IN}$, Drain Bias Pulse Width = 50 µs at 5% Duty Cycle, $T_{BASE}$ = 85°C

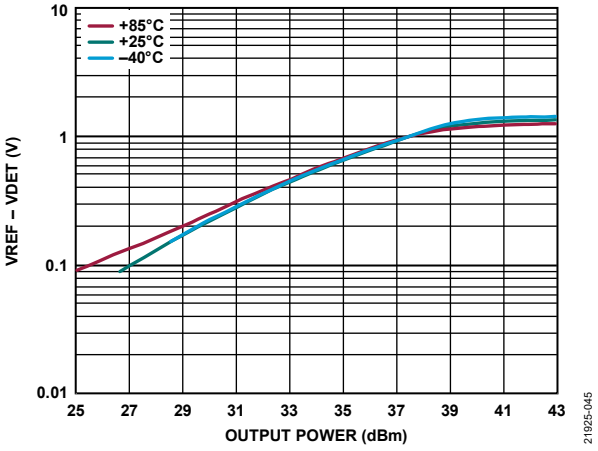


Figure 45. Detector Voltage (VREF – VDET) vs. Output Power for Various Temperatures at 1.2 GHz

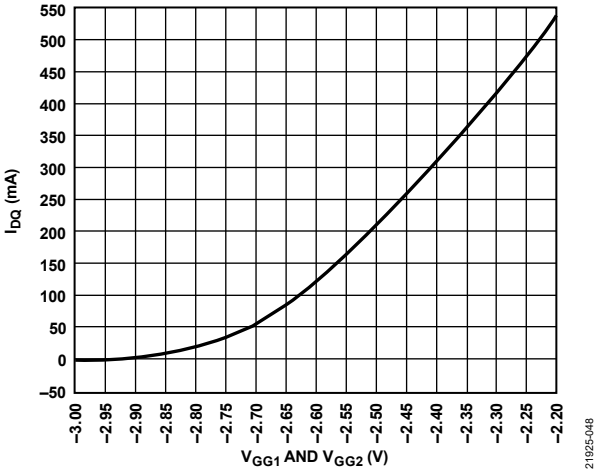


Figure 48. $I_{DQ}$ vs. $V_{GG1}$ and $V_{GG2}$, $V_{DD1}$ and $V_{DD2}$ = 50 V, Representative of a Typical Device

# THEORY OF OPERATION

The ADPA1105 is a GaN power amplifier that delivers 46 dBm (40 W) of pulsed power. The device consists of two cascaded gain stages. A simplified view of this architecture is shown in the basic block diagram in Figure 49.

The ADPA1105 has single-ended RFIN and RFOUT ports that are dc blocked. The impedances of these ports are nominally 50 Ω over the 0.9 GHz to 1.6 GHz operating frequency range. Consequently, the ADPA1105 can be directly inserted into a 50 Ω system without the need for external impedance matching components or ac coupling capacitors.

The pulsed bias voltages applied to the $V_{DD1}$ and $V_{DD2}$ pins bias the drains of the first and second gain stages, respectively (a single common supply voltage must be used). The negative dc voltages applied to the $V_{GG1}$ and $V_{GG2}$ pins bias the gates of the first and second gain stages, respectively, to allow control of the drain currents for each stage (a single common gate voltage must be used).

The recommended dc biasing results in a typical pulsed RF output power and PAE of 46 dBm and 60%, respectively, at 1.5 GHz when the input power is 19 dBm.

A portion of the RF output signal is directionally coupled to a diode to detect the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at the VDET pin. A symmetrical diode circuit that is not coupled to the RF output, which contains a dc voltage output at the VREF pin, is referenced to accomplish temperature compensation. The difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output.

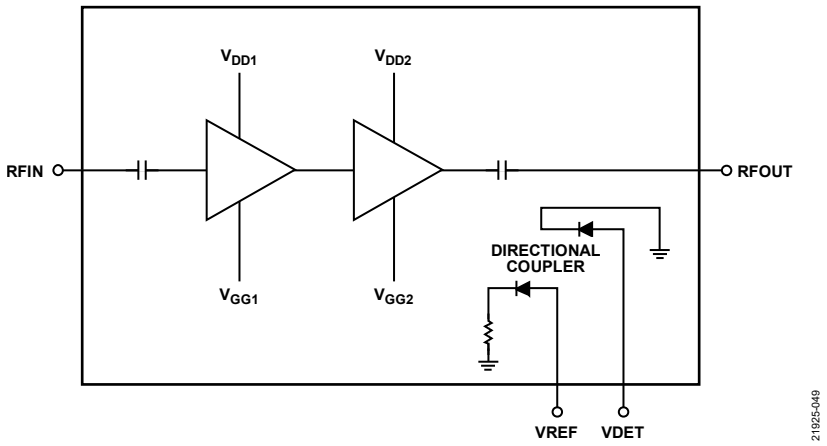


*Figure 49. Basic Block Diagram*

# APPLICATIONS INFORMATION

## BASIC CONNECTIONS

The basic connections for operating the ADPA1105 are shown in Figure 50. Apply a power supply voltage between 20 V and 50 V to the $V_{DD1}$ and $V_{DD2}$ pins. Decouple each pin with the capacitor values shown in Figure 50. Place 3.9 Ω resistors in series with the two 1000 pF power supply decoupling capacitors connected to Pin 28 and Pin 31 ($V_{DD2}$ and $V_{DD1}$). Tie together the two gate voltage pins, $V_{GG1}$ and $V_{GG2}$, and drive the pins as shown in Figure 50. Pin 2, Pin 3, Pin 7, Pin 12, Pin 13, Pin 18, Pin 22, Pin 23, Pin 26, Pin 27, Pin 29, and Pin 30 are designated as no connect (NC) pins. Although these pins are not internally connected, the pins were all connected to ground during the characterization of the device and provide some additional thermal relief.

The decoupling capacitors on the $V_{DD1}$, $V_{DD2}$, $V_{GG1}$, and $V_{GG2}$ lines represent the configuration that was used to characterize and qualify the ADPA1105. The user can reduce the number of capacitors, but the result varies from system to system. General guidance is to first remove or combine the largest capacitors that are farthest from the device.

External bias is provided to the on-chip RF detection circuit via two 715 Ω resistors that are pulled up to 5 V, which results in a current draw of approximately 12 mA. An operation amplifier configured as a differential amplifier can be used to subtract VDET from VREF to yield a temperature compensated voltage that is proportional to the RF output power.

Apply a voltage between 0 V and −4 V to the $V_{GG1}$ and $V_{GG2}$ lines to set the bias level and drain current. Because the ADPA1105 cannot support continuous operation, the device must be operated in pulsed mode by pulsing either the gate voltage or the drain voltage.

In gate pulsed mode, $V_{DD}$ is held at a fixed level (nominally +50 V) while the gate voltage is pulsed between −4 V (off) and approximately −2.3 V (on). The exact on level can be adjusted to achieve the desired quiescent drain current.

In drain pulsed mode, the $V_{DD}$ voltage is pulsed on and off while the gate voltage is held at a fixed negative level between 0 V and −4 V. Because high currents and voltages are being switched on and off, a metal-oxide semiconductor field effect transistor (MOSFET) and a MOSFET switch driver are required in the circuit. Large capacitors are also required, which act as local reservoirs of charge and help provide the drain current required by the ADPA1105 while maintaining a steady drain voltage during the on time of the pulse.

The ADPA1105-EVALZ evaluation board package includes a plugin pulser board that contains the required circuitry to implement drain pulsed mode. See the ADPA1105-EVALZ for more information.

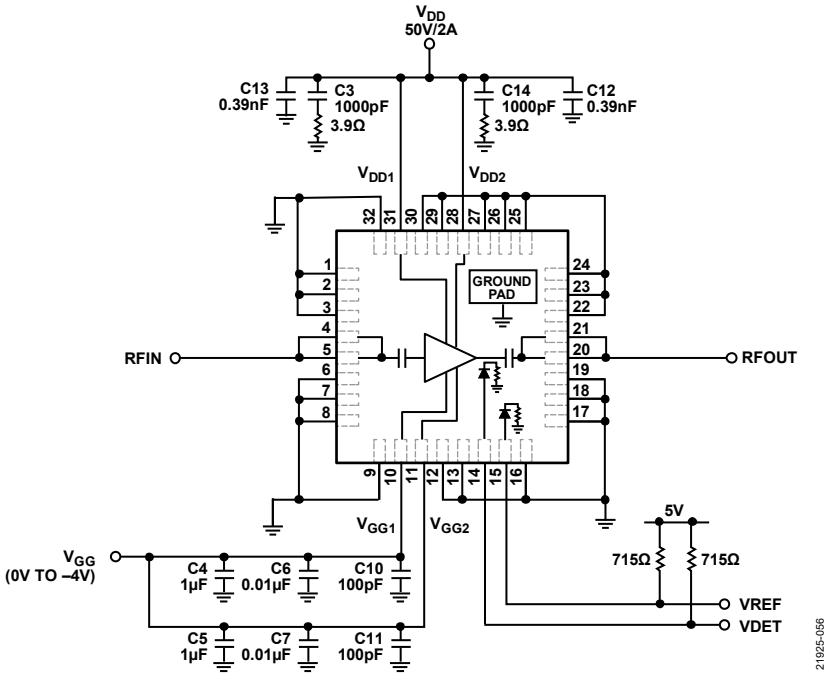


*Figure 50. Basic Connection*

## THERMAL MANAGEMENT

Proper thermal management is critical to achieve the specified performance and rated operating life. Pulsed biasing is required to limit the average power dissipated and maintain a safe channel temperature. The channel (or die) temperature correlates closely with the mean time to failure.

Consider a continuous bias case (see Figure 51). When bias is applied, the channel temperature ($T_{CHAN}$) of the device rises through a turn on transient interval and eventually settles to a steady state value. Calculate the $\theta_{JC}$ thermal resistance of the device as the rise in $T_{CHAN}$ above the starting $T_{BASE}$ divided by the total device $P_{DISS}$ with the following equation:

$$\theta_{JC} = t_{RISE}/P_{DISS} \quad (1)$$

where:

$t_{RISE}$ is the peak rise in the $T_{CHAN}$ of the device above the $T_{BASE}$ (°C).

$P_{DISS}$ is the power dissipation (W) of the device.

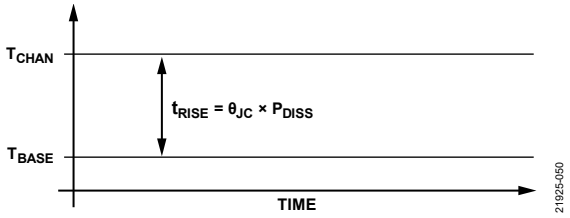


*Figure 51. Continuous Bias*

Next, consider a pulsed bias case at low duty cycle (see Figure 52). When bias is applied, the $T_{CHAN}$ of the device can be described as a series of exponentially rising and decaying pulses. The peak channel temperature reached during consecutive pulses increases during the turn on transient interval, and eventually settles to a steady state condition where peak channel temperatures from pulse to pulse stabilize.

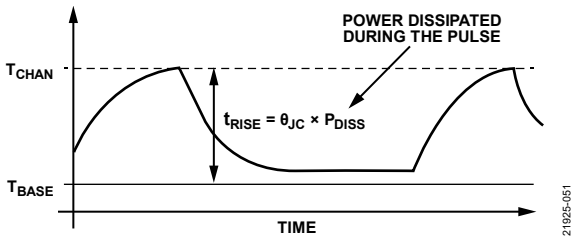


*Figure 52. Pulsed Bias at Low Duty Cycle*

Transient thermal measurements were performed on the ADPA1105 amplifier at several different bias pulse widths and duty cycles to obtain the thermal resistance values listed in Table 7.

**Table 7. Pulse Settings and Thermal Resistance Values**

| Pulse Settings | | |
|---|---|---|
| **Pulse Width (µs)** | **Duty Cycle (%)** | **$\theta_{JC}$ (°C/W)** |
| 100 | 10 | 2.11 |
| 200 | 20 | 2.82 |
| 300 | 30 | 3.54 |

Narrower pulse widths and/or lower duty cycles can result in greater reliability.

The ADPA1105 amplifier is designed for low duty cycle pulsed applications. However, there can be brief periods of time when the device operates (perhaps accidently) under continuous bias conditions. The thermal resistance increases to 6.5°C/W under these conditions. Even at the nominal quiescent bias $V_{DD1}$ and $V_{DD2}$ = 50 V and $I_{DD}$ = 0.4 A), the 20 W power dissipation results in a 130°C channel temperature rise above the base temperature. Use extreme caution in this case to ensure that the device does not exceed the device maximum reliable channel temperature of 200°C.

# OUTLINE DIMENSIONS

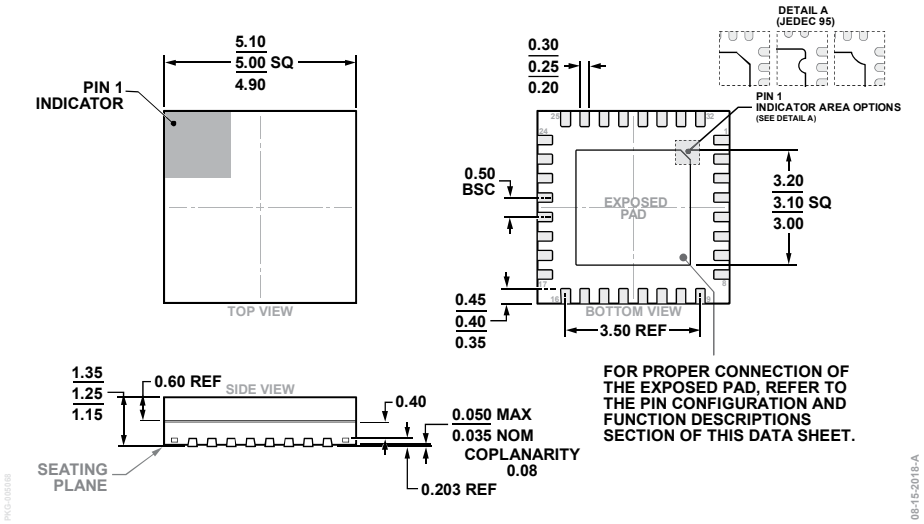


*Figure 53. 32-Lead Lead frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]*
*5 mm × 5 mm Body and 1.25 mm Package Height*
*(CG-32-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2, 3] | Temperature | MSL Rating[4] | Package Description | Package Option |
|---|---|---|---|---|
| ADPA1105ACGZN | −40°C to +85°C | MSL3 | 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV] | CG-32-2 |
| ADPA1105ACGZN-R7 | −40°C to +85°C | MSL3 | 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV] | CG-32-2 |
| ADPA1105-EVALZ | | | Evaluation Board | |

[1] All models are RoHS compliant parts.
[2] The lead finish of the ADPA1105ACGZN and the ADPA1105ACGZN-R7 is nickel palladium gold (NiPdAu).
[3] When ordering the evaluation board, use the reference model number ADPA1105-EVALZ.
[4] See the Absolute Maximum Ratings section for more information.