

INTRODUCTION

This user guide describes the AD9625 evaluation board, AD9625-2.5EBZ, which provides all of the support circuitry required to operate this part in the various modes and configurations. The application software used to interface with the device is also described.

The AD9625 data sheet provides additional information and should be consulted when using the evaluation board. All documents and software tools are available at www.analog.com/hsadcevalboard. For additional information or questions, send an email to highspeed.converters@analog.com.

The AD9625 is a 12-bit ADC with sampling speeds of up to 2500 <u>MSPS</u>. It is designed to support wideband applications where high sample rates, small size, wide bandwidth and versatility are desired. The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. This reference design includes the device data capture board via the JESD204B serial interface and the <u>SPI</u> interface. The samples are written to the internal memory on the FPGA capture board. It allows programming the device and monitoring its internal registers via <u>SPI</u>.

FEATURES

- Full featured evaluation board for the AD9625
- SPI interface for setup and control
- Balun input drive option
- On-board LDO regulator needing a single external 12V, 3 A dc supply
- VisualAnalog® and SPI controller software interfaces



Figure 1. AD9625 Evaluation Board Connection— AD9625-2.5EBZ (on Left) and HSC-ADC-EVALEZ (on Right)

REQUIRED HADWARE

- AC to 12V DC power supplies (2)
- Analog signal source, anti-aliasing filter and SMA cable.
- Analog Clock source and SMA cable.
- PC running Windows
- USB 2.0 cable
- AD9625 Evaluation Board
- HSC-ADC-EVALEZ FPGA Based Data Capture Board

DESIGN AND INTEGRATION FILES

- Schematic, mg9625ce04c1_sch.pdf
- Board File, 19625ce04c1-1-24.zip
- BOM, a9625ce04c1_bom-new04222014.xls
- Analog Input S-Parameter Model, analog Input_model.zip

HELPFUL DOCUMENTS

- AD9625 data sheet Shttp://www.analog.com/AD9625
- AD9625 Evaluation Board "Quick Start User Guide", aquickstartguide_ad9625_2p5.docx
- * High Speed ADC Capture Evaluation Kit Rev E (HSC-ADC-EVALEZ) Shttp://wiki.analog.com/resources/eval/hsc-adc-evale
- AN-905 Application Note, VisualAnalog Converter Evaluation Tool Version 1.0 User Manual
- AN-878 Application Note, High Speed ADC SPI Control Software
- NN-877 Application Note, Interfacing to High Speed ADCs via SPI
- N-835 Application Note, Understanding ADC Testing and Evaluation

EASY START Steps

Important Note Administrative rights for the Windows operating systems are needed during the entire software installation procedure. Completion of every step before reverting to a normal user mode is recommended.

1. Download and Install VisualAnalog. For the latest updates to the software, check the Analog Devices website at High Speed ADC Eval Boards.

2. Connect the ADC capture board to the ADC evaluation board. If an adapter is required, insert the adapter between the ADC evaluation board and the ADC capture board.

3. Connect the provided USB cable to the ADC capture board and to an available USB port on the computer.

4. The ADC capture board is supplied with a wall mount switching power supply. Connect the supply end to an ac wall outlet rated for 100 Vac to 240 Vac at 47 Hz to 63 Hz. The other end is terminated with a plug that connects to the PCB at P1301. The supply is fused and conditioned before connecting to the regulators that supply the proper bias to the entire HSC-ADC-EVALEZ capture board.

5. Once the USB cable is connected to both the computer and the HSC-ADC-EVALEZ board, and power is applied, the USB driver starts to install. The Found New Hardware Wizard opens and prompts you through the automated install process.

6. (Optional) Verify in the Windows device manager that Analog Devices HADV6-FMC is listed under the USB hardware.

7. Make sure the evaluation boards are powered on before connecting the analog input and clock. Connect the appropriate analog input (which Downloaded from Arrow company and low jitter clock signal.

eval/ad9625.txt · Last modified: 30 Jan 2015 15:54 by IanB

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