LTC1410
12-Bit, High Speed, 1.25Msps A/D Converter Demo Board

DESCRIPTION

The LTC®1410 is a 650ns, 1.25Msps, sampling 12-bit A/D converter which draws only 160mW from ±5V supplies. The LTC1410 demo board provides the user with a way to evaluate the LTC1410 high speed A/D converter. In addition, the LTC1410 demo board is intended to illustrate the layout and bypassing techniques required to obtain optimum performance from this part. The LTC1410 demo board is designed to be easy to use and requires only ±7V to ±15V supplies, a conversion start signal and an analog input signal (single-ended or differential). As shown in the board photo, the LTC1410 is a very space efficient solution for A/D users. By combining a 12-bit A/D, sample-and-hold, reference and clock circuitry into a single SOIC package, all the data acquisition circuitry including the bypass capacitors can be placed into an area of only 0.5 square inches.

This manual shows how to use the demo board. Included are timing diagrams, power supply requirements and analog input range information. Additionally, a schematic, parts list, drawings and dimensions of all the PC board layers are included. An explanation of the layout and bypass strategies used in this board is also included so that anyone designing a PC board using the LTC1410 will be able to get the maximum performance from the device.

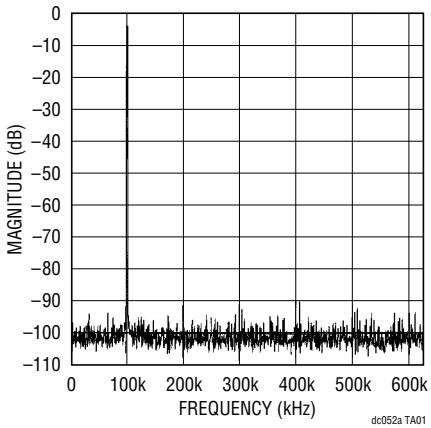
Some key features of this demo board include:

- Proven 1.25Msps 12-bit ADC surface mount layout
- Actual ADC footprint only 0.5 inch^2 including bypass capacitors
- 72dB SINAD and 82dB THD at 600kHz inputs

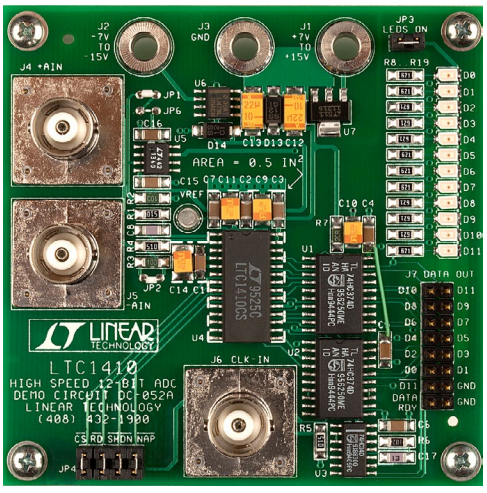
Design files for this circuit board are available at http://www.linear.com/demo

BOARD PHOTO AND TYPICAL PERFORMANCE CHARACTERISTICS

4096 Point FFT of LTC1410 Demo Board



Component Side



OPERATION

OPERATING THE BOARD

Powering the Board

To use the demo board, apply ±7V to ±15V at 200mA to the banana jacks J1 and J2 and 0V (GND) to J3. Be careful to observe the correct polarity. Internal regulators provide ±5V to the LTC1410. An LT1121-5 regulator (U7) provides 5V for analog and digital circuitry while –5V is provided for the A/D and buffer by the MC79L05 regulator (U6).

The Analog Input

The LTC1410 has a unique feature not found on previous ADCs: differential inputs with good common mode rejection from DC to over 10MHz. While this feature is extremely valuable for rejecting noise and measuring differential signals, the board can also be used to evaluate the LTC1410 in single-ended mode (with the "–" input grounded). This board allows evaluation in either mode.

Differential (bipolar) analog signals are applied to the LTC1410 demo board using BNC connectors J4 (noninverting + input) and J5 (inverting – input). The analog signal input range is ±2.5V.

The LTC1410 $+A_{IN}$ (noninverting) and $–A_{IN}$ (inverting) inputs have a common-mode range of V_{SS} to V_{DD}. The full-scale differential between the signals applied to $+A_{IN}$ and $–A_{IN}$ is ±2.5V. For example, when a 1.5V signal is applied to the $–A_{IN}$ input, the negative-to-positive full-scale input range of $+A_{IN}$ is –1V to 4V, corresponding to an output code of 1000 0000 0000 to 0111 1111 1111.

The demo board is delivered with jumpers JP1 and JP2 closed. This configures the board for a ±2.5V input signal centered around ground and applied to J4 ($+A_{IN}$).

The board includes a recommended lowpass filter (R1, R4, and C8) across the differential inputs. With the component values shown, the cutoff frequency (f_S) is:

$$\frac{1}{2\pi(102\Omega)(0.001\mu F)} = 1.56MHz$$

These values can be altered to meet other circuit and input signal requirements. For lower bandwidth input signals, increase C8's value. For undersampling applications that take advantage of the input circuitry's wide bandwidth, decrease the capacitance of C8.

The best way to observe the performance of the LTC1410 is by directly driving it from a low impedance signal source. However, since some applications involve high output impedance sources, the board also has provisions for an onboard LT1360 high speed operational amplifier. The buffer is recommended if the source impedance of the input signal is greater than 930Ω. The LT1360, operating as a noninverting buffer, provides the LTC1410 with a fast settling, low impedance signal that allows the input voltage to fully settle before starting a conversion. The LT1360 demonstrates an example of properly driving the LTC1410. When using the LT1360, open JP1 and close JP2 and JP6.

Optimum performance is achieved using a signal source that has low output impedance, is low noise and has low distortion. Signal generators, such as the B&K Type 1051 Sine Generator, give excellent results. Further, this generator can be configured to operate referenced to a master clock signal, as shown in Figure 1.

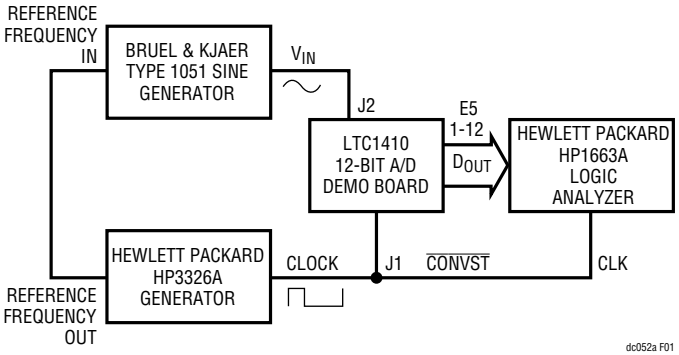


Figure 1. Typical Setup for LTC1410 Demo Board

OPERATION

Applying the Conversion Start Signal

A conversion is initiated by a falling edge on the $\overline{\text{CONVST}}$ input (BNC J6). The $\overline{\text{CONVST}}$ input uses TTL or CMOS levels. As shown in Figure 2, $\overline{\text{CONVST}}$ should remain low until the conversion is completed or returned high within 420ns of the negative going edge (as shown in Figure 3). During a conversion, transitions on the $\overline{\text{CONVST}}$ input can cause errors in the D_{OUT} output.

Reading the Output Data

The ADC data outputs are buffered by the two 74HC374 latches. The latches drive the LEDs and connector J7. In a practical circuit, latches are not required unless the ADC is tied to a noisy data bus. Refer to the LTC1410 data sheet for details on different digital interface modes.

The output data format of the LTC1410 is two's complement. The data can be converted to offset binary by using $\overline{\text{D11}}$ instead of D11. Offset binary is used when an FFT is to be performed on the sampled data. A Data Ready line (J7, Pin 2) is provided to latch the D_{OUT} word. D_{OUT} is valid on the rising edge of Data Ready.

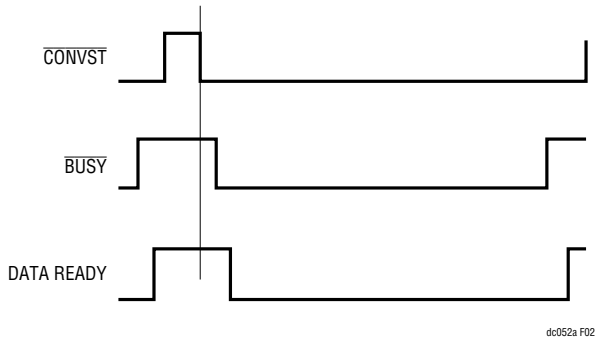


Figure 2. Timing Diagram

The LTC1410 D_{OUT} word can be acquired with a logic analyzer. Conversion data can be stored on a disk and easily transferred to a PC by using a logic analyzer that has a PC compatible floppy drive (such as an HP1663A). Once the data is transferred to a PC, use programs such as MathCAD or Excel to calculate FFTs. Use the FFTs to obtain LTC1410 AC specifications such as signal-to-noise ratio and total harmonic distortion.

LEDs D0 to D11 provide a visual display of the LTC1410 digital output word. D0 and D11 display the logic state of the LSB and MSB, respectively. Remove jumper JP3 to disable the LEDs, reducing supply consumption up to 36mA.

Driving $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{SHDN}}$, and NAP/$\overline{\text{SLP}}$ Pins

Jumpers for $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{SHDN}}$, and NAP/$\overline{\text{SLP}}$ (JP4A to JP4D) are shorted for normal operation. The jumpers can be removed and these lines externally driven if desired. See the LTC1410 data sheet for details on driving these lines.

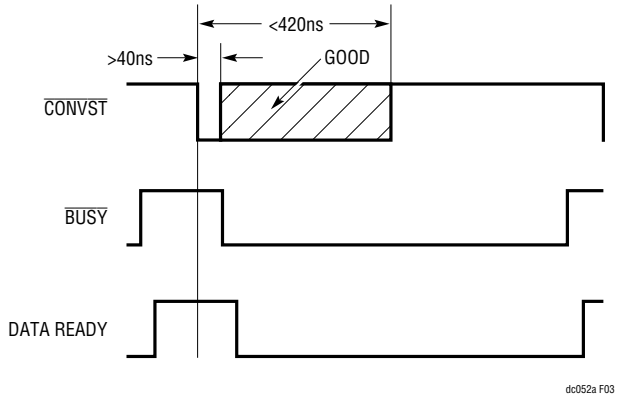


Figure 3. Alternative Timing Diagram

BOARD LAYOUT

A well designed printed circuit board layout incorporating the LTC1410 uses separate analog and digital ground planes. Except for connecting them at the power supply GND input (J3), or at Pin 19 (OGND), completely isolate the ground planes from each other. Additionally, they should not overlap if on different printed circuit board layers. Connecting the LTC1410 analog (AGND) and digital (DGND) pins to the analog ground plane ensures the lowest noise operation.

The demonstration board layout (section titled "PCB Layout and Film") shows the best way to configure and connect the ground planes. To ensure maximum ground plane efficiency, especially for the analog ground plane, it is important to minimize plane-breaking traces.

POWER SUPPLY CONNECTIONS AND BYPASSING

Analog and digital positive supply pins, AV_{DD} and DV_{DD}, respectively, are connected at the device and to the 5V supply with a single trace. The negative supply pin (V_{SS}) is connected to the –5V supply. The best performance is achieved by careful attention to proper bypassing. Bypass AV_{DD} and DV_{DD} together to the analog ground plane with a 10µF low ESR capacitor in parallel with a 0.1µF monolithic ceramic capacitor. Bypass V_{SS} to the analog ground plane with its own 10µF low ESR capacitor in parallel with a 0.1µF monolithic ceramic capacitor.

The internal voltage reference requires two bypass capacitors, a 10µF low ESR capacitor in parallel with a 0.1µF monolithic ceramic capacitor connected between the REFCOMP pin and the analog ground plane. These bypass capacitors are necessary because the LTC1410 internal reference requires a bypass capacitor of at least 1µF for stable operation. Reference noise can be reduced even further by using a 0.1µF monolithic ceramic capacitor connected between the V_{REF} pin and the analog ground plane.

As with all high accuracy, high resolution circuits, the best performance is achieved by minimizing the lead length of the bypass capacitors.

HARDWARE SETUP

Table 1. Functional Description of User Configurable Jumpers

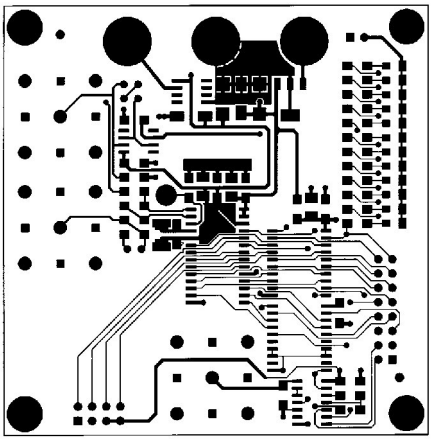
JUMPER	JUMPER NAME	JUMPER CONNECTION
JP1	$+A_{IN}$	Shorted for Single-Ended Unbuffered Operation. Open When Using the Noninverting Input Buffer. See JP6.
JP2	$-A_{IN}$	Shorted for Single-Ended Operation. Open for Differential Input Signals.
JP3	LED Enable	Shorting Enables LED Operation. Opening Disables LED Operation.
JP4A	$\overline{CS}$	Shorted for Normal Operation. Open to Externally Drive the $\overline{CS}$ Pin.
JP4B	$\overline{RD}$	Shorted for Normal Operation. Open to Externally Drive the $\overline{RD}$ Pin.
JP4C	$\overline{SHDN}$	Shorted for Normal Operation. Open to Externally Drive the $\overline{SHDN}$ Pin with a Logic Low for Shutdown Mode or with a Logic High for Normal Operation.
JP4D	NAP/$\overline{SLP}$	Shorted for Normal Operation. Open to Externally Drive the NAP/$\overline{SLP}$ Pin with a Logic Low for Normal Shutdown Operation (All Internal Analog and Digital Circuitry Is Shut Down) or with a Logic High for Fast Wake-Up Shutdown Mode (All Internal Analog and Digital Circuitry Except the Voltage Reference Circuitry Is Shut Down).
JP6	Noninverting Input Buffer Bypass	Open for Normal Operation. Short for Buffered Input Signals and Open JP1.

HARDWARE SETUP

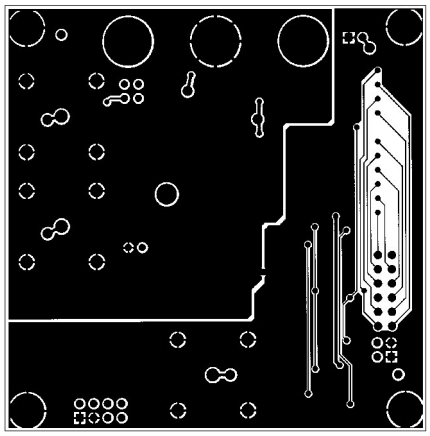
Table 2. Input and Output Pin Functional Description

INPUT/OUTPUT PIN	FUNCTION
J1	Positive Supply Voltage: 7V to 15V at 100mA
J2	Negative Supply Voltage: –7V to –15V at 100mA
J3	Supply Ground
J4	$+A_{IN}$, Noninverting Input: ±2.5V, Referenced to $-A_{IN}$. Input Voltage Range: V_{SS} to AV_{DD} (DV_{DD}).
J5	$-A_{IN}$, Inverting Input: ±2.5V, Referenced to $+A_{IN}$. Input Voltage Range: V_{SS} to AV_{DD} (DV_{DD}).
J6	Convert Start: 0V to 5V
J7-1	Digital Ground
J7-2	RDY Output (End of Conversion)
J7-3	Digital Ground
J7-4	$\overline{D11}$ (MSB)
J7-5	D01
J7-6	D00
J7-7	D03
J7-8	D02
J7-9	D05
J7-10	D04
J7-11	D07
J7-12	D06
J7-13	D09
J7-14	D08
J7-15	D11
J7-16	D10
E1	V_{REF} (2.50V Typical)
E2	DGND (Mounting Hole)
E3	DGND (Mounting Hole)
E4	DGND (Mounting Hole)
E5	DGND (Mounting Hole)

PCB LAYOUT AND FILM

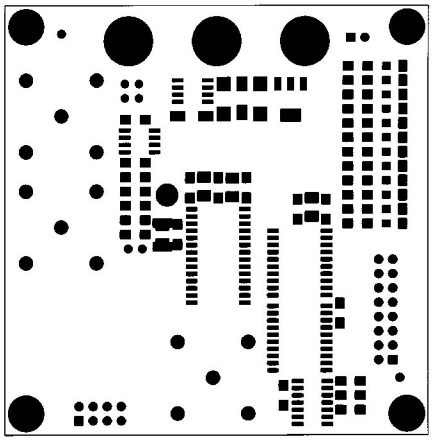


Component Side

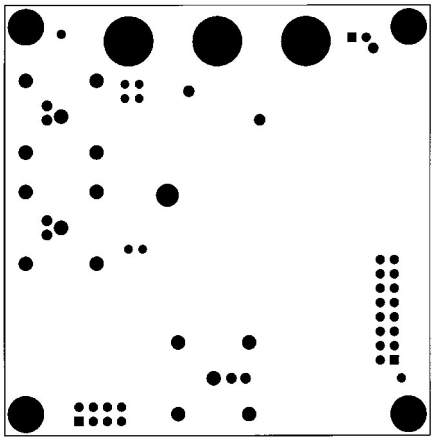


Solder Side

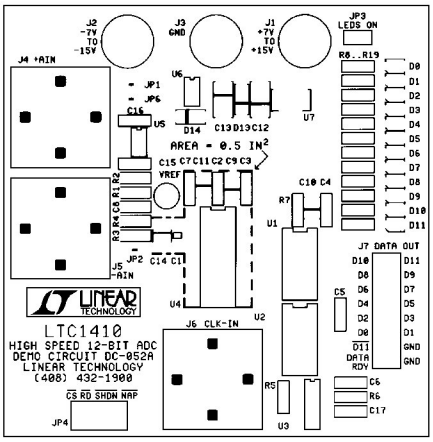
PCB LAYOUT AND FILM



Component Side Solder Mask



Solder Side Solder Mask



Component Side Silkscreen

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	9	C1-C7, C15, C16	CAP., X7R, 0.1µF, 50V, 20%	AVX, 12065C104MAT2A
2	1	C8	CAP., NPO, 0.001µF, 50V, 10%	AVX, 12065A102KAT2A
3	4	C9-C11, C14	CAP., TANTALUM, 10µF, 10V, 20%	AVX, TAJB106M010R
4	2	C12, C13	CAP., TANTALUM, 22µF, 10V, 20%	AVX, TAJC226M010R
5	1	C17	CAP., X7R, 15pF, 50V, 20%	AVX, 12065C102MAT2A
6	12	D0-D11	LED, SMT RED, 2.1V, 45mW	PANASONIC, LN1251C
7	2	D13, D14	DIODE, SCHOTTKY, SS12, 20V, 1A	GENERAL INS., SS12
8	1	E1	TERMINAL, TURRET, 0.094	KEYSTONE, 1502-02
9	4	E2-E5	STDOFF, NYLON F/F, #4-40, 1/2"	MICRO PLASTIC, HTSP-3
10	4		SCREW, #4-40, 3/8", PAN HD PHILL	ANY
11	3	JP1, JP2, JP6	JUMPER LINK, INSULATED, 0.1"	SAMTEC, JL-100-25-T
12	1	J3	JUMPER, 2-PIN, 0.100", 0.025 SQR	SAMTEC, TSW-102-07-G-S
13	5		SHUNT, 0.100"	SAMTEC, SNT-100-BK-T
14	1	JP4	HEADER, 8-PIN, 0.100", 2-ROW	SAMTEC, TSW-104-07-G-D
15	3	J1-J3	JACK, BANANA, 0.175-ID, LOW PROFILE	KEYSTONE, 575-4
16	3	J4-J6	CON., PC-MNT, BNC, VERT	AMP, 227699-3
17	1	J7	HEADER, 16-PIN, 0.100", 2-ROW	SAMTEC, TSW-108-07-G-D
18	3	R1, R4, R5	RES., SMD-1206, 51, 1/8W, 5%	AVX, CR32-510J-T
19	2	R2, R3	RES., SMD-1206, 10k, 1/8W, 5%	AVX, CR32-103J-T
20	1	R6	RES., SMD-1206, 1k, 1/8W, 5%	AVX, CR32-102J-T
21	1	R7	RES., SMD-1206, 20, 1/8W, 5%	AVX, CR32-200J-T
22	12	R8-R19	RES., SMD-1206, 620, 1/8W, 5%	AVX, CR32-621J-T
23	2	U1, U2	I.C., SOIC-WIDE, HC374, OCTAL, D-F/F	MOTOROLA, MC74HC374DV
24	1	U3	I.C., SOIC., 74HC14, HEX INVERTER	MOTOROLA, MC74HC14AD
25	1	U4	I.C., SOIC-0.300, LTC1410, 12-BIT, ADC	LINEAR TECHNOLOGY, LTC1410CS
26	1	U5	I.C., SO-8, LT1360, HI-SPEED OP AMP	LINEAR TECHNOLOGY, LT1360CS8
27	1	U6	I.C., SO-8, 79L05, NEG 5V REG	MOTOROLA, MC79L05ACD
28	1	U7	I.C., SOT-223, LT1121, POS 5V REG	LINEAR TECHNOLOGY, LT1121CST-5

SCHEMATIC DIAGRAM

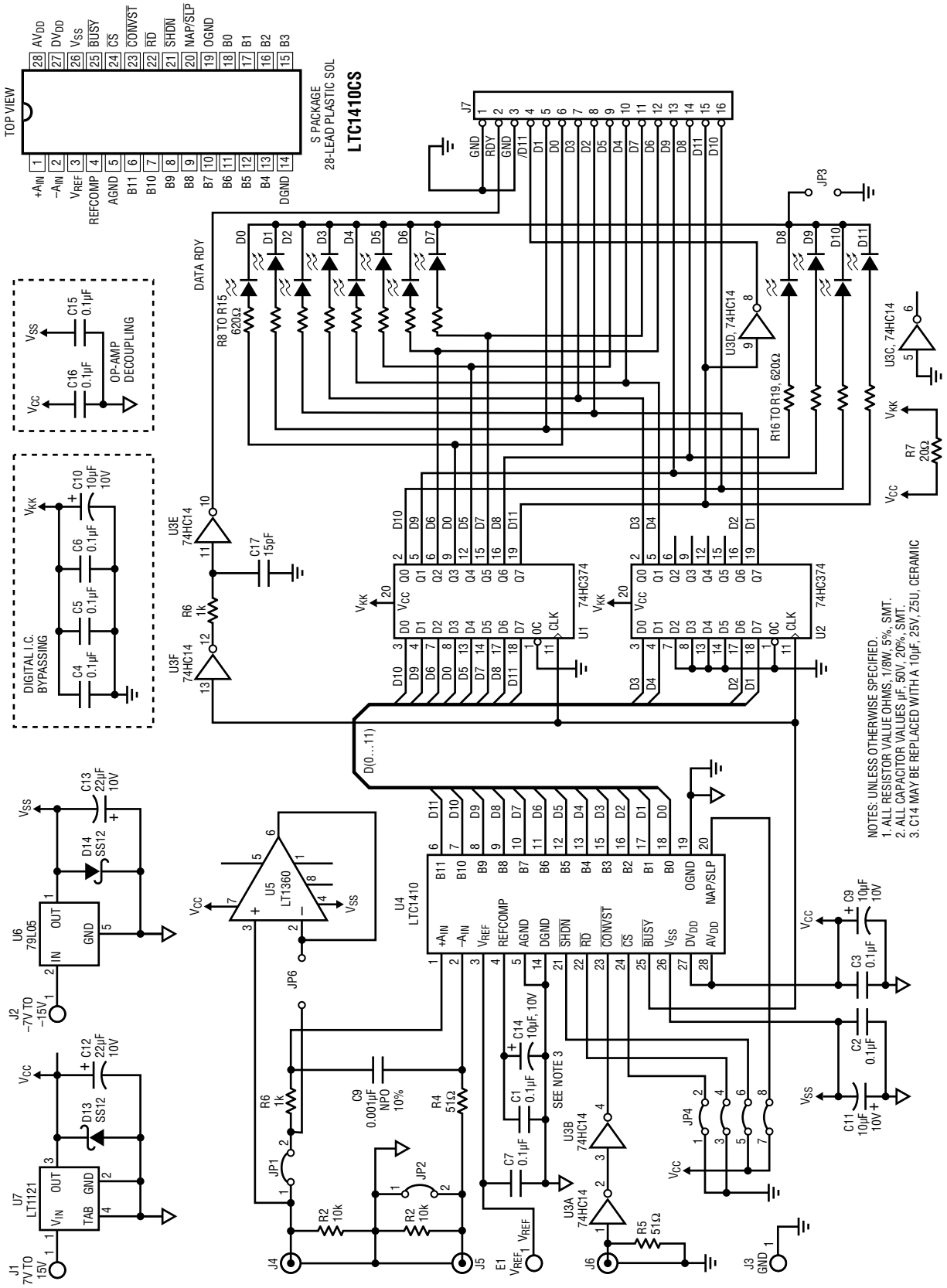
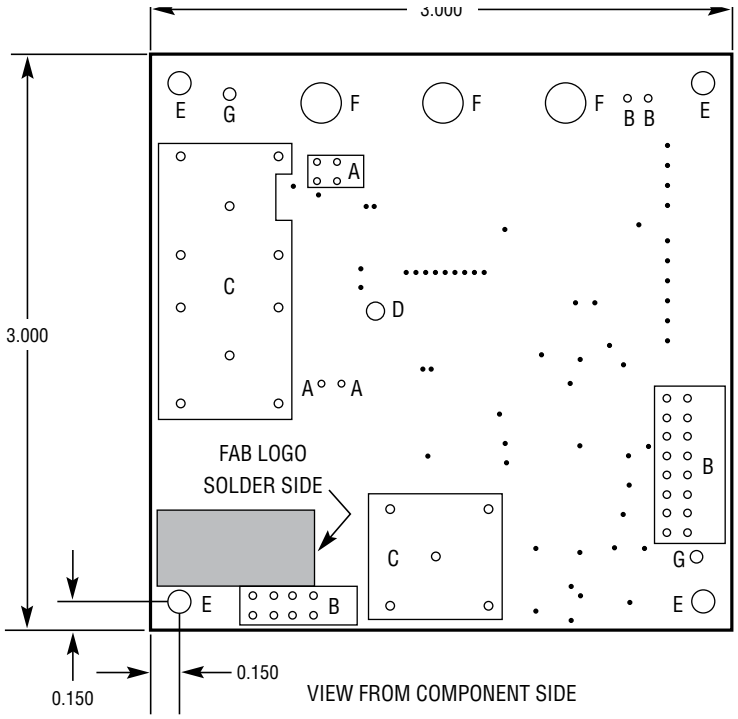


Figure 4. LTC1410 Demonstration Board Features Analog Input Signal Buffer, 1.25 Msps, Parallel Data Output 12-Bit ADC, Data Latches and LED Binary Data Display. Latched Conversion Data Is Available on the 16-Pin Header, J7.

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED.
1. FINISHED MATERIAL IS FR4, 0.062" THICK, 2-OZ COPPER.
2. PCB WILL BE DOUBLE-SIDED WITH PLATED THROUGH HOLES.
3. PTH SIZES AFTER PLATING, 0.001" MIN WALL THICKNESS.
4. USE PADMASTER PROCESS.
5. SOLDER MASK BOTH SIDES USING LIQUID PHOTO-IMAGEABLE (GREEN).
6. SILKSCREEN COMPONENT SIDE USING WHITE NONCONDUCTIVE INK.
7. ALL DIMENSIONS IN INCHES, 0.005".
8. ALL HOLE SIZES AFTER PLATING, 0.003"/–0".

HOLE CHART

SYMBOL	DIAMETER	COMMENT	NUMBER OF HOLES	PLT
NONE	0.020		56	YES
A	0.035		6	YES
B	0.039		26	YES
C	0.045		15	YES
D	0.094		1	YES
E	0.120		4	YES
F	0.210		3	YES
G	0.065	+0/–.002	2	NO
		TOTAL HOLES	113	

dc052a F05

Figure 5. PC Fab View From the Component Side

DEMONSTRATION BOARD IMPORTANT NOTICE

Linear Technology Corporation (LTC) provides the enclosed product(s) under the following **AS IS** conditions:

This demonstration board (DEMO BOARD) kit being sold or provided by Linear Technology is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not provided by LTC for commercial use. As such, the DEMO BOARD herein may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including but not limited to product safety measures typically found in finished commercial goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may or may not meet the technical requirements of the directive, or other regulations.

If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

No License is granted under any patent right or other intellectual property whatsoever. **LTC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind.**

LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035