

## Evaluating the HMC8362/HMC8364 Low Noise Quadband Voltage Controlled Oscillators (VCOs)

### FEATURES

Self contained board, including **HMC8362** or **HMC8364** low noise quadband VCO, **ADG1604** 4:1 multiplexer, filtering options, and **LT3042** voltage regulator and header connectivity to allow use of **Arduino Uno** or **Linduino** microcontroller

Externally powered by a single 6 V supply

### EVALUATION KIT CONTENTS

EV1HMC8362LP6G or EV1HMC8364LP6G evaluation board

### EQUIPMENT NEEDED

Power supply (6 V)

Power supply (low noise, variable 0 V to 13.5 V)

50 Ω terminations

Signal source analyzer

### ONLINE RESOURCES

[HMC8362](#) data sheet

[HMC8364](#) data sheet

[Linduino DC2026C Demo Manual](#)

### GENERAL DESCRIPTION

The EV1HMC8362LP6G and EV1HMC8364LP6G allow the evaluation of the performance of the HMC8362 and HMC8364 low noise quadband voltage controlled oscillators (VCOs). A photograph of the evaluation board is shown in Figure 1. The evaluation board contains the **HMC8362** or **HMC8364** VCO, an **LT3042** ultralow noise voltage regulator, a jumper, an **ADG1604** 4:1 multiplexer, and subminiature Version A (SMA) and 2.92 mm K connectors.

Consult the **HMC8362** and **HMC8364** data sheets in conjunction with this user guide when working with the evaluation boards.

### EV1HMC8362LP6G/EV1HMC8364LP6G EVALUATION BOARD PHOTOGRAPH

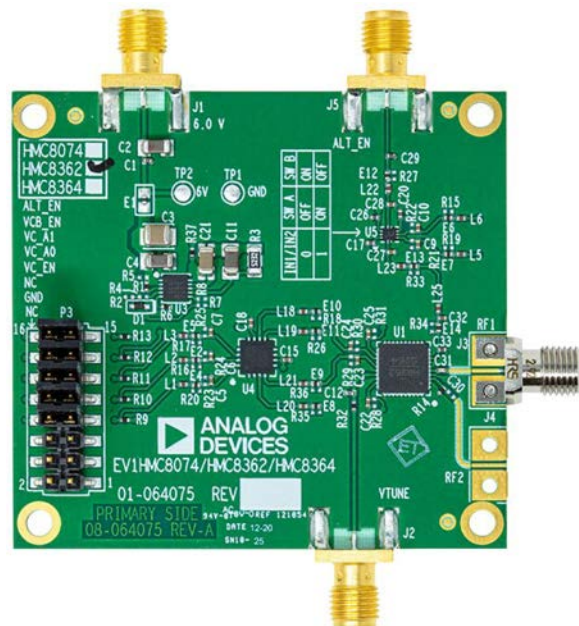


Figure 1.

## TABLE OF CONTENTS

Features .....	1	Buffer Amplifier .....	4
Evaluation Kit Contents.....	1	RF Output.....	4
Equipment Needed.....	1	Loop Filter.....	5
Online Resources.....	1	Default Configuration .....	5
General Description .....	1	Evaluation Board Software.....	6
EV1HMC8362LP6G/EV1HMC8364LP6G Evaluation Board		Software .....	6
Photograph.....	1	Evaluation and Test .....	7
Revision History .....	2	Evaluation Board Schematic and Artwork.....	8
Getting Started .....	3	EV1HMC8362LP6G Schematic .....	8
Evaluation Board Setup Procedure .....	3	Silkscreen Layers .....	9
Evaluation Board Hardware.....	4	Ordering Information.....	10
Power Supplies .....	4	Bill of Materials.....	10
Voltage Controlled Oscillator (VCO) .....	4		

## REVISION HISTORY

9/2020—Revision 0: Initial Version

## GETTING STARTED

### EVALUATION BOARD SETUP PROCEDURE

To configure the EV1HMC8362LP6G or EV1HMC8364LP6G for the first time, perform the following steps:

1. Verify that the analog power supply used to power the evaluation board is configured to allow an output of 6.0 V and 200 mA of compliance current.
2. Disable the power supply output.
3. Using a double shielded BNC cable and a BNC to SMA adapter, connect the analog power supply to J1.
4. Use the supplied shorting jumpers to configure the logic, as shown in Figure 2. In the configuration shown in Figure 2, alternative 5 V supply, the ADG1604 multiplexer, VCO Band 1 of the HMC8362 or HMC8364, and the output buffer amplifier are all enabled. When a jumper is disconnected, the corresponding signal is pulled up to  $V_{CC}$ . To reset a pin, connect the shorting jumper from the pin to the adjacent ground (GND). Figure 2 is annotated in green to indicate where a jumper is connected and thus shorted to ground.
5. Connect the low noise, variable power supply to the SMA connector on the tuning port (J2) using a double shielded BNC cable and a BNC to SMA adapter. Torque this connection to 8 in/lb using an SMA torque wrench.
6. Connect a 50  $\Omega$  RF cable capable of mating to the 2.92 mm K connector at J3, and torque this connection to 8 in/lb. Connect the other end of the cable to a signal source analyzer.
7. Enable the 6 V power supply. Approximately 103 mA is drawn if the device is configured correctly.
8. Enable the variable power supply, and adjust the tuning voltage to within the range of the VCO band being used.
9. Verify that the correct output frequency is observed on the signal source analyzer. An example using the HMC8362 is outlined in the Evaluation and Test section.

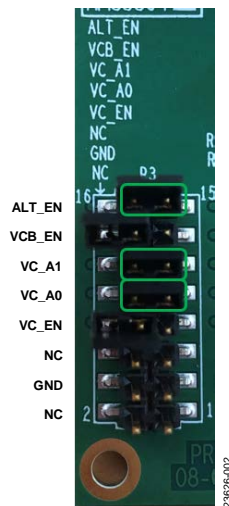


Figure 2. Connector P3 Jumper Configuration: Alternative 5 V Supply, Multiplexer, VCO Band 1, and Buffer Amplifier Enabled

## EVALUATION BOARD HARDWARE

The EV1HMC8362LP6G and EV1HMC8364LP6G are identical except for Resistor R6, which sets the current limit function of the [LT3042](#), and C31, which is the ac coupling capacitor on the RF output port.

The evaluation board schematics, assembly, silkscreen, and bill of materials are available in the Evaluation Board Schematic and Artwork section and Ordering Information section. The Gerber fabrication files are available at [www.analog.com/HMC8362](http://www.analog.com/HMC8362) and [www.analog.com/HMC8364](http://www.analog.com/HMC8364).

### POWER SUPPLIES

The EV1HMC8362LP6G and EV1HMC8364LP6G boards are powered by a 6 V dc (150 mA) power supply connected to the J1 SMA connector labeled 6.0 V. This supply path includes a single ultralow noise, low dropout linear regulator, the [LT3042](#). As an extra safeguard, the [LT3042](#) is configured to use the current-limit feature. A resistor (R6) sets the current limit on ILIM (Pin 5) of the [LT3042](#) to 114 mA ( $R6 = 1100 \Omega$ ) for the EV1HMC8362LP6G and 156 mA ( $R6 = 806 \Omega$ ) for the EV1HMC8364LP6G.

Users that intend to use an external power supply such as the Linduino® or Arduino® Uno microcontroller to directly program the logic from the P3 header must remove the five 10 k $\Omega$  resistors (R9, R10, R11, R12, and R13) or damage may occur.

A second low noise power supply cable providing up to 13.5 V is required to tune the VCOs. Use of a noisy power supply on the tuning port results in narrow-band FM modulation and sidebands.

### VOLTAGE CONTROLLED OSCILLATOR (VCO)

The [HMC8362](#) and [HMC8364](#) include a total of four VCO cores that generate a range of fundamental frequencies. The frequency range of each core overlaps the adjacent core to allow continuous frequency coverage including any supply and temperature variation.

By generating fundamental frequencies, the need for additional filtering can be reduced or eliminated because there are no subharmonics. The tuning sensitivity across the band is similar for each core, which simplifies the loop filter design. Any frequency planning or dynamic loop bandwidth adjustment required to manage spurs or settling time is made easier by the consistent tuning sensitivity from core to core. The integrated common tuning (VTUNE on J2) and RF output (J3) ports simplify layout. Each band has an allowable tune voltage of 1.0 V dc to 13.5 V dc.

The oscillator cores must be selected, one at a time, depending on the frequency range required at any point in time by the application. The VCO cores are selected by simply enabling the supply voltage at its respective bias pin (VC1 through VC4). The EV1HMC8362LP6G and EV1HMC8364LP6G boards accomplish this VCO core selection through the use of the

[ADG1604](#) 4:1 multiplexer. The VCO cores can be enabled and disabled in any sequence desired.

The EV1HMC8362LP6G and EV1HMC8364LP6G boards include additional filtering to prevent supply voltage overshoot and undershoot, which can damage the device if overshoot exceeds 5.5 V. This filtering provides 5 V of biasing that settles within about 1  $\mu$ s.

### BUFFER AMPLIFIER

The buffer amplifier used in the [HMC8362](#) and [HMC8364](#) is a broadband cascode design that draws approximately 12 mA and is shared by all four VCO cores. Pin 8 (VCB) of the [HMC8362](#) and [HMC8364](#) provides the bias voltage for the upper half of the cascode amplifier. The VCO outputs provide the biasing for the lower half of the cascode amplifier stage. When one of the four VCOs is enabled, the cascode amplifier becomes fully enabled and provides an output signal at Pin 5 (RFOUT). The buffer amplifier was designed to handle the power supplied by only one VCO at a time. To prevent long-term damage that can occur if more than one VCO is powered up simultaneously, the EV1HMC8362LP6G and EV1HMC8364LP6G boards incorporate the [ADG1604](#) 4:1 multiplexer. As configured on the EV1HMC8362LP6G and EV1HMC8364LP6G, the [ADG1604](#) multiplexer incorporates exclusive OR (XOR) logic and the ability to break contact with one VCO for a minimum of 30 ns before closing the contacts on the next switch to power up a different VCO core. To minimize the switching time of the [ADG1604](#), 5 V logic is used but 3 V can also be used through an external power supply or microcontroller such as a Linduino or Arduino Uno.

Refer to the [ADG1604](#) data sheet for more information regarding the [ADG1604](#) logic and use with other logic levels.

Users can opt to leave the VCO enabled and power down Pin 8 (VCB) to mute the output signal, which leaves the lower stage of the cascode enabled. However, because the upper circuitry is disabled, RF is not routed to the output.

Figure 5 shows the EV1HMC8362LP6G with VCO Band 1, but with the output buffer muted (VCB\_EN on P3 = 0).

For additional details on the buffer amplifier circuitry, consult the [HMC8362](#) or [HMC8364](#) data sheet.

### RF OUTPUT

The EV1HMC8362LP6G and EV1HMC8364LP6G boards have a single RF output port (J3). J3 is supplied by a buffer amplifier that is common to all four VCO cores.

J3 is a single-ended RF output that operates up to 26.6 GHz. The actual frequency range and power level at any given time depends on which quadband VCO variant is being evaluated and the VCO core that is enabled. Consult the [HMC8362](#) and [HMC8364](#) data sheets for additional information relative to the specific variant being evaluated for more information.

## LOOP FILTER

Although the EV1HMC8362LP6G and EV1HMC8364LP6G boards do not incorporate the entire loop filter, they do provide the means to filter noise that may appear on the tuning port when evaluating only the VCOs.

By default, a 100 pF capacitor (C12) is placed near Pin 27 ( $V_{TUNE}$ ) of the [HMC8362](#) and [HMC8364](#) to filter high frequency noise that may couple onto the tune port path when evaluating the various VCOs.

The EV1HMC8362LP6G and EV1HMC8364LP6G boards also include placements for the last pole of a loop filter on the tuning port path for use when configuring the [HMC8362](#) and [HMC8364](#) with an Analog Devices, Inc., standalone phase-locked loop (PLL) product like the [ADF41513](#). Although the tuning port path and input capacitance of the VCO makes up the last pole of the loop filter, this user guide refers to the last pole as that which can be accessed by the user.

Due to the increased length of the loop filter path that typically occurs when using evaluation boards to build a synthesizer, placement of the loop filter components becomes critical. Loop stability and overall performance is improved by placing the first pole of the loop filter as close to the PLL charge pump (CP) output as possible while placing the last pole as close to the tuning port pin ( $V_{TUNE}$ ) of the VCO. The placement of any

additional poles that may exist between the first and last pole of the loop filter are not as critical. Therefore, these filter poles remain on the [ADF41513](#). The placements for this last pole on the EV1HMC8362LP6G and EV1HMC8364LP6G are populated by default and consist of R32 (0  $\Omega$  by default) and a 100 pF capacitor (C12) near Pin 27 ( $V_{TUNE}$ ). Users can replace these components with the proper values as needed.

The tuning voltage requirements of the [HMC8362](#) and [HMC8364](#) (1.0 V to 13.5 V) require an active loop filter to be used unless the charge pump of the PLL can output at least 14 V. The PLL evaluation board typically includes placements for the operational amplifier, its biasing circuitry, and any component placements. Therefore, these components are not included on the EV1HMC8362LP6G and EV1HMC8364LP6G.

SMA Connector J2 provides a means to connect the PLL CP output to the tuning port ( $V_{TUNE}$ ) when the EV1HMC8362LP6G and EV1HMC8364LP6G are used with an optional PLL evaluation board. J2 can also be used to manually tune the VCO within its band when evaluating the open-loop VCO performance.

## DEFAULT CONFIGURATION

All components necessary for local oscillator generation are inserted on the EV1HMC8362LP6G and EV1HMC8364LP6G boards.

## EVALUATION BOARD SOFTWARE

Currently, there is no software available for the EV1HMC8362LP6G and EV1HMC8364LP6G because they can be evaluated without the use of software. However, the EV1HMC8362LP6G and EV1HMC8364LP6G are configured in a manner that allows use of a Linduino, Arduino Uno, [SDP-K1](#), or similar microcontroller board, which may be beneficial for

users needing to develop and test switching algorithms for their application.

To connect the [SDP-K1](#) interface board to the EV1HMC8362LP6G or EV1HMC8364LP6G, flip the [SDP-K1](#) board over so that the digital input/output pins (Pin 8 through Pin 14) of the [SDP-K1](#) line up with the odd numbered pins of Connector P3 (Pin 3 to Pin 15), respectively, as shown in Figure 3.



Figure 3. SDP-K1 Board Mounted to the EV1HMC8362LP6G

23626-003

## EVALUATION AND TEST

To configure the EV1HMC8362LP6G and EV1HMC8364LP6G for the first time, follow Step 1 through Step 6 outlined in the Evaluation Board Setup Procedure section.

The frequency vs. tuning voltage listed in the following steps are specific to the EV1HMC8362LP6G, but the same process is applicable to the EV1HMC8364LP6G. The frequency range and performance are different.

1. Enable the variable power supply, and adjust the tuning voltage to 8.45 V.
2. If the EV1HMC8362LP6G is configured correctly, a signal at approximately 13.5 GHz with approximately 0 dBm to 2 dBm of output power appears on a spectrum analyzer or signal source analyzer. Refer to Figure 4.
3. Remove the bias for the buffer amplifier (VCB), which results in the output power decreasing by approximately 28 dBm. Refer to Figure 5.
4. Finally, use the signal source analyzer to measure the phase noise. Refer to Figure 6.

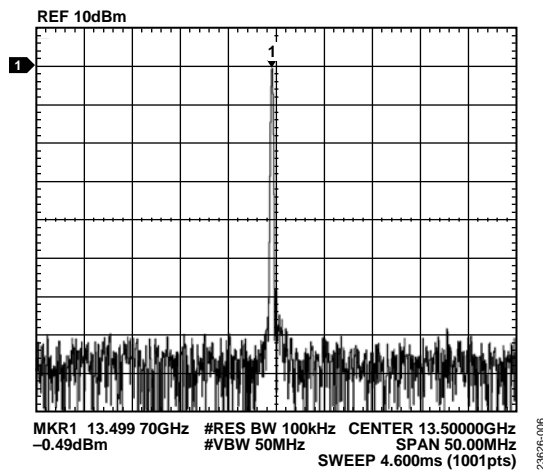


Figure 4. EV1HMC8362LP6G, VCO Band 1,  $V_{TUNE} = 8.45$  V, 13.5 GHz, Includes Insertion Loss of RF Cable

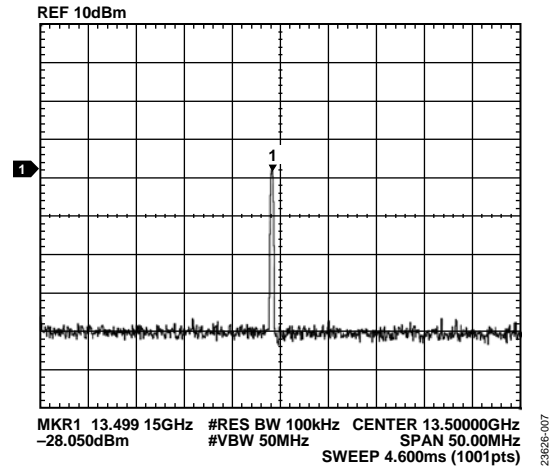


Figure 5. EV1HMC8362LP6G, VCO Band 1,  $V_{TUNE} = 8.45$  V, 13.5 GHz, Buffer Amplifier Disabled (J3 Output Muted), Includes Insertion Loss of RF Cable

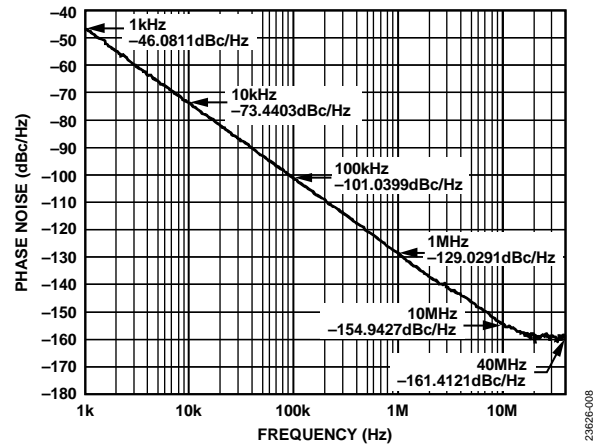


Figure 6. EV1HMC8362LP6G Phase Noise at J3, VCO Band 1,  $V_{TUNE} = 8.45$  V, 13.5 GHz

EVALUATION BOARD SCHEMATIC AND ARTWORK

EV1HMC8362LP6G SCHEMATIC

Figure 7 shows the schematic for the EV1HMC8362LP6G. For the EV1HMC8364LP6G variant, two component values that must be changed are highlighted within this schematic.

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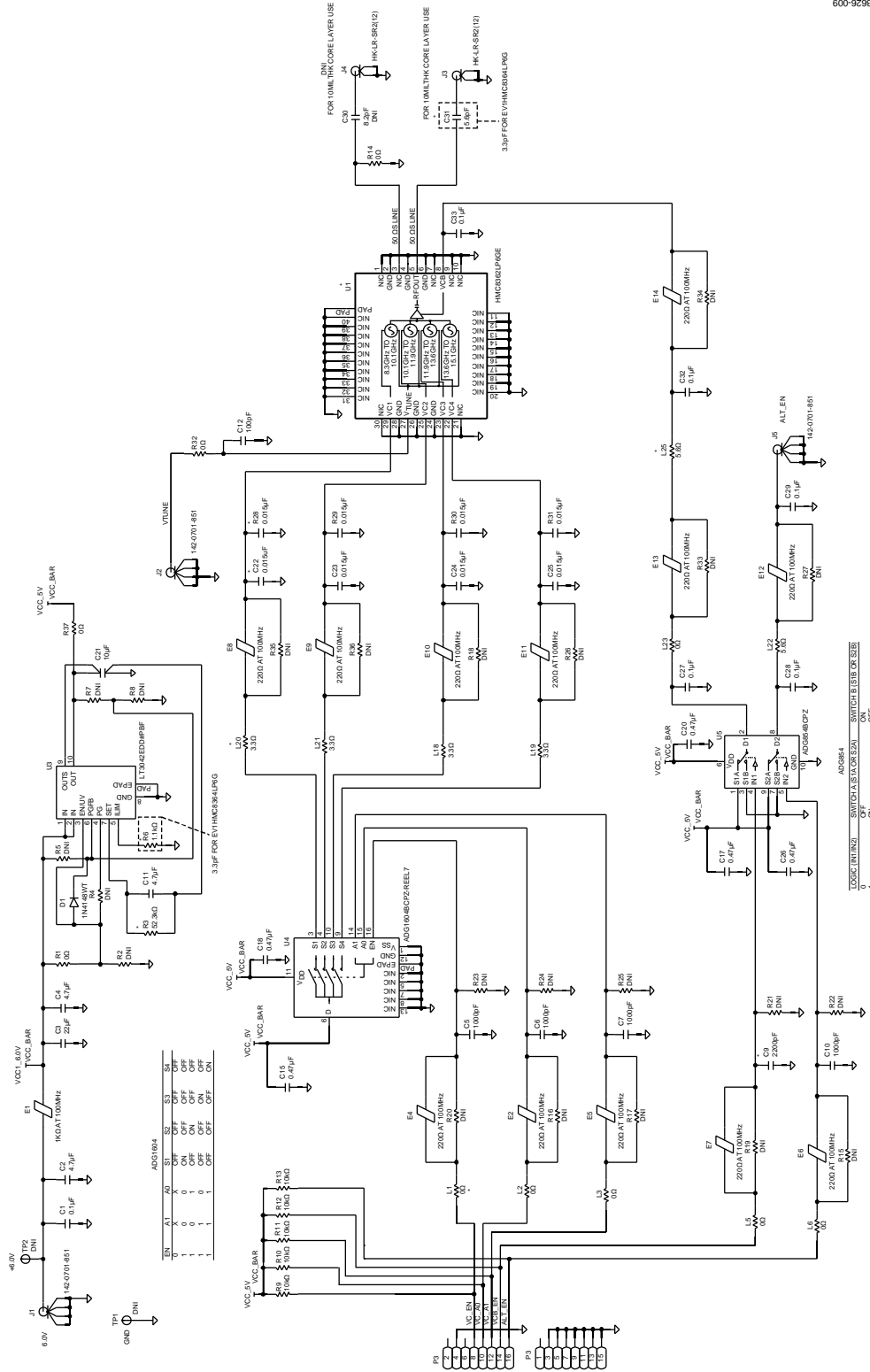


Figure 7. EV1HMC8362LP6G Schematic



SILKSCREEN LAYERS

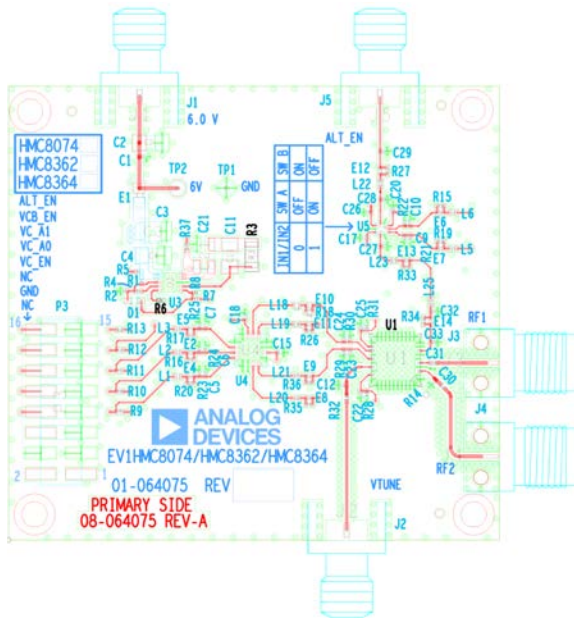


Figure 8. EV1HMC8362LP6G and EV1HMC8364LP6G Silk Screen and Metal 1 (Top Side)

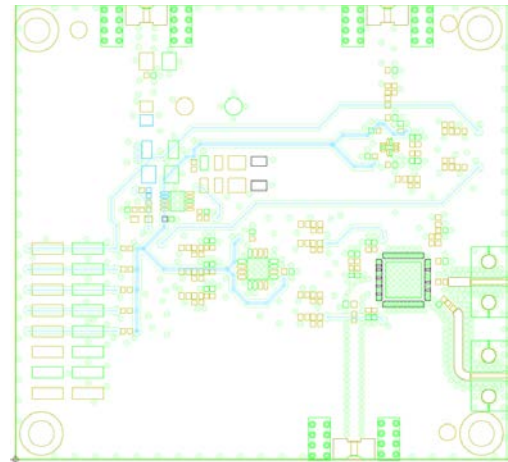


Figure 10. EV1HMC8362LP6G and EV1HMC8364LP6G Metal 3 (RF and DC)

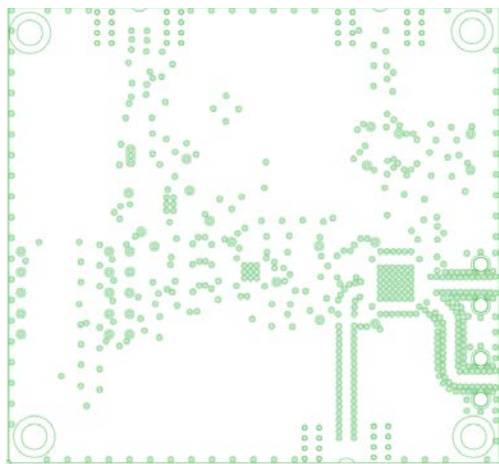


Figure 9. EV1HMC8362LP6G and EV1HMC8364LP6G Metal 2 (Ground)

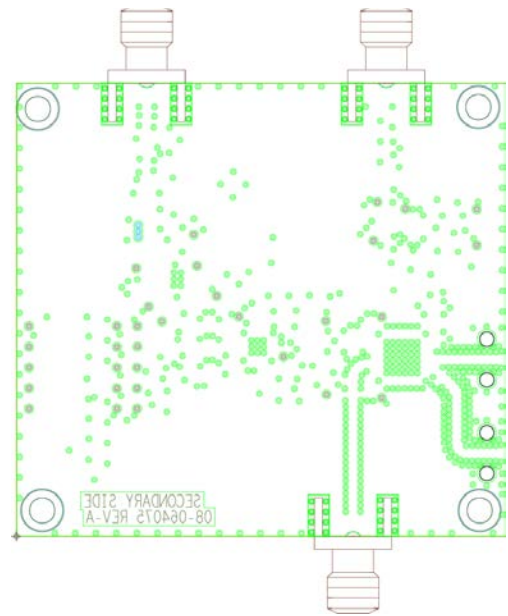


Figure 11. EV1HMC8362LP6G and EV1HMC8364LP6G Metal 4 (Backside)

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 1.

Reference Designator	Description	Value	Manufacturer	Part Number
C1, C27, C28, C32, C29, C33	Ceramic capacitor, X7R, automotive grade	0.1 $\mu$ F	Murata	GCM155R71C104KA55D
C5, C6, C7, C10	Ceramic capacitor, general-purpose	1000 pF	Murata	GRM1555C1H102JA01
C2, C4, C11	Ceramic capacitor, X7R	4.7 $\mu$ F	Kemet	C1206C475K3RACTU
C12	Capacitor, multilayer ceramic, high temperature, 4.7 $\mu$ F	100 pF	TDK	C1005NP01H101J050BA
C15, C17, C18, C20, C26	Ceramic capacitor, 0.47 $\mu$ F, 10V, 10%, X7S 0402, automotive grade, 100 pF	0.47 $\mu$ F	Murata	GCM155C71A474KE36D
C21	Ceramic capacitor, X7R, 4-pin footprint	10 $\mu$ F	Murata	GRM32ER71H106KA12L
C22, C23, C24, C25, R28, R29, R30, R31	Ceramic capacitor, 0.015 $\mu$ F, 50 V, 5%, X7R, 0402, automotive	0.015 $\mu$ F	Murata	GCM155R71H153JA55D
C3	Ceramic capacitor, 22 $\mu$ F, 25 V, 10%, X7R	22 $\mu$ F	Samsung	CL32B226KAJNNNE
C31	Ceramic capacitor, 5.6 pF, 200 V, 0.1 pF tolerance, C0G, 0402	5.6 pF	American Technical Ceramics	600L5R6BT200T
C9	Ceramic capacitor, 2200 pF, 50 V, 10%, X7R, 0402 AEC-Q200	2200 pF	Murata	GCM155R71H222KA37D
D1	Diode, fast switching	Not applicable	Diodes, Inc.	1N4148WT
E1	Inductor, chip ferrite bead, multilayer, 0.5 A, 0.280 $\Omega$ maximum	1 k $\Omega$ at 100 MHz	Murata	BLM21AG102SN1D
E2, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14	Inductor, chip ferrite bead, 0.7 $\Omega$ , 0.3 A	220 $\Omega$ at 100 MHz	Murata	BLM15GG221SN1D
J1, J2, J5	SMA, 50 $\Omega$ , end launch jack	Not applicable	Cinch	142-0701-851
J3	2.92 mm coaxial for frequency test measurements, 50 $\Omega$ , 40 GHz	Not applicable	Hirose Electric Co.	HK-LR-SR2(12)
L18, L19, L20, L21	Surface-mount resistor, 3.3 $\Omega$ , 1%, 1/16 W, 0402 size	3.3 $\Omega$	Yageo	RC0402FR-073R3L
L1, L2, L3, L5, L6, L23, R1, R32, R37, R14	Resistor, surface-mount jumper	0 $\Omega$	Panasonic	ERJ-2GE0R00X
L22, L25	Resistor, thick film chip	5.6 $\Omega$	Panasonic	ERJ-2GEJ5R6X
P3	16-position, male header, double row	Not applicable	Samtec, Inc.	TSM-108-01-L-DV
R9, R10, R11, R12, R13	Precision resistor, thick film chip	10 k $\Omega$	Panasonic	ERJ-2RKF1002X
R3	Surface-mount resistor, 52.3 k $\Omega$ , 1%, 1/4 W, AEC-Q200	52.3 k $\Omega$	Panasonic	ERJ-8ENF5232V
R6	Surface-mount resistor, 1.1 k $\Omega$ , 1%, 1/16 W, 0402 size	1.1 k $\Omega$	Yageo	RC0402FR-071K1L
U1	Quadband monolithic microwave integrated circuit (MMIC), VCO, 11.90 GHz to 18.30 GHz	Not applicable	Analog Devices	<a href="#">HMC8362LP6GE</a>
U3	20 V, 200 mA, ultralow noise, ultrahigh power supply rejection ratio (PSRR) RF linear regulator	Not applicable	Analog Devices	<a href="#">LT3042EDD#PBF</a>
U4	3.3 V, 4:1 multiplexer	Not applicable	Analog Devices	<a href="#">ADG1604BCPZ-REEL7</a>
U5	CMOS, dual, SPDT multiplexer	Not applicable	Analog Devices	<a href="#">ADG854BCPZ-REEL7</a>

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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