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### Evaluating the AD5040/AD5060, AD5061, and AD5062 16-/14-Bit, nanoDAC

#### **FEATURES**

Full featured evaluation board for the AD5040/AD5060, AD5061 or AD5062

On board reference

**Various link options** 

PC control in conjunction with the Analog Devices, Inc., EVAL-SDP-CB1Z system demonstration platform (SDP)

#### **EVALUATION KIT CONTENTS**

EVAL-AD5040SDZ, EVAL-AD5060SDZ, EVAL-AD5061SDZ,

and EVAL-AD5062SDZ evaluation board CD includes

Self installing evaluation software that allows users to control the board and exercise all functions of the device Electronic version of the EVAL-AD5040SDZ/

EVAL-AD5060SDZ/EVAL-AD5061SDZ/EVAL-AD5062SDZ user guide

#### ADDITIONAL EQUIPMENT AND SOFTWARE NEEDED

EVAL-SDP-CB1Z SDP board, includes a USB cable PC running Windows® Vista, Windows 7, or Windows 8 with a USB 2.0 port

#### **ONLINE RESOURCES**

#### **Documents needed**

AD5040/AD5060, AD5061, and AD5062 data sheets EVAL-AD5040SDZ/EVAL-AD5060SDZ/EVAL-AD5061SDZ/

EVAL-AD5062SDZ user guide

**Required software** 

AD5040/AD5060, AD5061, and AD5062 evaluation software (download from the AD5040/AD5060, AD5061, and AD5062 product pages)

Design and integration files

Schematics, layout files, and bill of materials

#### **GENERAL DESCRIPTION**

This user guide details the operation of the evaluation boards for the AD5040/AD5060, AD5061 and AD5062 14-/16-bit, voltage output *nano*DACs. The evaluation boards are identical apart from the DAC being evaluated, which is determined by the order code. For the purpose of this user guide, the AD5040/AD5060, AD5061, or AD5062 is referred to as the device being evaluated.

The evaluation board helps users quickly prototype new circuits for the AD5040/AD5060, AD5061, or AD5062 and reduce design time. The AD5040/AD5060, AD5061, and AD5062 operate from a single 2.7 V to 5.5 V supply. An ADR444 is provided on-board as a 4.096 V reference source.

Full data on the AD5040/AD5060, AD5061, and AD5062 is available in the appropriate data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

The evaluation board interfaces to the USB port of a PC via the SDP board. Software is supplied with the evaluation board to allow the user to program the AD5040/AD5060, AD5061, or the AD5062.

The evaluation boards are compatible with the EVAL-SDP-CB1Z Blackfin<sup>®</sup> SDP controller board (SDP-B).

# EVAL-AD5040SDZ/EVAL-AD5060SDZ to EVAL-AD5062SDZ User Guide

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#### **REVISION HISTORY**

4/16—Revision 0: Initial Version

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# UG-923

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## **TYPICAL EVALUATION BOARD SETUP**

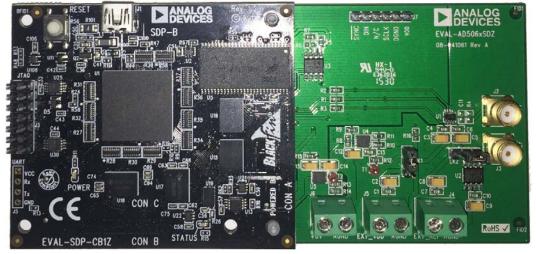


Figure 1.

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### **GETTING STARTED** INSTALLING THE SOFTWARE

The evaluation kit for the device being evaluated includes selfinstalling software on the provided CD. The software is compatible with Windows Vista (32-bit), Windows 7 (32-bit and 64-bit), and Windows 8 (32-bit and 64-bit).

Install the software before connecting the SDP-B board to the USB port of the PC to ensure the SDP-B board is recognized when it connects to the PC.

To install the software, take the following steps:

- 1. Start the Windows operating system and insert the CD.
- 2. The installation software opens automatically. If it does not open automatically, run the **setup.exe** file from the CD.
- 3. After installation is complete, power up the evaluation board as described in the Power Supplies section.

- 4. Connect the evaluation board to the SDP-B board and connect the SDP-B board to the PC using the USB cable included in the kit.
- 5. When the software detects the evaluation board, proceed through any dialog boxes that appear to finalize the installation.

### **EVALUATION BOARD SETUP PROCEDURES**

To set up the evaluation board, take the following steps:

- 1. Connect the evaluation board to the SDP-B board and connect the USB cable between the SDP-B board and the PC.
- Power the SDP-B and evaluation boards by connecting a 6 V dc to the J6 connector.

### **EVALUATION BOARD HARDWARE** POWER SUPPLIES

To power the evaluation board, supply 6 V to connector J6. This creates a 5 V supply for the device being evaluated and a 3.3 V supply to power the SDP-B board. Alternatively, if the SDP-B board is not being used, a 2.7 V to 5.5 V can connect to Connector J5. An external reference voltage may be required so the reference voltage does not exceed  $V_{DD}$ .

All supplies are decoupled to ground with 10  $\mu F$  tantalum and 0.1  $\mu F$  ceramic capacitors.

### **INPUT SIGNALS**

When the SDP-B board controls the evaluation board, the digital input signals are applied to Connector J1. When the SDP-B board is not used, apply the digital signals Connector J7.

#### **OUTPUT SIGNALS**

The DAC output voltage is available on the J2 SMB connector.

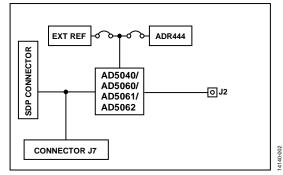


Figure 2. Evaluation Board Block Diagram

#### **Table 1. Power Supply Connectors**

Connector	Voltage
J5	Analog power supply, VDD for single-supply operation.
J6	Power supply connection when using the evaluation board with the SDP-B board.

### LINK CONFIGURATION OPTIONS

There are two link options (LK1 and LK2) that must be set correctly to select the appropriate operating setup before using the evaluation board. The functions of these options are described in Table 2.

### **SETUP CONDITIONS**

Before applying power and signals to the evaluation board, ensure that all link positions are as required by the operating mode. There are two modes in which to operate the evaluation board: SDP-B controlled mode, used with the SDP-B board, or the evaluation board used in standalone mode.

Table 2 also shows the default positions where the links are set when the evaluation board is packaged. When the board is shipped, it is set up to operate with the SDP-B board in the SDP controlled mode.

#### **Table 2. Link Functions**

Link No.	Function	Default Position	
LK1	This link selects the V <sub>DD</sub> source for the device being evaluated.	A	
	Position A selects the output of the ADP7102 voltage regulator (U4) as the $V_{DD}$ source.		
	Position B selects connector J5 as the $V_{DD}$ source.		
LK2	This link selects the reference source for the device being evaluated.	В	
	Position A selects an external reference voltage applied to Connector J4.		
	Position B selects the on-board ADR444, 4.096 V reference.		

### **EVALUATION BOARD CIRCUITRY**

Control of the device is typically performed by the SDP-B board, which is attached to Connector J1. The SDP-B board allows the software provided with the kit to load register values and set the voltage of the DAC output.

When the SDP-B board is not required, the control signals can be applied to the device by connecting them to the relevant pins on Connector J7.

The DAC output voltage is available on the J2 SMB Connector.

# HOW TO USE THE SOFTWARE STARTING THE SOFTWARE

To run the software, take the following steps:

- 1. Connect the evaluation board to the SDP-B board and connect the USB cable between the SDP-B board and the PC.
- 2. Power the SDP-B board and the evaluation board by connecting 5 V to Connector J2.
- Click Start > All Programs > Analog Devices > AD506x Evaluation Software The software will identify the board connected to the SDP-B and display the board name, as shown in Figure 3.

1 matching system matching board.	found. LED1 is flash	ing on
Press Select to use t	this board.	
SDPB:		
		<b>^</b>
EVAL-AD5062SDZ		_
EVAL-AD30025D2		
EVAL-AU5062502		
EVAL-AU5062502		-

Figure 3. Connection Message

If the SDP-B board is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 4). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

No matching system is attached correctly		
Your SDP board ma Please allow up to 4		ting.
		-

Figure 4. Connectivity Error

When the software connects to the SDP-B and evaluation board, the main window of the evaluation software opens, as shown in Figure 5.

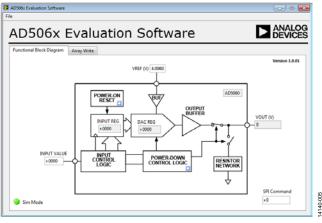


Figure 5. AD506x Evaluation Software Main Window

### SOFTWARE OPERATION

The evaluation software allows the user to program values to the input register of the DAC. The value that is written and the value of the reference voltage calculates the output voltage.

#### Power-Down Menu

The device has three power down modes. These can be accessed by clicking the blue box on the **Power-Down Control Logic** section of the block diagram (Figure 5). The **Powerdown Configuration** window, shown in Figure 6, then appears to select the required operating mode.

The input register can still be loaded while the device is in power down mode, but the output voltage is determined by the power down condition.

Powerdown Configuration	×
Power Down Control	
Normal Operation	
Migh Impedance	
100K to GND	
1K to GND	
ОК	

Figure 6. Powerdown Configuration Window

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### **EVALUATION BOARD SCHEMATICS AND ARTWORK**

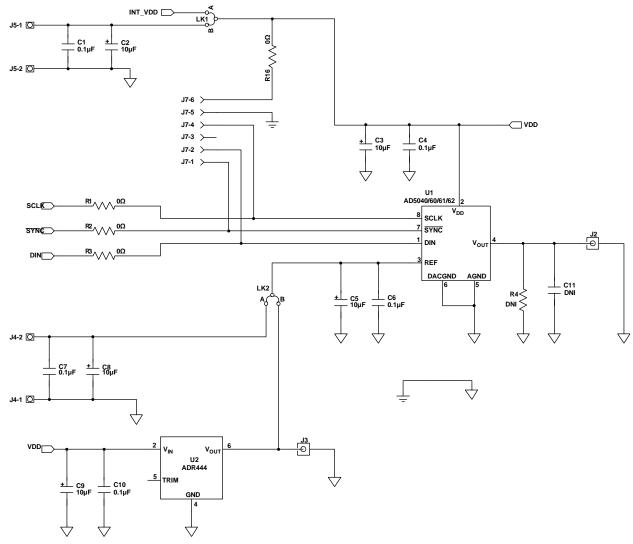


Figure 7. EVAL-AD5040SDZ/EVAL-AD5060SDZ/EVAL-AD5061SDZ/EVAL-AD5062SDZ Schematic, Page 1

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### EVAL-AD5040SDZ/EVAL-AD5060SDZ to EVAL-AD5062SDZ User Guide

#### +3.3\ BMODE1 UART\_TX GND SLEEP WAKE R5 Re - C13 0.1µF Ş 64 65 100kΩ Ţ SDP STANDARD CONNECTOR U3 U4 NO 1 A0 A1 A1 A2 VSS VCC 8 WP 6 SCL 5 SDA ADP7102ACP2 VOUT VDD 24LC64-I/S C12 ± TIMERS R10 4 ≶ N/C Gr GND 7 GPI05 7 GPI03 7 GPI03 7 SCL\_0 SCL\_0 SDA\_0 GND SPI\_CLK SPI\_CLK SPI\_MISO SPI\_MISO SPI\_SEL\_/ GNI SPI\_SEL\_/ SPI\_SEL\_/ 100kΩ $\overline{\downarrow}$ GENERAL INPUT/OUTPUT Ŧ 76 77 78 79 J6-2 AGND ADJ R11 30.9kΩ ≷ I<sup>2</sup>C SCL\_1 SPI SEL INSPI SS SPI SEL SS SPI SEL B GND T SPD SEL B SPD SEL B SPD ST SP ム R8 Λ/ΛΛ 100kΩ vin <u>T</u>1 SPI\_ULK SPI\_MISO SPI\_SEL\_A GND SPORT\_TSCLK SPI $\downarrow$ PG R9 100kΩ ≥ EP ORT\_TSCLK SPORT\_TFS SPORT\_TFS SPORT\_TFS SPORT\_DR0 ORT\_RSCLK ORT\_RSCLK PAR\_CLK PAR\_CLK PAR\_A0 PAR\_A0 PAR\_A2 SPORT Ą $\triangleleft$ PAR\_AZ GND PAR\_INT PAR\_WR PAR\_D0 PAR\_D2 PAR\_D2 U5 ADP7102ACPZ-5.0-R7 PARALLEL VOUT PAR\_D5 GND PAR\_D7 PAR\_D9 PAR\_D11 PAR\_D13 PAR\_D14 GND PAR\_D17\* PAR\_D21\* PAR\_D21\* PAR\_D23\* GND C14 ±⊥ 1µF ----17 16 15 GND PAR\_DO PAR\_DO PAR\_D10 PAR\_D10 + C15 N/C 1 1µF D10 D12 SENSE ≥<sup>R15</sup> 100kΩ GND D15 D16 D18 D20 PAR \*PAR \*PAR \*PAR \*PAR ÷ R13 **T**2 PAR GND USB GND GND \*PAR\_D20 \*PAR\_D22 GND VIO(+3.3V) GND GND NC DP NC 100kΩ PG VBUS ← +3.3V R14 100kΩ 9 GND NC VIN 119 \*NC ON BLACKFIN SDP Ŧ Figure 8. EVAL-AD5040SDZ/EVAL-AD5060SDZ/EVAL-AD5061SDZ/EVAL-AD5062SDZ Schematic, Page 2 ANALOG DEVICES EVAL-AD506xSDZ Ë • 08-041061 Rev A Rf U3 R2 = = R1 🔳 5 R3 = = U1 C4 . R9 🔳 🔳 = = R11 R8 C3 0000 R10 C12 २१५ 🔳 🔳 -LK1 214 U2 C8 C2 R13 C1 🔳 🔳 C7 🔳 🔳 = = R14 10 . C9 RoHS 🗸 4140-009 • +6V AGND EXT\_VDD AGND EXT\_REF AGND

Figure 9. Component Placement Drawing

+6V -10

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# EVAL-AD5040SDZ/EVAL-AD5060SDZ to EVAL-AD5062SDZ User Guide

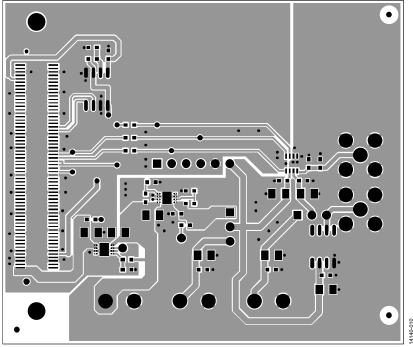


Figure 10. Printed Circuit Board, Component Side

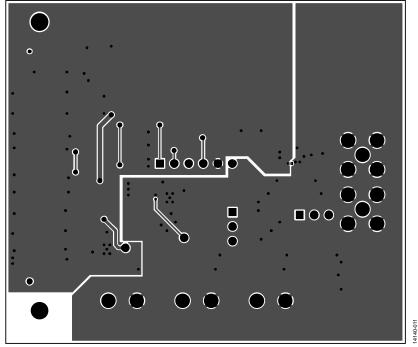


Figure 11. Printed Circuit Board, Solder Side

### **ORDERING INFORMATION**

#### **BILL OF MATERIALS**

Table 3.

Qty	Reference Designator	Description	Part Number <sup>1</sup>
6	C1, C4, C6, C7, C10, C13	100 nF, 50 V, 0603 capacitor	FEC 8820023
5	C2, C3, C5, C8, C9	10 μF, 16 V, tantalum capacitor	FEC 1432339
1	C11	Multilayer ceramic capacitor	Do not insert
3	C12 to C15	1 μF, 16 V, tantalum capacitor	FEC 498701
1	G1	Copper short	Not applicable
1	J1	120-way connector, 0.6 mm pitch	FEC 1324660
2	J2, J3	50 Ω SMA jack, vertical	FEC 1814376
2	J4, J5	2-pin terminal block (5 mm pitch)	FEC 1177875
1	J6	2-pin terminal block (5 mm pitch)	FEC 151789
1	J7	7-pin SIL, 0.1" pitch, header	FEC 1022257 (8-way, cut to size)
2	LK1, LK2	Jumper block using 3-pin SIP header	FEC 1022248 and 150410
3	R1 to R3	0 Ω, 1%, 0603 resistor	FEC 9331662
2	R4, R6	0603 SMD resistor	Do not insert
10	R5, R7 to R15	100 kΩ, 1%, 0603 resistor	FEC 9330402
2	T1, T2	Red test point	FEC 8731144
1	U1 <sup>2</sup>	DAC	AD5060BRJZ-1500RL7/AD5040BRJZ-RL7/ AD5061BRUZ-1REEL7/AD5062-1REEL7
1	U2	4.096 V reference	ADR444ARZ
1	U3	64K I <sup>2</sup> C serial EEPROM	FEC 9758070
1	U4	Ultralow noise, linear regulator, adjustable	ADP7102ACPZ-R7
1	U5	5 V, ultralow noise, linear regulator	ADP7102ACPZ-5.0-R7
2	SCREW1, SCREW2	M3X10 nylon screw	FEC 7070597
2	NUT1, NUT2	M3 nylon nut/washer	FEC 7061857
4		Stick on feet, small, one on each corner	FEC 1165061

<sup>1</sup> FEC is Farnell Electronics Components.

<sup>2</sup> The Part Number populated depends on the evaluation board used.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).



#### ESD Caution

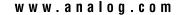
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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