14-Bit, 8-Channel, 250 kSPS PulSAR ADC

Enhanced Product

AD7949-EP

FEATURES

- 14-bit resolution with no missing codes
- 8-channel multiplexer with choice of inputs
  - Unipolar single-ended
  - Differential (GND sense)
  - Pseudobipolar
- Throughput: 250 kSPS
- INL/DNL: ±0.5/±0.25 LSB typical
- SINAD: 85 dB at 20 kHz
- THD: −100 dB at 20 kHz
- Analog input range: 0 V to V_{REF} with V_{REF} up to VDD
- Multiple reference types
  - Internal selectable 2.5 V or 4.096 V
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor (TEMP)
- Channel sequencer, selectable 1-pole filter, busy indicator
- No pipeline delay, SAR architecture
- Single-supply 2.3 V to 5.5 V operation with
  - 1.8 V to 5.5 V logic interface
- Serial interface compatible with SPI, MICROWIRE, QSPI, and DSP
- Power dissipation
  - 2.9 mW at 2.5 V/200 kSPS
  - 10.8 mW at 5 V/250 kSPS
- Standby current: 50 nA
- 20-lead 4 mm × 4 mm LFCSP package
- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Multichannel system monitoring
- Battery-powered equipment
- Medical instruments: ECG/EKG
- Mobile communications: GPS
- Power line monitoring
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process control

FUNCTIONAL BLOCK DIAGRAM

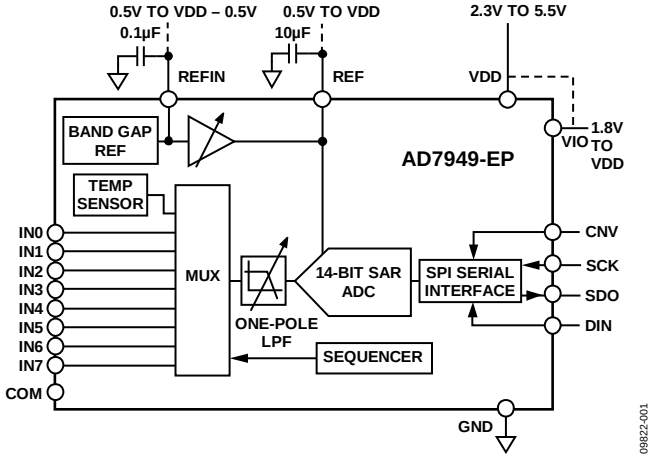

Figure 1.

GENERAL DESCRIPTION

The AD7949-EP is an 8-channel, 14-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) that operates from a single power supply, VDD.

The AD7949-EP contains all components for use in a multichannel, low power data acquisition system, including a true 14-bit SAR ADC with no missing codes; an 8-channel, low crosstalk multiplexer that is useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The AD7949-EP uses a simple SPI interface for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

The AD7949-EP is housed in a tiny 20-lead LFCSP with operation specified from −55°C to +125°C. Full details about this enhanced product are available in the AD7949 data sheet, which should be consulted in conjunction with this data sheet.

Table 1. Multichannel 14-/16-Bit PulSAR® ADCs

Type	Channels	250 kSPS	500 kSPS	ADC Driver
14-Bit	8	AD7949		ADA4841-1
16-Bit	4	AD7682		ADA4841-1
16-Bit	8	AD7689	AD7699	ADA4841-1

Rev. B
Document Feedback

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REVISION HISTORY

5/2018—Rev. A to Rev. B

Updated Outline Dimensions 12
Changes to Ordering Guide 12

5/2015—Rev. 0 to Rev. A

Changes to Table 1 1
Updated Outline Dimensions 12
Changes to Ordering Guide 12

4/2011—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications −55°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUT					
Voltage Range	Unipolar mode	0		$+V_{REF}$	V
	Bipolar mode	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Voltage	Positive input, unipolar and bipolar modes	−0.1		V_{REF} + 0.1	V
	Negative or COM input, unipolar mode	−0.1		+0.1	
	Negative or COM input, bipolar mode	$V_{REF}/2$ − 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	
Analog Input CMRR	f_{IN} = 250 kHz		68		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance[1]					
THROUGHPUT					
Conversion Rate					
Full Bandwidth[2]	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
¼ Bandwidth[2]	VDD = 4.5 V to 5.5 V	0		62.5	kSPS
	VDD = 2.3 V to 4.5 V	0		50	kSPS
Transient Response	Full-scale step, full bandwidth			1.8	µs
	Full-scale step, ¼ bandwidth			14.5	µs
ACCURACY					
No Missing Codes		14			Bits
Integral Linearity Error		−1	±0.5	+1	LSB[3]
Differential Linearity Error		−1	±0.25	+1	LSB
Transition Noise	REF = VDD = 5 V		0.1		LSB
Gain Error[4]		−5	±0.5	+5	LSB
Gain Error Match		−1	±0.2	+1	LSB
Gain Error Temperature Drift			±1		ppm/°C
Offset Error[4]			±0.5		LSB
Offset Error Match		−1	±0.2	+1	LSB
Offset Error Temperature Drift			±1		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.2		LSB
AC ACCURACY[5]					
Dynamic Range			85.6		dB[6]
Signal-to-Noise	f_{IN} = 20 kHz, V_{REF} = 5 V	84.5	85.5		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF		85		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF		84		dB
SINAD	f_{IN} = 20 kHz, V_{REF} = 5 V	84	85		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input		33.5		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF		85		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF		84		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−100		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		108		dB
Channel-to-Channel Crosstalk	f_{IN} = 100 kHz on adjacent channel(s)		−125		dB
SAMPLING DYNAMICS					
−3 dB Input Bandwidth	Full bandwidth		1.7		MHz
	¼ bandwidth		0.425		MHz
Aperture Delay	VDD = 5 V		2.5		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE					
REF Output Voltage	2.5 V, at 25°C	2.490	2.500	2.510	V
	4.096 V, at 25°C	4.086	4.096	4.106	V
REFIN Output Voltage[7]	2.5 V, at 25°C		1.2		V
	4.096 V, at 25°C		2.3		V
REF Output Current			±300		µA
Temperature Drift			±10		ppm/°C
Line Regulation	VDD = 5 V ± 5%		±15		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	CREF = 10 µF		5		ms
EXTERNAL REFERENCE					
Voltage Range	REF input	0.5		VDD + 0.3	V
	REFIN input (buffered)	0.5		VDD − 0.5	V
Current Drain	250 kSPS, REF = 5 V		50		µA
TEMPERATURE SENSOR					
Output Voltage[8]	At 25°C		283		mV
Temperature Sensitivity			1		mV/°C
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[9]					
Pipeline Delay[10]					
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.3		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
	Operating range	1.8		VDD + 0.3	V
Standby Current[11, 12]	VDD and VIO = 5 V, at 25°C		50		nA
Power Dissipation	VDD = 2.5 V, 100 SPS throughput		1.5		µW
	VDD = 2.5 V, 100 kSPS throughput		1.45	2.0	mW
	VDD = 2.5 V, 200 kSPS throughput		2.9	4.0	mW
	VDD = 5 V, 250 kSPS throughput		10.8	12.5	mW
	VDD = 5 V, 250 kSPS throughput with internal reference		13.5	15.5	mW
Energy per Conversion			50		nJ
TEMPERATURE RANGE[13]					
Specified Performance	T_{MIN} to T_{MAX}	−55		+125	°C

[1] See the AD7949 data sheet.
[2] The bandwidth is set in the configuration register.
[3] LSB means least significant bit. With the 5 V input range, one LSB = 305 µV.
[4] See the AD7949 data sheet. These specifications include full temperature range variation but not the error contribution from the external reference.
[5] With VDD = 5 V, unless otherwise noted.
[6] All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[7] This is the output from the internal band gap.
[8] The output voltage is internal and present on a dedicated multiplexer input.
[9] Unipolar mode: serial 14-bit straight binary.
Bipolar mode: serial 14-bit twos complement.
[10] Conversion results available immediately after completed conversion.
[11] With all digital inputs forced to VIO or GND as required.
[12] During acquisition phase.
[13] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

TIMING SPECIFICATIONS

VDD = 4.5 V to 5.5 V, VIO = 1.8 V to VDD, all specifications −55°C to +125°C, unless otherwise noted.

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			2.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	4.0			µs
Data Write/Read During Conversion	t_{DATA}			1.0	µs
CNV Pulse Width	t_{CNVH}	10			ns
SCK Period	t_{SCK}	t_{DSDO} + 2			ns
SCK Low Time	t_{SCKL}	11			ns
SCK High Time	t_{SCKH}	11			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				23	ns
VIO Above 1.8 V				28	ns
CNV Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
VIO Above 1.8 V				25	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			32	ns
CNV Low to SCK Rising Edge	t_{CLSCK}	10			ns
DIN Valid Setup Time from SCK Rising Edge	t_{SDIN}	5			ns
DIN Valid Hold Time from SCK Rising Edge	t_{HDIN}	5			ns

[1] See Figure 2 and Figure 3 for load conditions.

VDD = 2.3 V to 4.5 V, VIO = 1.8 V to VDD, all specifications −55°C to +125°C, unless otherwise noted.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}			3.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	5			µs
Data Write/Read During Conversion	t_{DATA}			1.2	µs
CNV Pulse Width	t_{CNVH}	10			ns
SCK Period	t_{SCK}	t_{DSDO} + 2			ns
SCK Low Time	t_{SCKL}	12			ns
SCK High Time	t_{SCKH}	12			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 3 V				24	ns
VIO Above 2.7 V				30	ns
VIO Above 2.3 V				38	ns
VIO Above 1.8 V				48	ns
CNV Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 3 V				21	ns
VIO Above 2.7 V				27	ns
VIO Above 2.3 V				35	ns
VIO Above 1.8 V				45	ns
CNV High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			50	ns
CNV Low to SCK Rising Edge	t_{CLSCK}	10			ns
DIN Valid Setup Time from SCK Rising Edge	t_{SDIN}	5			ns
DIN Valid Hold Time from SCK Rising Edge	t_{HDIN}	5			ns

[1] See Figure 2 and Figure 3 for load conditions.

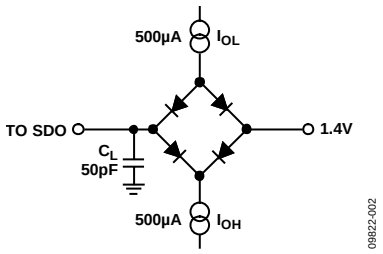


Figure 2. Load Circuit for Digital Interface Timing

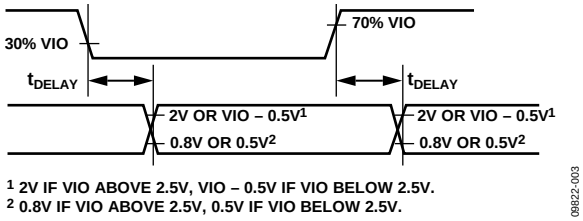


Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
INx, COM[1]	GND − 0.3 V to VDD + 0.3 V or VDD ± 130 mA
REF, REFIN	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VIO to VDD	−0.3 V to VDD + 0.3 V
DIN, CNV, SCK to GND	−0.3 V to VIO + 0.3 V
SDO to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (LFCSP)	47.6°C/W
θ_{JC} Thermal Impedance (LFCSP)	4.4°C/W

[1] See the AD7949 data sheet.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

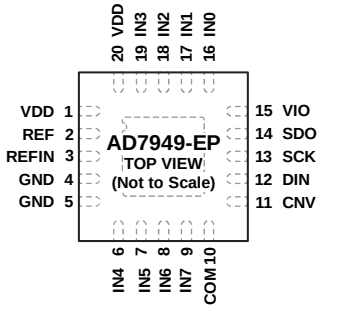


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 20	VDD	P	Power Supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for 2.5 V output, the minimum should be 3.0 V. When using the internal reference for 4.096 V output, the minimum should be 4.5 V.
2	REF	AI/O	Reference Input/Output. See the AD7949 data sheet. When the internal reference is enabled, this pin produces a selectable system reference = 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (4.096 V maximum), useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 µF capacitor connected as close to REF as possible. See the AD7949 data sheet.
3	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. See the AD7949 data sheet. When using the internal reference, the internal unbuffered reference voltage is present and needs decoupling with a 0.1 µF capacitor. When using the internal reference buffer, apply a source between 0.5 V and 4.096 V that is buffered to the REF pin as described above.
4, 5	GND	P	Power Supply Ground.
6 to 9	IN4 to IN7	AI	Channel 4 through Channel 7 Analog Inputs.
10	COM	AI	Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or $V_{REF}/2$ V.
11	CNV	DI	Convert Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held high, the busy indictor is enabled.
12	DIN	DI	Data Input. This input is used for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.
13	SCK	DI	Serial Data Clock Input. This input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion.
14	SDO	DO	Serial Data Output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes, conversion results are twos complement.
15	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
16 to 19	IN0 to IN3	AI	Channel 0 through Channel 3 Analog Inputs.
21 (EPAD)	Exposed Pad (EPAD)	NC	The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane.

[1] AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V to 5.5 V, V_{REF} = 2.5 V to 5 V, VIO = 2.3 V to VDD, unless otherwise noted.

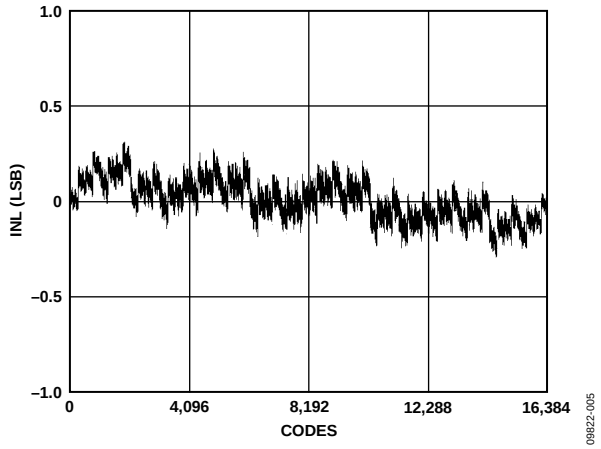


Figure 5. Integral Nonlinearity vs. Code, V_{REF} = VDD = 5 V

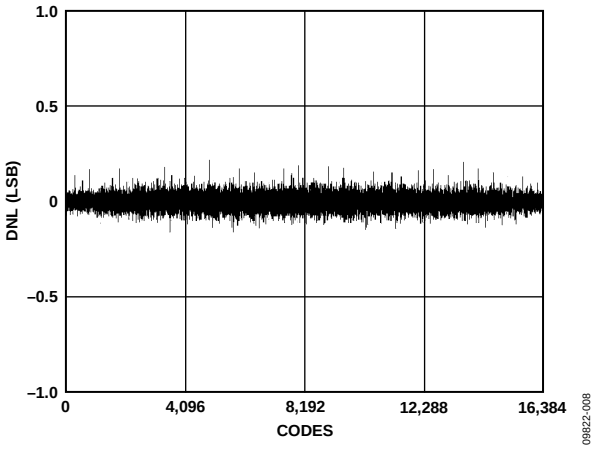


Figure 8. Differential Nonlinearity vs. Code, V_{REF} = VDD = 5 V

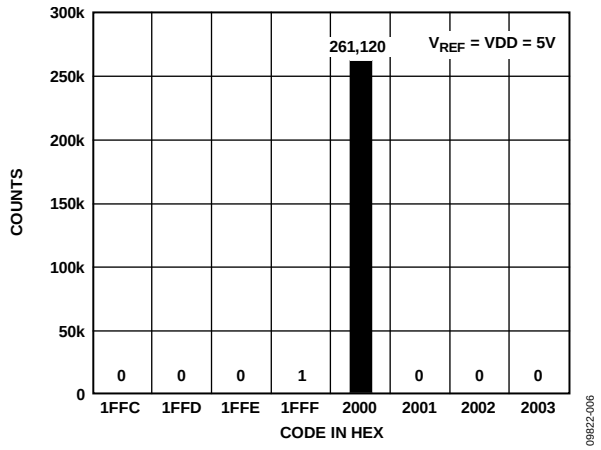


Figure 6. Histogram of a DC Input at Code Center

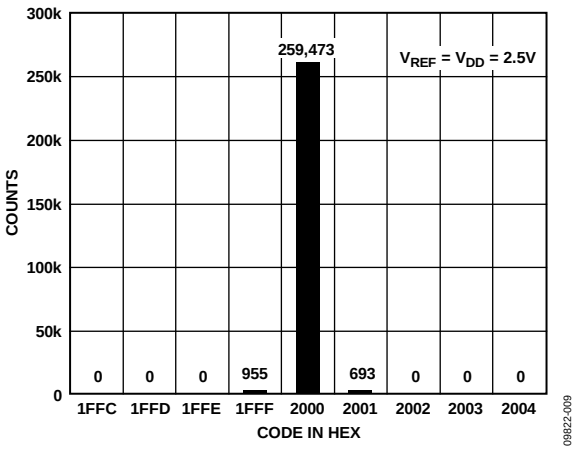


Figure 9. Histogram of a DC Input at Code Center

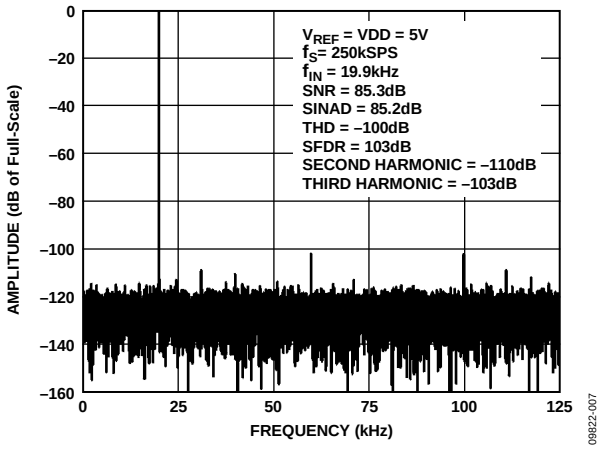


Figure 7. 20 kHz FFT, V_{REF} = VDD = 5 V

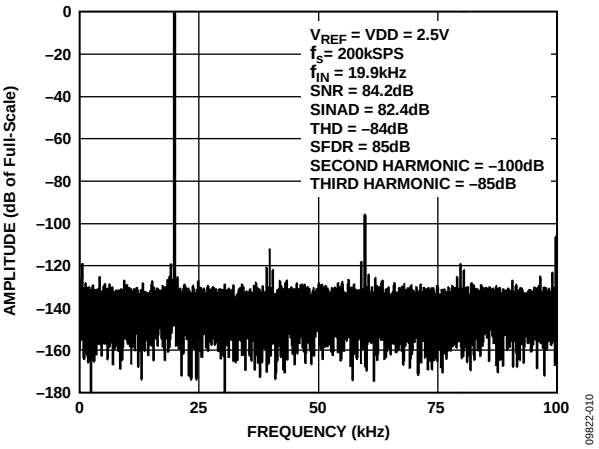


Figure 10. 20 kHz FFT, V_{REF} = VDD = 2.5 V

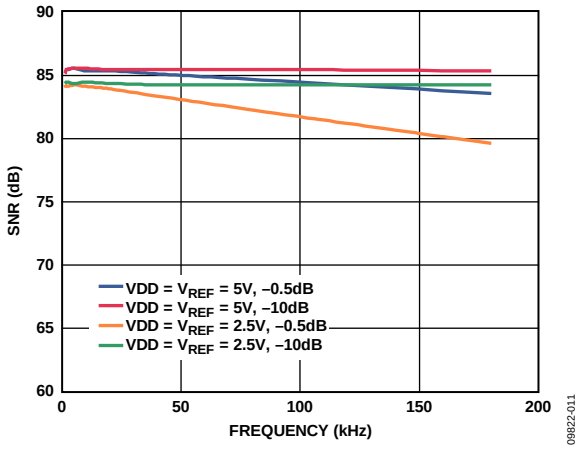


Figure 11. SNR vs. Frequency

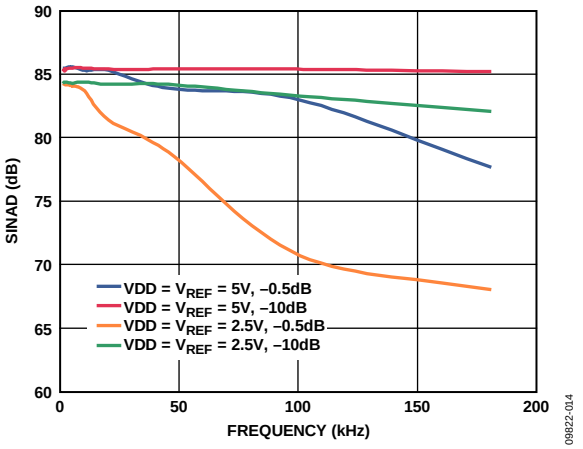


Figure 14. SINAD vs. Frequency

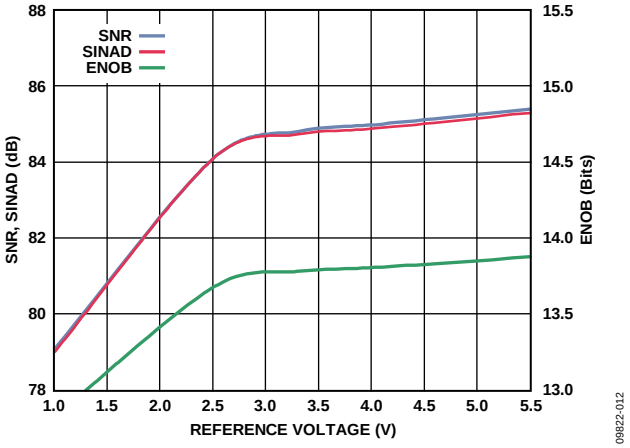


Figure 12. SNR, SINAD, and ENOB vs. Reference Voltage

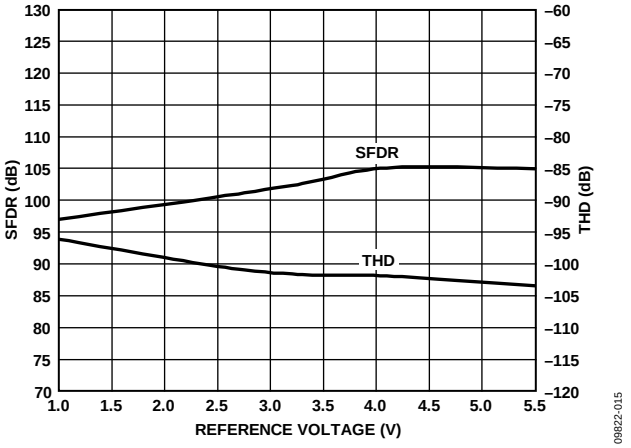


Figure 15. SFDR and THD vs. Reference Voltage

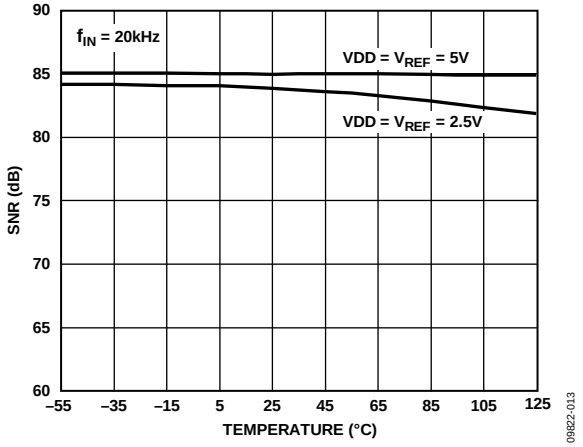


Figure 13. SNR vs. Temperature

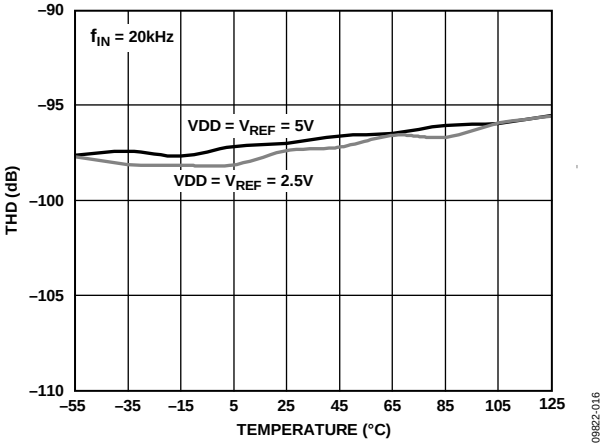


Figure 16. THD vs. Temperature

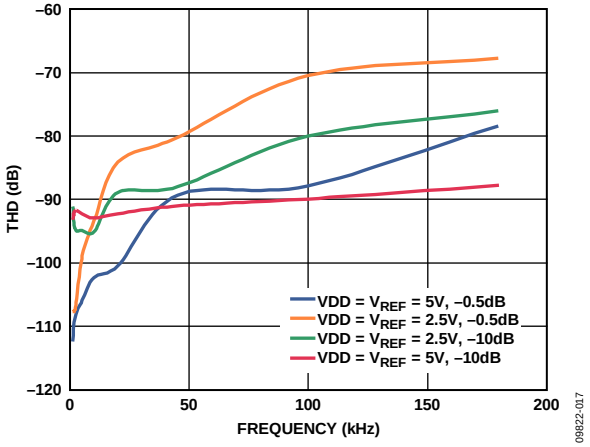


Figure 17. THD vs. Frequency

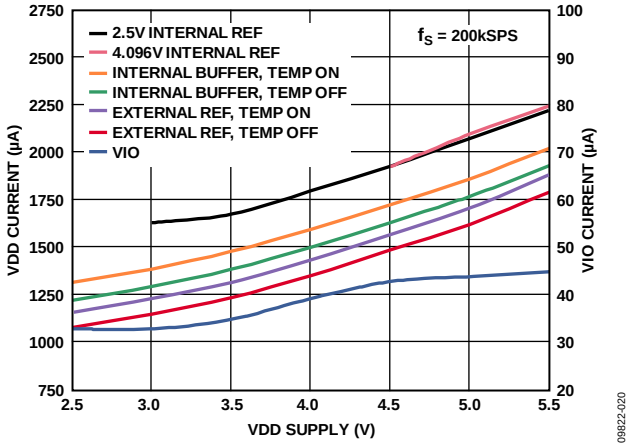


Figure 20. Operating Currents vs. Supply

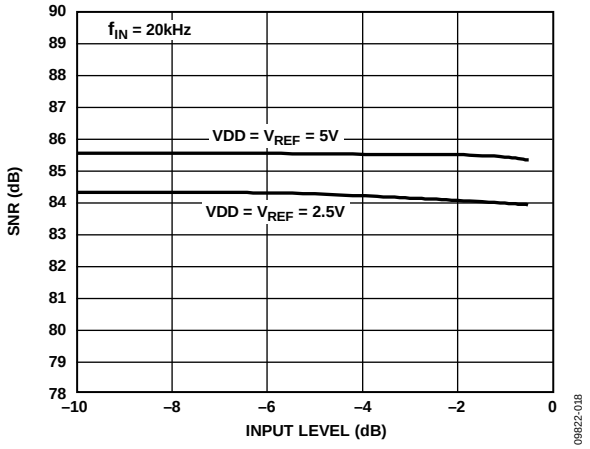


Figure 18. SNR vs. Input Level

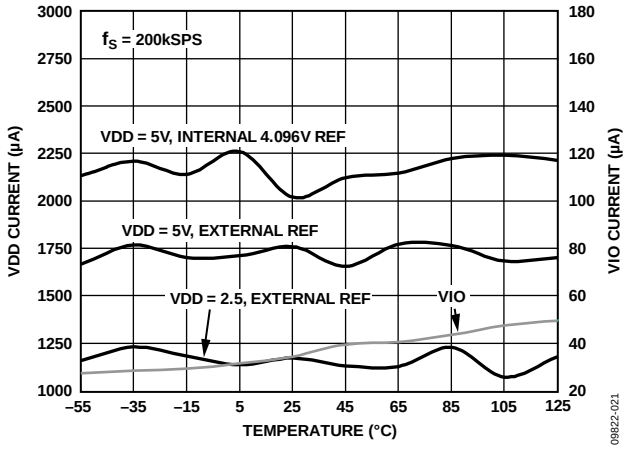


Figure 21. Operating Currents vs. Temperature

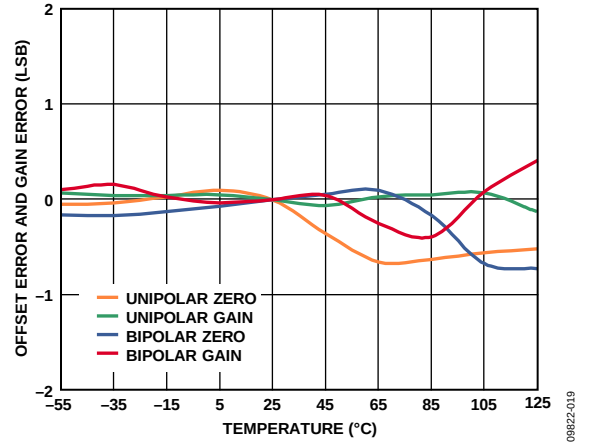
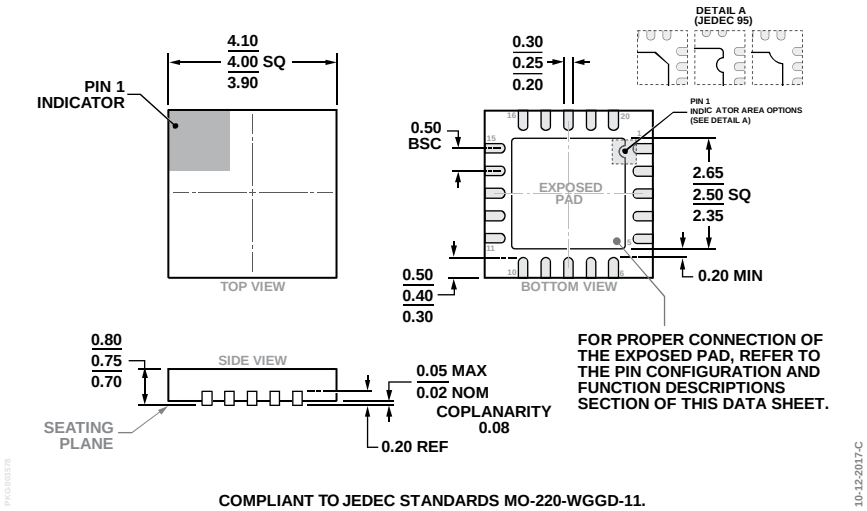


Figure 19. Offset and Gain Errors vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 22. 20-Lead Lead Frame Chip Scale Package (LFCSP)
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD7949SCPZ-EP-RL7	−55°C to +125°C	20-Lead LFCSP, 7″ Tape and Reel	CP-20-10	1,500
AD7949SCPZ-EP-R2	−55°C to +125°C	20-Lead LFCSP, 7″ Tape and Reel	CP-20-10	1,500

[1] Z = RoHS Compliant Part.