This version (17 Jul 2015 09:19) was ***approved*** by LucianS.
The Previously approved version (14 May 2015 00:05) is available.

AD-FMCADC2-EBZ FMC Board

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The AD-FMCADC2-EBZ is a high speed data acquisition board featuring AD9625 single channel ADC at 2500 MSPS, in a FMC form factor which supports the JESD204B high speed serial interface. This board meets most of the FMC specifications in terms of mechanical size, mounting hole locations, and more. For that information, please refer to the FMC specification.

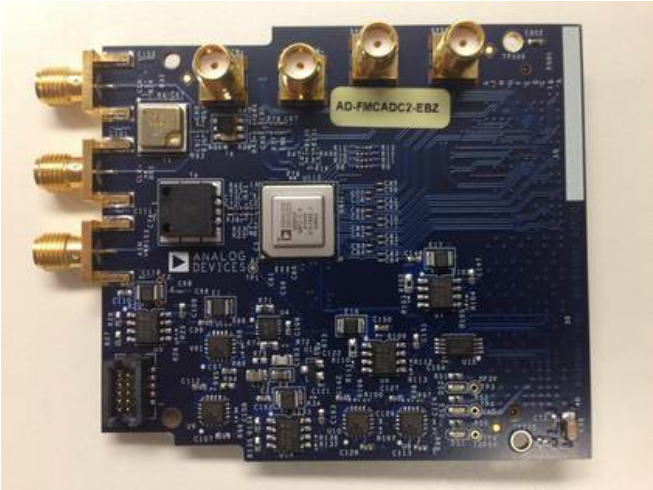
Although this board does meet most of the FMC specifications, it is not meant as a commercial off the shelf (COTS) board. If you want a commercial, ready to integrate product, please refer to one of the many FMC manufacturers.

This board is targeted to use the ADI reference designs that work with Xilinx development systems. ADI provides complete source (HDL and software) to re-create those projects (minus the IP provided by the FPGA vendors, which we use), but may not provide enough info to port this to your custom platform.

Contains

The card contains:

- AD9625 12-bit ADC with sampling speeds of up to 2500 MSPS, with a JESD204B digital interface.
- ADP7104 is a 20V, 500mA, low noise, CMOS LDO
- ADP1753 is a low dropout linear regulators that operate from 1.6 V to 3.6 V and provide up to 800mA of output current.
- ADP2119 is a 2A, 1.2MHz, synchronous step-down DC-to-DC regulator
- ADP1741 is a 2A, low Vin, low dropout, CMOS linear regulator
- ADR280 is a ultralow power high PSRR voltage reference.



Note For Revision C

If you have a revision C board as indicated in etch next to the white scratch pad area of the PCB we recommend writing to the Serial Output Adjust Register. If you are using the reference design this is done for you. Otherwise when you configure the AD9625 it is suggested that you increase the serial output emphasis by writing to register 0x015 bits 5:4 either 10 or 11.

FPGA Code

Xilinx FPGA Code

Eye Scan

Eye scan for this board can be found at jesd_eye_scan.

Linux

- JESD Linux Driver
- AD9625 Linux driver
- ZC706 Linux image
- Linux on the VC707

Specifications

The AD-FMCADC2-EBZ board's primary purpose is to quickly and easily connect to an FMC carrier platform and start collecting data using the AD9625. The board is designed to be easy to use. Out of the box the board will self power and self clock when connected to and FMC carrier. The only other required equipment is your chosen signal source to provide and input signal to “Ain”.

This rapid prototyping board also has 4 vertically mounted SMA connectors. These are labeled SYSREF IN and SYSREF OUT. These are to enable synchronization of multiple AD-FMCADC2-EBZ boards together using characteristics of the JESD204B high speed serial interface between the AD9625 and FPGA.

Clocking

The AD-FMCADC2-EBZ provides multiple options for clocking the AD9625. The default configuration of the board clocks the ADC using an on-board 2.5 GHz, low noise, crystal oscillator. This oscillator is then routed through a wide band transformer producing the differential clock for the ADC.

Alternatively, the oscillator can be disconnected and an external clock source connected by only changing two components on the board. A single ended clock connected to the CLK+ input would then be routed through the transformer in the same way.

Finally, the option exists to connect a differential clock to the board using both the CLK+ and CLK- inputs. Then referencing the schematic make the component changes to directly route the differential input bypassing the transformer.

Front End

The AD-FMCADC2-EBZ uses a passive front end designed for very wide bandwidth. A single ended input needs to be provided to “Ain”. A 500 kHz to 6 GHz broadband balun then converts the input signal to differential.

Layout

Downloads

Rev C

- 02-036007-01-c-1.pdf
- ad-fmcadc2-ebz_gerbers.zip
- 05_036007_c_bom_wiki.xlsx

Rev D

- 02_036007d.pdf
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- 036007_d_bom_wiki.xlsx

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