GaAs, pHEMT, MMIC, Power Amplifier, 20 GHz to 54 GHz

Preliminary Data Sheet

ADL8106XCEZ

FEATURES

Gain: 21 dB typical
Noise Figure: 3.5 dB typical
Output power for 1 dB compression (P1dB): 12 dB typical
Saturated output power (P_{SAT}): 15 dBm typical
Output third-order intercept (IP3): 22 dBm typical
Supply voltage: 3 V at 120 mA
50 Ω matched input/output
Package: 5x5mm SMT

APPLICATIONS

Test instrumentation
Military and space

FUNCTIONAL BLOCK DIAGRAM

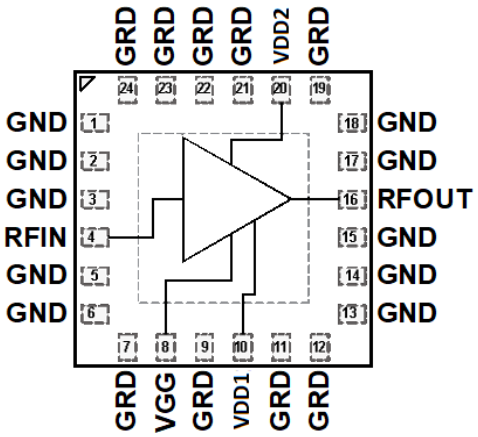

Figure 1.

GENERAL DESCRIPTION

The ADL8106XCEZ is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), distributed power amplifier that operates from 20 GHz to 54 GHz. The ADL8106XCEZ provides 21 dB of gain, 22 dBm output IP3, and 12 dBm of output power at 1 dB gain compression, while requiring 120 mA from a 3 V supply.

Rev. PrA **Document Feedback**

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REVISION HISTORY

ELECTRICAL SPECIFICATIONS

20 GHz TO 54 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 3 V, I_{DD} = 120 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V to 0 V to achieve I_{DD} = 120 mA typical.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			20		54	GHz
GAIN				21		dB
Gain Variation Over Temperature						dB/°C
RETURN LOSS						
Input				14		dB
Output				14		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB			12		dBm
Saturated Output Power	P_{SAT}			15		dBm
Output Third-Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		22		dBm
NOISE FIGURE				3		
TOTAL SUPPLY CURRENT	I_{DD}	V_{DD} = 3 V		120		mA

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

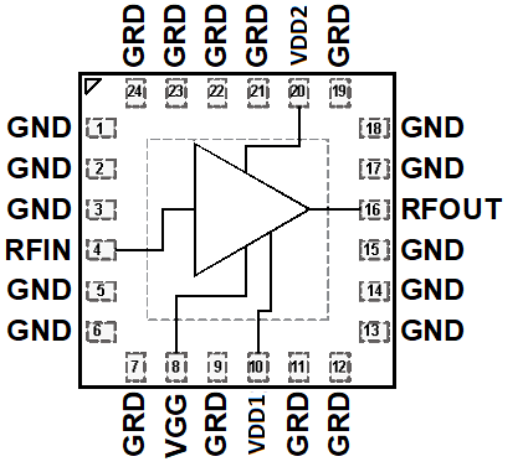


Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pad No.	Mnemonic	Description
1, 2, 3, 5, 6, 7, 9, 11, 12, 13, 14, 15, 17, 18, 19, 21, 22, 23, 24	GND	Ground. The package bottom has an exposed metal pad that must be connected to RF/dc ground.
4	RFIN	RF Input. This pin is ac-coupled and matched to 50 Ω.
10	$V_{DD1,}$	Power Supply Voltage with Integrated RF Choke. Connect dc bias to this pin to provide drain current (I_{DD}).
16	RFOUT	RF Output. This pin is ac-coupled and matched to 50 Ω.
20	$V_{DD2,}$	Power Supply Voltage with Integrated RF Choke. Connect dc bias to this pin to provide drain current (I_{DD}).
8	V_{GG}	Gate Control for Amplifier. Attach bypass capacitors as shown in Figure 5. Adjust this pin to achieve I_{DD} = 120 mA.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

TYPICAL PERFORMANCE CHARACTERISTICS

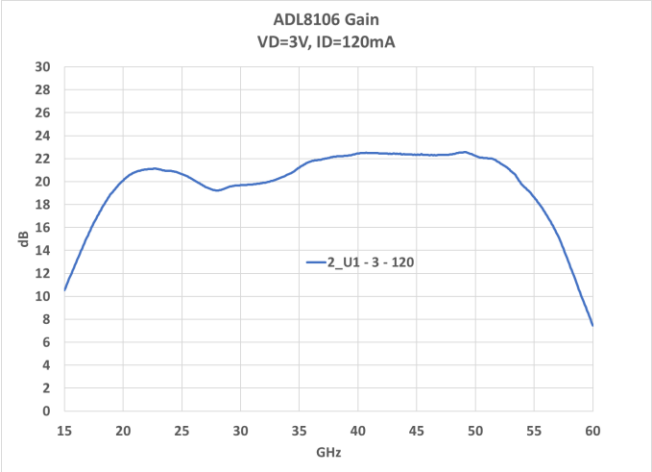


Figure 3. Gain vs. Frequency, Vdd=3V, Idq=120mA

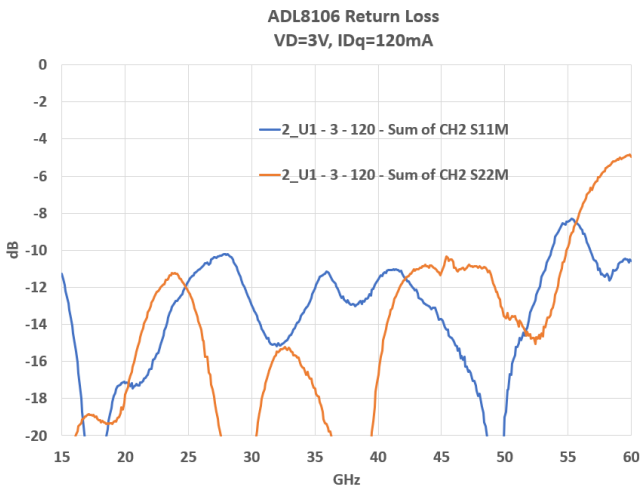


Figure 4. Return Loss vs. Frequency, Vdd=3V, Idq=120mA

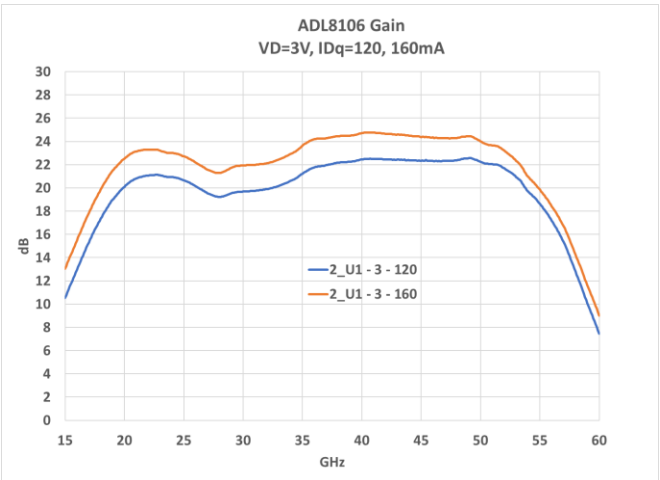


Figure 5. Gain vs. Frequency, Vdd=3V, Idq=120, 160mA

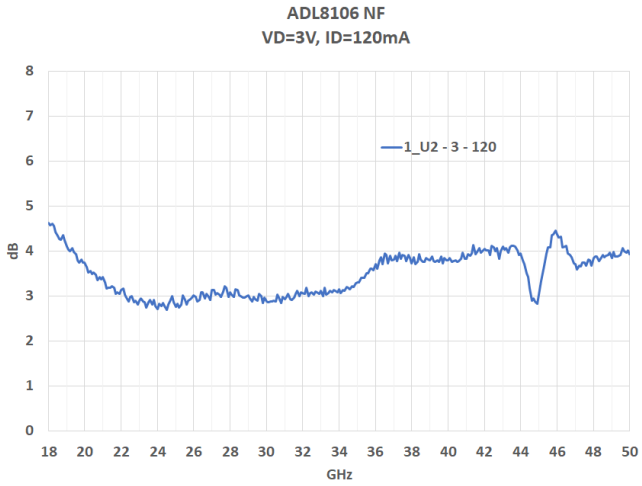


Figure 6. Noise Figure vs. Frequency, Vdd=5V, Idq=120mA

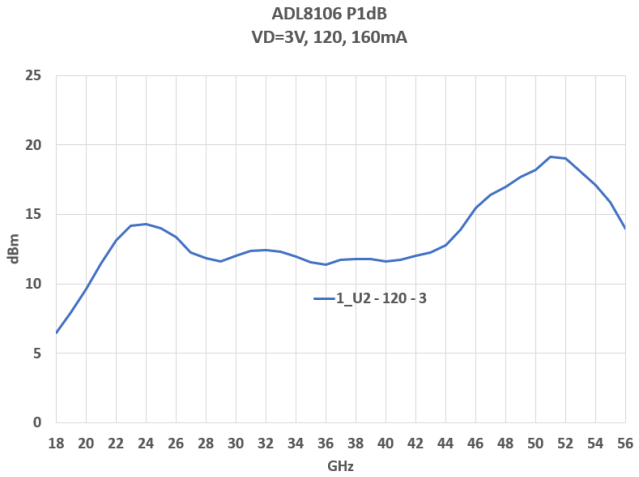


Figure 7. P1dB vs. Frequency, Vdd=3V, Idq=120mA

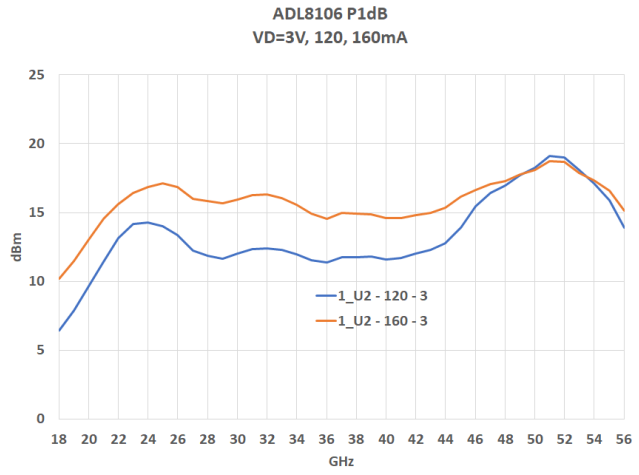


Figure 8. OIP3 vs. Frequency, Vdd=3V, Idq=120, 160mA

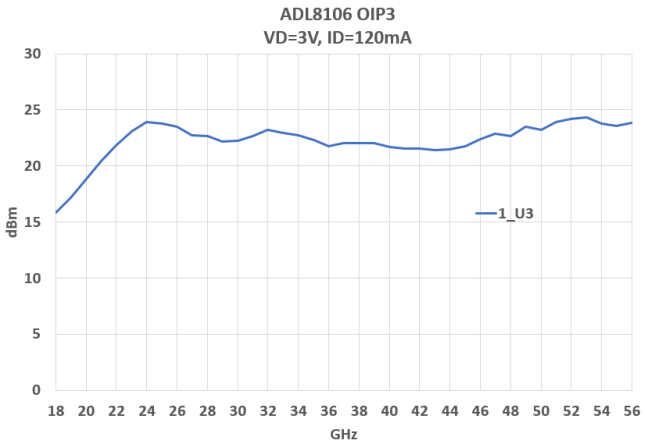


Figure 9. OIP3 vs. Frequency, Vdd=3V, Idq=120mA

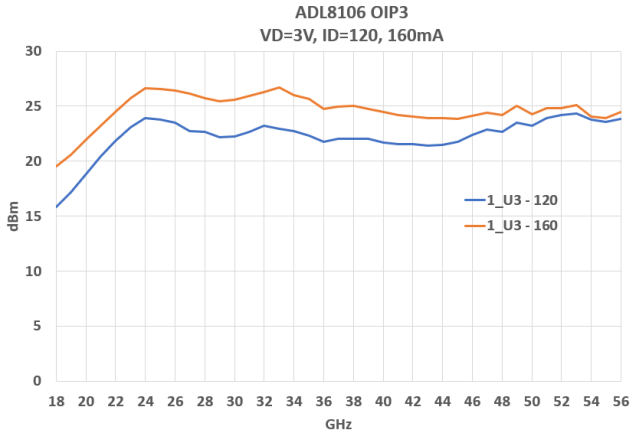
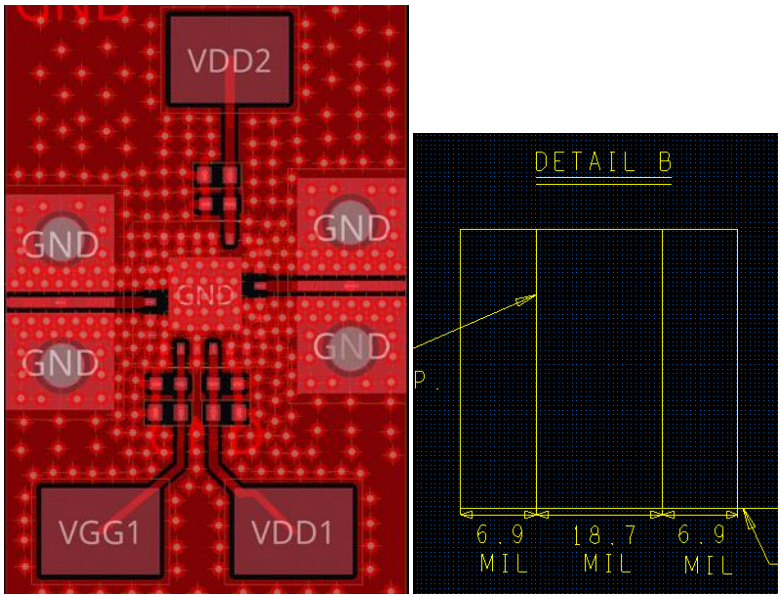


Figure 10. OIP3 vs. Frequency, Vdd=3V, Idq=120, 160mA

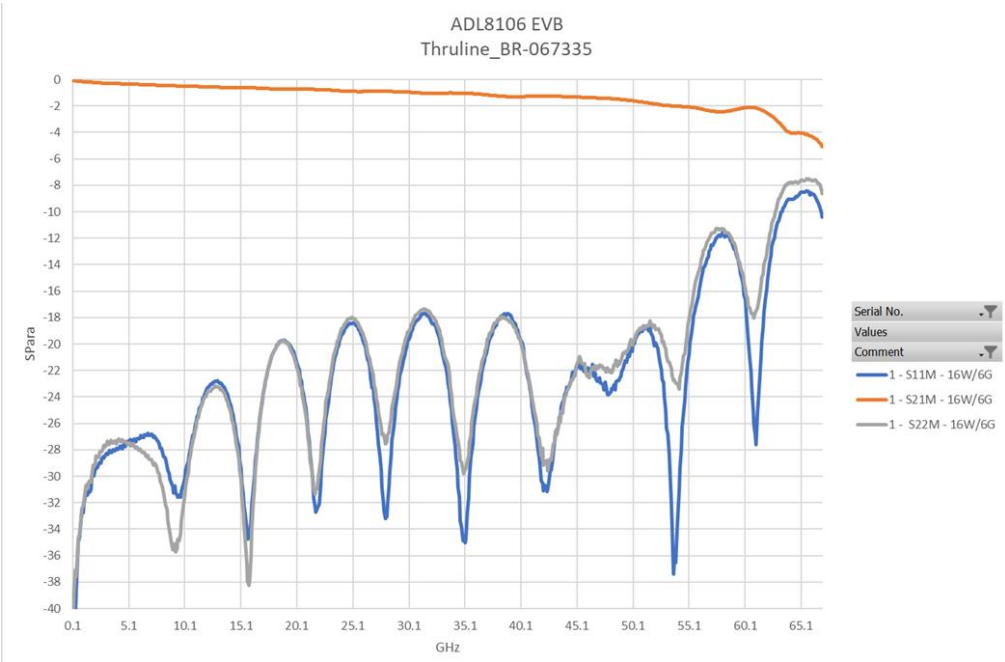
EVAL BOARD SCHEMATIC

Eval Board Via layout shown below. Width and Gap of RF trace shown below: 18.7mil trace, 6.9mil gap. The board material is ROGERS RO4003C 12MIL thick.

No external capacitors are required for ADL8106, they are integrated inside of the package. VGG1 is required to control the current of the amplifier (~-0.5V roughly). VDD1 and VDD2 are required to power the drain of the amplifier (3V nominal).



Eval Board thru path:



APPLICATIONS INFORMATION

The recommended bias sequence during power up is the following:

1. Connect GND.
2. Set V_{GG} to −2 V.
3. Set V_{DD1} & V_{DD2} to 3 V.
4. Increase V_{GG} to achieve a typical quiescent current (I_{DQ}) = 120 mA.
5. Apply the RF signal.

The recommended bias sequence during power down is the following:

1. Turn off the RF signal.
2. Decrease $V_{GG}1$ to −2 V to achieve I_{DQ} = 0 mA.
3. Decrease V_{DD} to 0 V.
4. Increase $V_{GG}1$ to 0 V.

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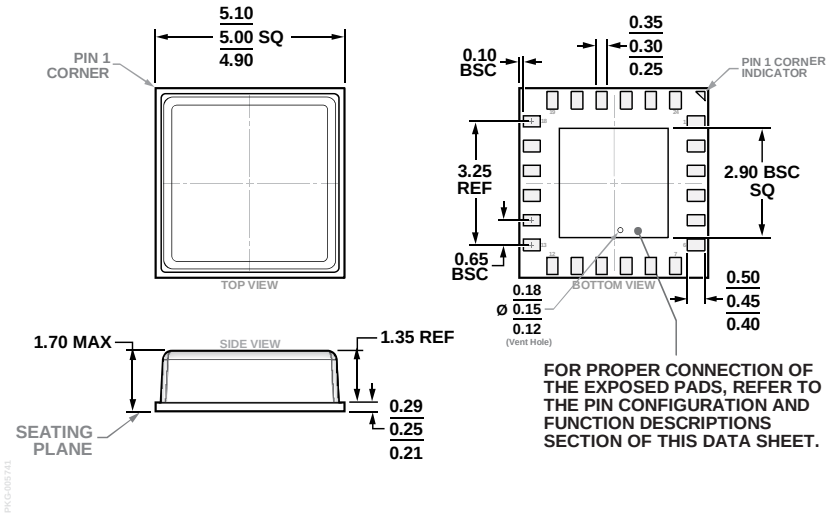
Figure 5. Application Circuit

OUTLINE DIMENSIONS



SOLDERING FOOTPRINT DIMENSIONS
(Dimensions shown in millimeters)

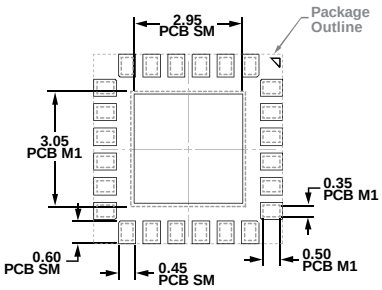


Figure 6. 24-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
5.00 x 5.00 mm Body and 1.70 mm Package Height
(CE-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL8106XCEZ	−40°C to +85°C	MSL3	CE-24-2

[1] The ADL8106XCEZ is RoHS Compliant.

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