300 MHz, 32 × 16 Buffered Analog Crosspoint Switch

ADV3202/ADV3203

FEATURES

- Large, 32 × 16, nonblocking switch array
- G = +1 (ADV3202) or G = +2 (ADV3203) operation
- 32 × 32 pin-compatible version available (ADV3200/ADV3201)
- Single +5 V, dual ±2.5 V, or dual ±3.3 V supply (G = +2)
- Serial programming of switch array
- 2:1 OSD insertion mux per output
- Input sync-tip clamp
- High impedance output disable allows connection of multiple devices with minimal output bus load
- Excellent video performance
  - 60 MHz 0.1 dB gain flatness
  - 0.1% differential gain error (R_L = 150 Ω)
  - 0.1° differential phase error (R_L = 150 Ω)
- Excellent ac performance
  - Bandwidth: >300 MHz
  - Slew rate: >400 V/µs
- Low power: 1 W
- Low all hostile crosstalk: −48 dB @ 5 MHz
- Reset pin allows disabling of all outputs
  - Connected through a capacitor to ground, provides power-on reset capability
- 176-lead exposed pad LQFP package (24 mm × 24 mm)

APPLICATIONS

- CCTV surveillance
- Routing of high speed signals, including
  - Composite video (NTSC, PAL, S, SECAM)
  - RGB and component video routing
  - Compressed video (MPEG, wavelet)
- Video conferencing

FUNCTIONAL BLOCK DIAGRAM

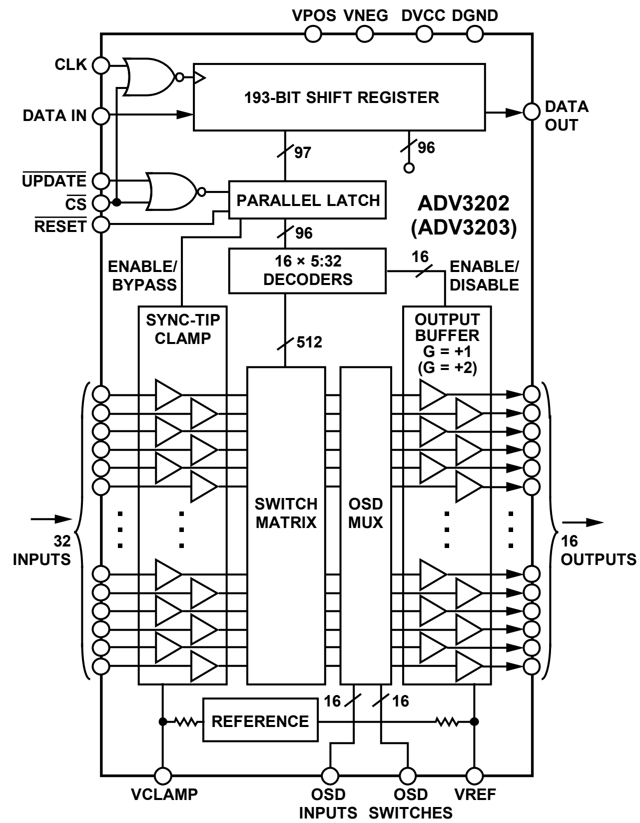

Figure 1.

GENERAL DESCRIPTION

The ADV3202/ADV3203 are 32 × 16 analog crosspoint switch matrices. They feature a selectable sync-tip clamp input for ac-coupled applications and a 2:1 on-screen display (OSD) insertion mux. With −48 dB of crosstalk and −80 dB isolation at 5 MHz, the ADV3202/ADV3203 are useful in many high density routing applications. The 0.1 dB flatness out to 60 MHz makes the ADV3202/ADV3203 ideal for both composite and component video switching.

The 16 independent output buffers of the ADV3202/ADV3203 can be placed into a high impedance state for paralleling cross-point outputs so that off-channels present minimal loading to an output bus if building a larger array. The ADV3202 has a gain of +1 while the ADV3203 has a gain of +2 for ease of use in back-terminated load applications. A single +5 V supply, dual ±2.5 V supplies, or dual ±3.3 V supplies (G = +2) can be used while consuming only 195 mA of idle current with all outputs enabled. The channel switching is performed via a double buffered, serial digital control that can accommodate daisy chaining of several devices.

The ADV3202/ADV3203 are packaged in a 176-lead exposed pad LQFP package (24 mm× 24 mm) and are available over the extended industrial temperature range of −40°C to +85°C.

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TABLE OF CONTENTS

REVISION HISTORY

10/08—Revision 0: Initial Version

SPECIFICATIONS

OSD DISABLED

V_S = ±2.5 V (ADV3202), V_S = ±3.3 V (ADV3203) at T_A = 25°C, G = +1 (ADV3202), G = +2 (ADV3203), R_L = 150 Ω, all configurations, unless otherwise noted.

Table 1.

Parameter	Conditions	ADV3202/ADV3203 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	200 mV p-p		300		MHz
	2 V p-p		120		MHz
Gain Flatness	0.1 dB, 200 mV p-p		60		MHz
	0.1 dB, 2 V p-p		40		MHz
Settling Time	1% , 2 V step		6		ns
Slew Rate	2 V step, peak		400		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL		0.06/0.1		%
Differential Phase Error	NTSC or PAL		0.06/0.03		Degrees
Crosstalk, All Hostile, RTI	f = 5 MHz, R_L = 150 Ω		−48		dB
	R_L = 1 kΩ		−65		dB
	f = 100 MHz, R_L = 150 Ω		−23		dB
	R_L = 1 kΩ		−30		dB
Off Isolation, Input-to-Output	f = 5 MHz, one channel		−80		dB
Input Voltage Noise	0.1 MHz to 50 MHz		25/22		nV/√Hz
DC PERFORMANCE					
Gain Error	Broadcast mode, no load		±0.5	±1.75/±2.2	%
	Broadcast mode		±0.5	±2.2/±2.7	%
Gain Matching	No load, channel-to-channel		±0.5/±0.8	±2.8	%
	Channel-to-channel		±0.5/±0.8	±3.4	%
OUTPUT CHARACTERISTICS					
Output Impedance	DC, enabled		0.15		Ω
	DC, disabled	900/3.2	1000/4		kΩ
Output Capacitance	Disabled		3.7		pF
Output Voltage Range	ADV3202	−1.1 to +1.1	−1.2 to +1.2		V
	ADV3203	−1.5 to +1.5	−1.6 to +2.0		V
	ADV3203, no output load	−1.5 to +1.5	−2.0 to +2.0		V
INPUT CHARACTERISTICS					
Input Offset Voltage			±5	±30	mV
Input Voltage Range	ADV3202	−1.1 to +1.1	−1.2 to +1.2		V
	ADV3203	−0.75 to +0.75	−0.8 to +1.0		V
	ADV3203, no output load	−0.75 to +0.75	−1.0 to +1.0		V
Input Capacitance			3		pF
Input Resistance		1	4		MΩ
Input Bias Current	Sync-tip clamp enabled, V_{IN} = VCLAMP + 0.1 V	0.1	3	12	µA
	Sync-tip clamp enabled, V_{IN} = VCLAMP − 0.1 V	−2.9	−1	−0.25	mA
	Sync-tip clamp disabled	−10	−3		µA
SWITCHING CHARACTERISTICS					
Enable On Time	50% update to 1% settling		50		ns
Switching Time, 2 V Step	50% update to 1% settling		40		ns
Switching Transient (Glitch)	IN00 to IN31, RTI		300		mV p-p

Parameter	Conditions	ADV3202/ADV3203 Min	Typ	Max	Unit
POWER SUPPLIES					
Supply Current	V_{POS} or V_{NEG}, outputs enabled, no load		195/200	220/235	mA
	V_{POS} or V_{NEG}, outputs disabled		120/130	155/165	mA
	D_{VCC}		2.5	3.5	mA
Supply Voltage Range	$V_{POS} - V_{NEG}$		5 ± 10%/ 6.6 ± 10%		V
PSR	V_{NEG}, V_{POS}, f = 1 MHz		−50/−45		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (still air)		−40 to +85		°C
$θ_{JA}$	Operating (still air)		16		°C/W

OSD ENABLED

V_S = ±2.5 V (ADV3202), V_S = ±3.3 V (ADV3203) at T_A = 25°C, G = +1 (ADV3202), G = +2 (ADV3203), R_L = 150 Ω, all configurations, unless otherwise noted.

Table 2.

Parameter	Conditions	ADV3202/ADV3203 Min	Typ	Max	Unit
OSD DYNAMIC PERFORMANCE					
−3 dB Bandwidth	200 mV p-p		170/150		MHz
	2 V p-p		135/130		MHz
Gain Flatness	0.1 dB, 200 mV p-p		35		MHz
	0.1 dB, 2 V p-p		35		MHz
Settling Time	1%, 2 V step		6		ns
Slew Rate	2 V step, peak		400		V/µs
OSD NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC or PAL		0.12/0.35		%
Differential Phase Error	NTSC or PAL		0.06/0.04		Degrees
Input Voltage Noise	0.5 MHz to 50 MHz		27/25		nV/√Hz
OSD DC PERFORMANCE					
Gain Error	No load		±0.1	±2.3/±2.2	%
			±0.1	±2.7	%
OSD INPUT CHARACTERISTICS					
Input Bias Current	Sync-tip clamp disabled	−10	−4		µA
OSD SWITCHING CHARACTERISTICS					
OSD Switch Delay, 2 V Step	50% OSD switch to 1% settling		20		ns
OSD Switching Transient (Glitch)			15/40		mV p-p

TIMING CHARACTERISTICS (SERIAL MODE)

Specifications subject to change without notice.

Table 3.

Parameter	Symbol	Limit Min	Limit Typ	Limit Max	Unit
Serial Data Setup Time	t_1	40			ns
CLK Pulse Width	t_2	50			ns
Serial Data Hold Time	t_3	50			ns
CLK Pulse Separation	t_4	150			ns
CLK to UPDATE Delay	t_5		50	160	ns
UPDATE Pulse Width	t_6	40			ns
CLK to DATA OUT Valid	t_7			130	ns
Propagation Delay, UPDATE to Switch On or Off			50		ns
Data Load Time, CLK = 5 MHz, Serial Mode			38.6		µs
RESET Time			160		ns

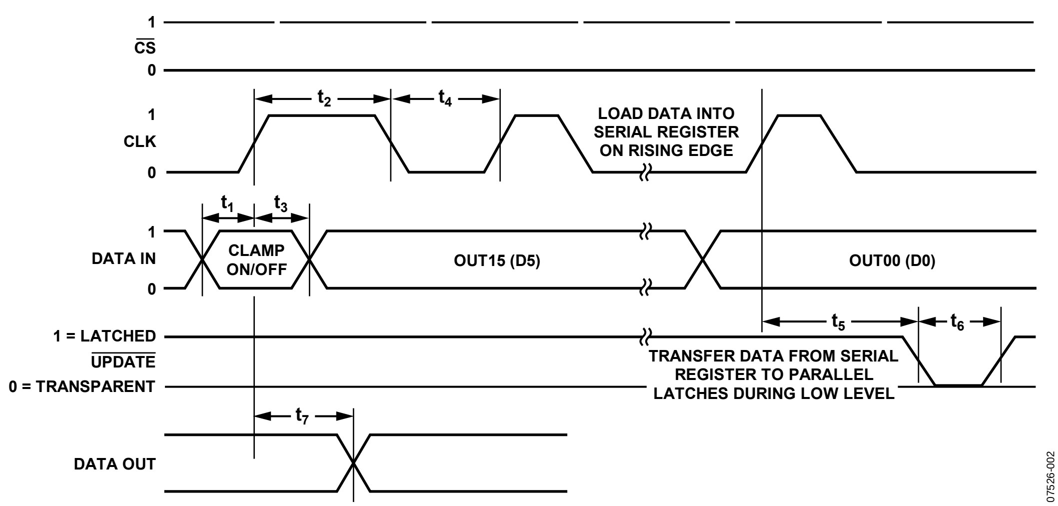


Figure 2. Timing Diagram, Serial Mode

Table 4. Logic Levels, DVCC = 3.3 V

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
RESET, CS, CLK, DATA IN, UPDATE, OSDS	RESET, CS, CLK, DATA IN, UPDATE, OSDS	DATA OUT	DATA OUT	RESET, CS, CLK, DATA IN, UPDATE, OSDS	RESET, CS, CLK, DATA IN, UPDATE, OSDS	DATA OUT	DATA OUT
2.5 V min	0.8 V max	2.7 V min	0.5 V max	0.5 µA typ	−0.5 µA typ	3 mA typ	−3 mA typ

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Supply Voltage (V_{POS} – V_{NEG})	7.5 V
Digital Supply Voltage (DVCC – D_{GND})	6 V
Ground Potential Difference (V_{NEG} – D_{GND})	+0.5 V to –4 V
Maximum Potential Difference	
DVCC – V_{NEG}	9.4 V
Disabled Outputs	
ADV3202 (|V_{OSD} – V_{OUT}|)	<3 V
ADV3203 (|V_{OSD} –(V_{OUT}+V_{REF})/2|)	<3 V
|V_{CLAMP} – V_{INxx}|	6 V
V_{REF} Input Voltage	
ADV3202	V_{POS} – 3.5 V to V_{NEG} + 3.5 V
ADV3203	V_{POS} – 4 V to V_{NEG} + 4 V
Analog Input Voltage	V_{NEG} to V_{POS}
Digital Input Voltage	DVCC
Output Voltage (Disabled Analog Output)	(V_{POS} – 1 V) to (V_{NEG} + 1 V)
Output Short-Circuit Duration	Momentary
Output Short-Circuit Current	45 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
176-Lead LQFP_EP	16	°C/W

POWER DISSIPATION

The ADV3202/ADV3203 are operated with ±2.5 V, +5 V, or ±3.3 V supplies and can drive loads down to 150 Ω, resulting in a large range of possible power dissipations. For this reason, extra care must be taken while derating the operating conditions based on ambient temperature.

Packaged in a 176-lead exposed-pad LQFP, the ADV3202/ ADV3203 junction-to-ambient thermal impedance (θ_{JA}) is 16°C/W. For long-term reliability, the maximum allowed junction temperature of the die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. Figure 3 shows the range of allowed internal die power dissipations that meet these conditions over the −40°C to +85°C ambient temperature range. When using Figure 3, do not include external load power in the maximum power calculation, but do include load current dropped on the die output transistors.

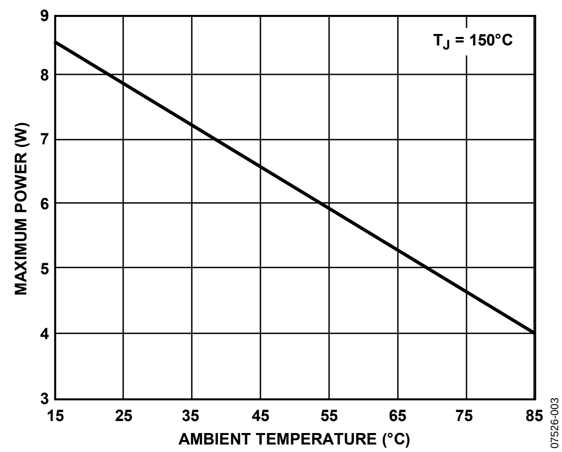
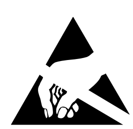


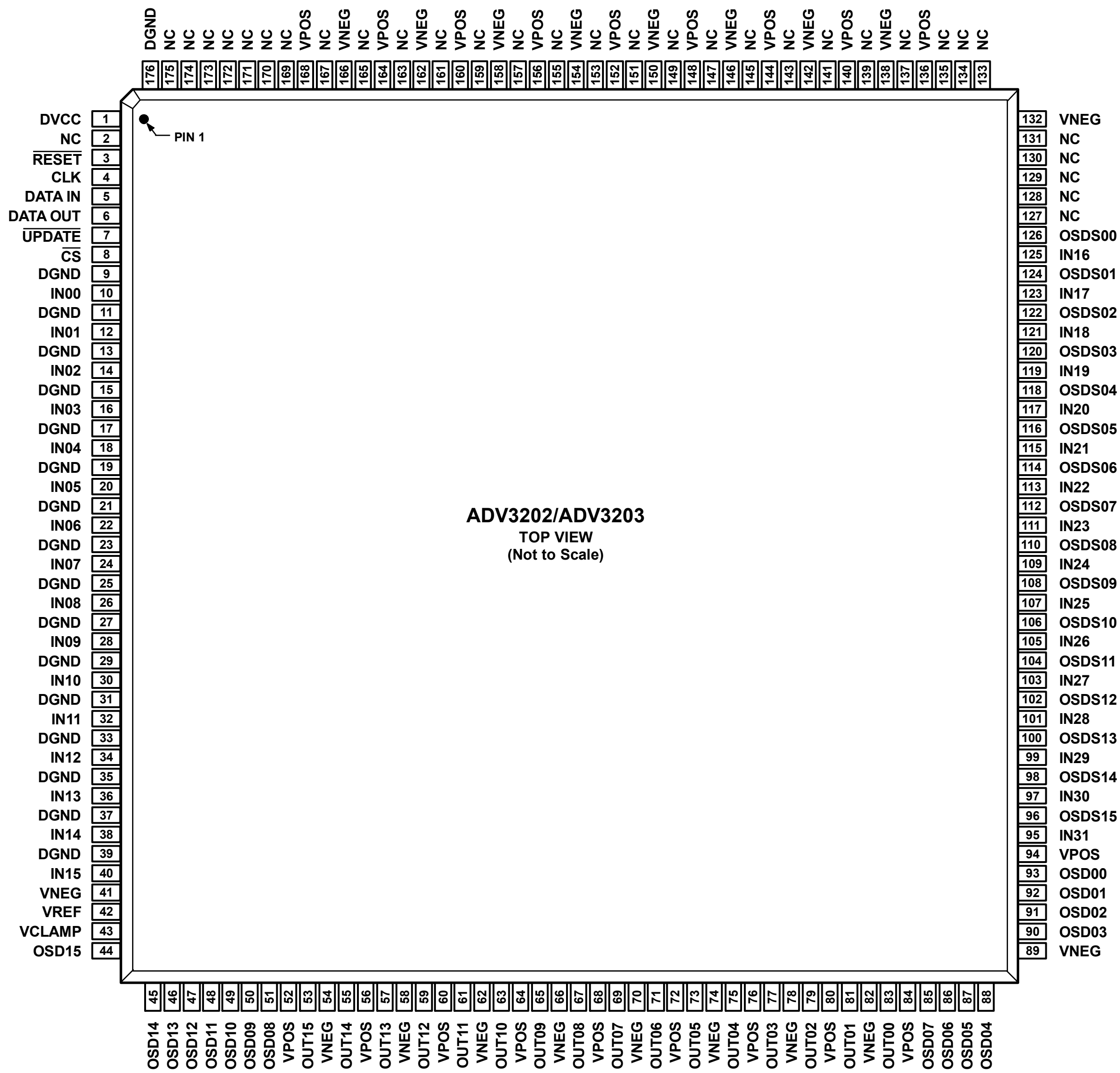
Figure 3. Maximum Die Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT
2. OSDS#: OSD SELECT FOR OUTPUT #
OSD#: OSD VIDEO INPUT FOR OUTPUT #
3. THE EXPOSED PAD SHOULD BE
CONNECTED TO ANALOG GROUND.

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Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin	Mnemonic	Description
1	DVCC	Digital Positive Power Supply.
2	NC	No Connect.
3	$\overline{\text{RESET}}$	Control Pin: 1st and 2nd Rank Reset.
4	CLK	Control Pin: Serial Data Clock.
5	DATA IN	Control Pin: Serial Data In.
6	DATA OUT	Control Pin: Serial Data Out.
7	$\overline{\text{UPDATE}}$	Control Pin: Second Rank Write Strobe.
8	$\overline{\text{CS}}$	Control Pin: Chip Select.
9	DGND	Digital Negative Power Supply.
10	IN00	Input Number 0.
11	DGND	Digital Negative Power Supply.
12	IN01	Input Number 1.
13	DGND	Digital Negative Power Supply.
14	IN02	Input Number 2.
15	DGND	Digital Negative Power Supply.
16	IN03	Input Number 3.
17	DGND	Digital Negative Power Supply.
18	IN04	Input Number 4.
19	DGND	Digital Negative Power Supply.
20	IN05	Input Number 5.
21	DGND	Digital Negative Power Supply.
22	IN06	Input Number 6.
23	DGND	Digital Negative Power Supply.
24	IN07	Input Number 7.
25	DGND	Digital Negative Power Supply.
26	IN08	Input Number 8.
27	DGND	Digital Negative Power Supply.
28	IN09	Input Number 9.
29	DGND	Digital Negative Power Supply.
30	IN10	Input Number 10.
31	DGND	Digital Negative Power Supply.
32	IN11	Input Number 11.
33	DGND	Digital Negative Power Supply.
34	IN12	Input Number 12.
35	DGND	Digital Negative Power Supply.
36	IN13	Input Number 13.
37	DGND	Digital Negative Power Supply.
38	IN14	Input Number 14.
39	DGND	Digital Negative Power Supply.
40	IN15	Input Number 15.
41	VNEG	Analog Negative Power Supply.
42	VREF	Reference Voltage. See the Theory of Operation section for details.
43	VCLAMP	Sync-Tip Clamp Voltage. See the Theory of Operation section for details.
44	OSD15	OSD Input Number 15.
45	OSD14	OSD Input Number 14.
46	OSD13	OSD Input Number 13.
47	OSD12	OSD Input Number 12.
48	OSD11	OSD Input Number 11.
49	OSD10	OSD Input Number 10.
50	OSD09	OSD Input Number 9.
51	OSD08	OSD Input Number 8.
52	VPOS	Analog Positive Power Supply.
53	OUT15	Output Number 15.
54	VNEG	Analog Negative Power Supply.
55	OUT14	Output Number 14.
56	VPOS	Analog Positive Power Supply.
57	OUT13	Output Number 13.
58	VNEG	Analog Negative Power Supply.
59	OUT12	Output Number 12.
60	VPOS	Analog Positive Power Supply.
61	OUT11	Output Number 11.
62	VNEG	Analog Negative Power Supply.
63	OUT10	Output Number 10.
64	VPOS	Analog Positive Power Supply.
65	OUT09	Output Number 9.
66	VNEG	Analog Negative Power Supply.
67	OUT08	Output Number 8.
68	VPOS	Analog Positive Power Supply.
69	OUT07	Output Number 7.
70	VNEG	Analog Negative Power Supply.
71	OUT06	Output Number 6.
72	VPOS	Analog Positive Power Supply.
73	OUT05	Output Number 5.
74	VNEG	Analog Negative Power Supply.
75	OUT04	Output number 4.
76	VPOS	Analog Positive Power Supply.
77	OUT03	Output Number 3.
78	VNEG	Analog Negative Power Supply.
79	OUT02	Output Number 2.
80	VPOS	Analog Positive Power Supply.
81	OUT01	Output Number 1.
82	VNEG	Analog Negative Power Supply.
83	OUT00	Output Number 0.
84	VPOS	Analog Positive Power Supply.
85	OSD07	OSD Input Number 7.
86	OSD06	OSD Input Number 6.
87	OSD05	OSD Input Number 5.
88	OSD04	OSD Input Number 4.
89	VNEG	Analog Negative Power Supply.
90	OSD03	OSD Input Number 3.
91	OSD02	OSD Input Number 2.
92	OSD01	OSD Input Number 1.
93	OSD00	OSD Input Number 0.
94	VPOS	Analog Positive Power Supply.
95	IN31	Input Number 31.
96	OSDS15	Control Pin: OSD Select Number 15.
97	IN30	Input Number 30.
98	OSDS14	Control Pin: OSD Select Number 14.
99	IN29	Input Number 29.
100	OSDS13	Control Pin: OSD Select Number 13.

Pin	Mnemonic	Description
101	IN28	Input Number 28.
102	OSDS12	Control Pin: OSD Select Number 12.
103	IN27	Input Number 27.
104	OSDS11	Control Pin: OSD Select Number 11.
105	IN26	Input Number 26.
106	OSDS10	Control Pin: OSD Select Number 10.
107	IN25	Input Number 25.
108	OSDS09	Control Pin: OSD Select Number 9.
109	IN24	Input Number 24.
110	OSDS08	Control Pin: OSD Select Number 8.
111	IN23	Input Number 23.
112	OSDS07	Control Pin: OSD Select Number 7.
113	IN22	Input Number 22.
114	OSDS06	Control Pin: OSD Select Number 6.
115	IN21	Input Number 21.
116	OSDS05	Control Pin: OSD Select Number 5.
117	IN20	Input Number 20.
118	OSDS04	Control Pin: OSD Select Number 4.
119	IN19	Input Number 19.
120	OSDS03	Control Pin: OSD Select Number 3.
121	IN18	Input Number 18.
122	OSDS02	Control Pin: OSD Select Number 2.
123	IN17	Input Number 17.
124	OSDS01	Control Pin: OSD Select Number 1.
125	IN16	Input Number 16.
126	OSDS00	Control Pin: OSD Select Number 0.
127	NC	No Connect.
128	NC	No Connect.
129	NC	No Connect.
130	NC	No Connect.
131	NC	No Connect.
132	VNEG	Analog Negative Power Supply.
133	NC	No Connect.
134	NC	No Connect.
135	NC	No Connect.
136	VPOS	Analog Positive Power Supply.
137	NC	No Connect.
138	VNEG	Analog Negative Power Supply.
139	NC	No Connect.

Pin	Mnemonic	Description
140	VPOS	Analog Positive Power Supply.
141	NC	No Connect.
142	VNEG	Analog Negative Power Supply.
143	NC	No Connect.
144	VPOS	Analog Positive Power Supply.
145	NC	No Connect.
146	VNEG	Analog Negative Power Supply.
147	NC	No Connect.
148	VPOS	Analog Positive Power Supply.
149	NC	No Connect.
150	VNEG	Analog Negative Power Supply.
151	NC	No Connect.
152	VPOS	Analog Positive Power Supply.
153	NC	No Connect.
154	VNEG	Analog Negative Power Supply.
155	NC	No Connect.
156	VPOS	Analog Positive Power Supply.
157	NC	No Connect.
158	VNEG	Analog Negative Power Supply.
159	NC	No Connect.
160	VPOS	Analog Positive Power Supply.
161	NC	No Connect.
162	VNEG	Analog Negative Power Supply.
163	NC	No Connect.
164	VPOS	Analog Positive Power Supply.
165	NC	No Connect.
166	VNEG	Analog Negative Power Supply.
167	NC	No Connect.
168	VPOS	Analog Positive Power Supply.
169	NC	No Connect.
170	NC	No Connect.
171	NC	No Connect.
172	NC	No Connect.
173	NC	No Connect.
174	NC	No Connect.
175	NC	No Connect.
176	DGND	Digital Negative Power Supply.
	EPAD (exposed pad)	Connect to analog ground.

TRUTH TABLE AND LOGIC DIAGRAM

Table 8. Operation Truth Table

$\overline{CS}$	$\overline{UPDATE}$	CLK	DATA INPUT	DATA OUTPUT	$\overline{RESET}$	Operation/Comment
X	X	X	X	X	0	Asynchronous reset. All outputs are disabled; the 193-bit shift register is reset to all 0s.
0	1	↑	$Data_i$ [1]	$Data_{i-193}$	1	The data on the serial DATA IN line is loaded into the serial register. The first bit clocked into the serial register appears at DATA OUT 193 clock cycles later.
0	0	X	X	X	1	Switch matrix update. Data in the 193-bit shift register transfers into the parallel latches that control the switch array and sync-tip clamps.
1	X	X	X	X	1	Chip is not selected. No change in logic.

[1] $Data_i$: serial data.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±2.5 V (ADV3202), V_S = ±3.3 V (ADV3203) at T_A = 25°C, R_L = 150 Ω.

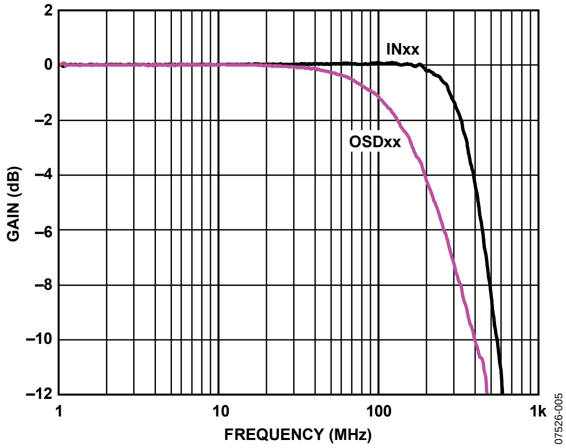

Figure 5. ADV3202 Small Signal Frequency Response, 200 mV p-p

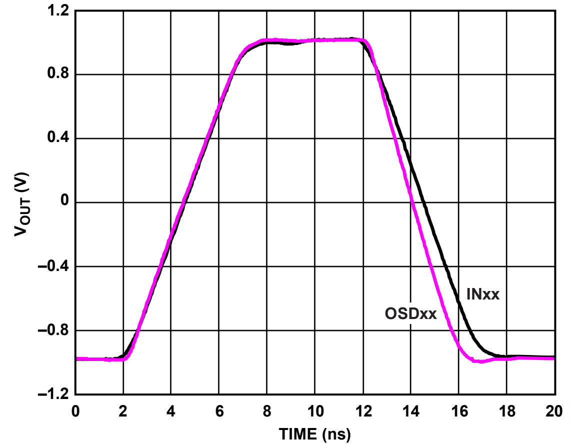

Figure 8. ADV3202 Large Signal Pulse Response, 2 V p-p

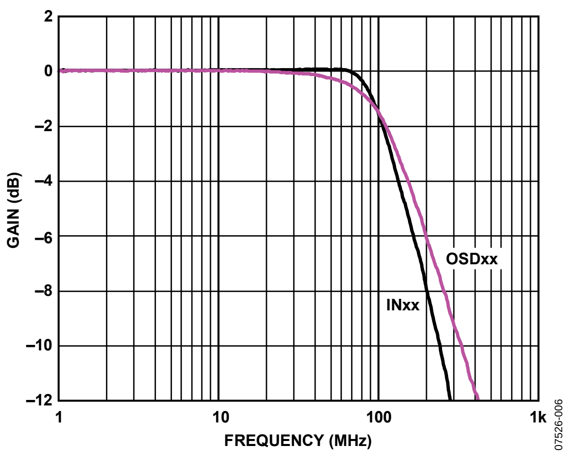

Figure 6. ADV3202 Large Signal Frequency Response, 2 V p-p

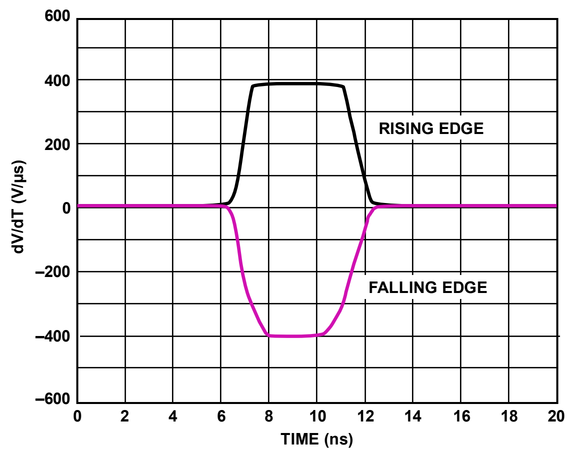

Figure 9. ADV3202 Slew Rate

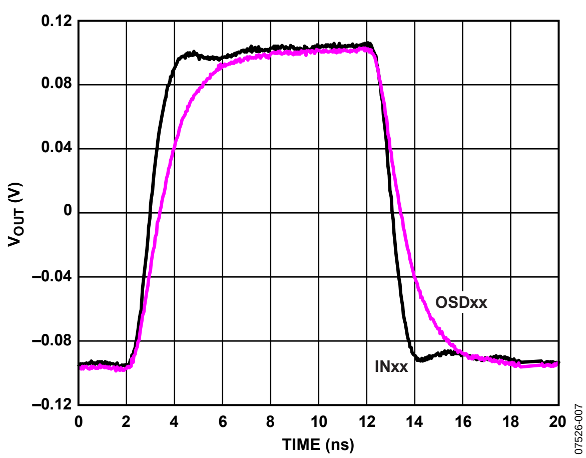

Figure 7. ADV3202 Small Signal Pulse Response, 200 mV p-p

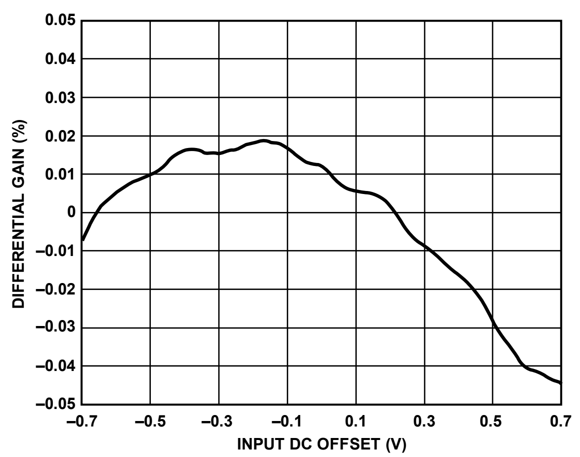

Figure 10. ADV3202 Differential Gain, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

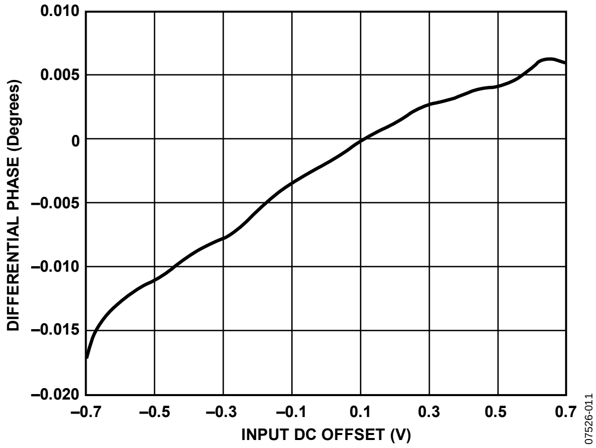

Figure 11. ADV3202 Differential Phase, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

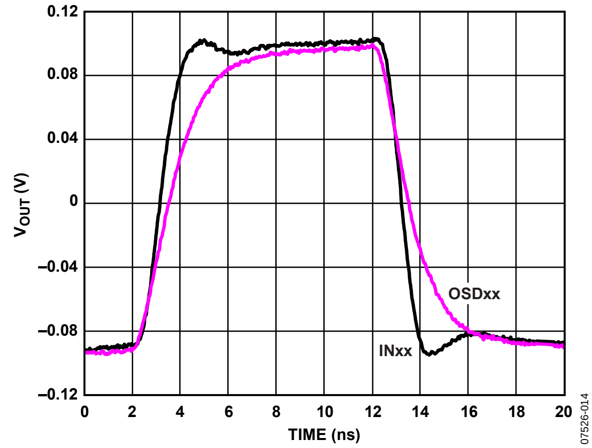

Figure 14. ADV3203 Small Signal Pulse Response, 200 mV p-p

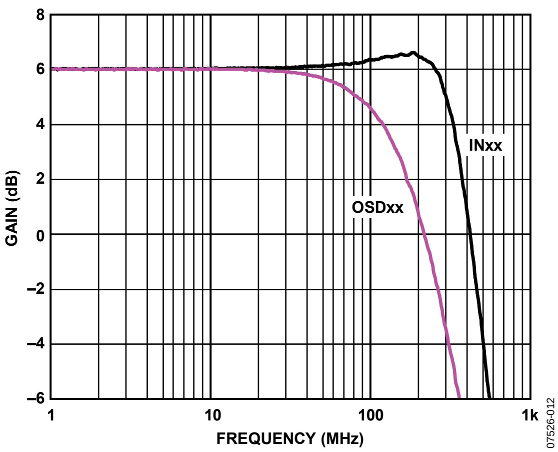

Figure 12. ADV3203 Small Signal Frequency Response, 200 mV p-p

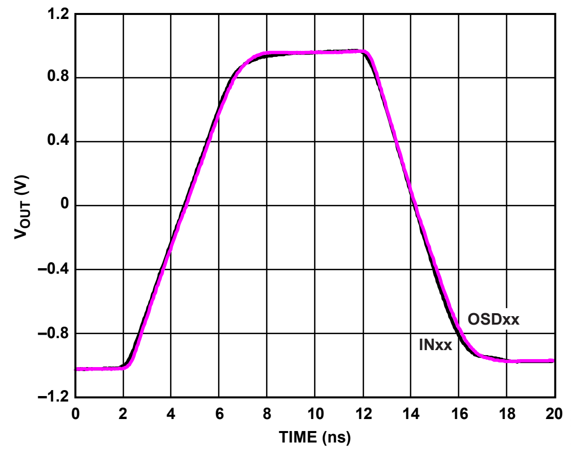

Figure 15. ADV3203 Large Signal Pulse Response, 2 V p-p

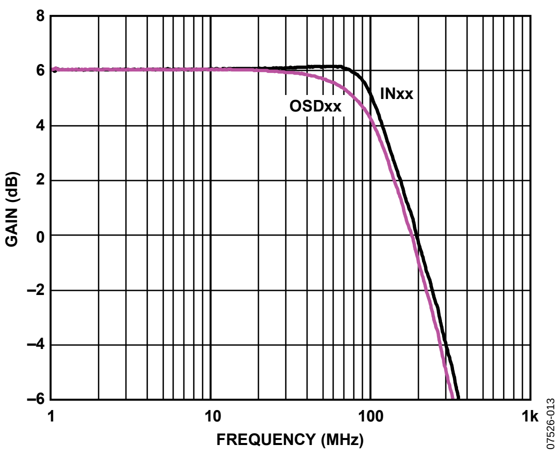

Figure 13. ADV3203 Large Signal Frequency Response, 2 V p-p

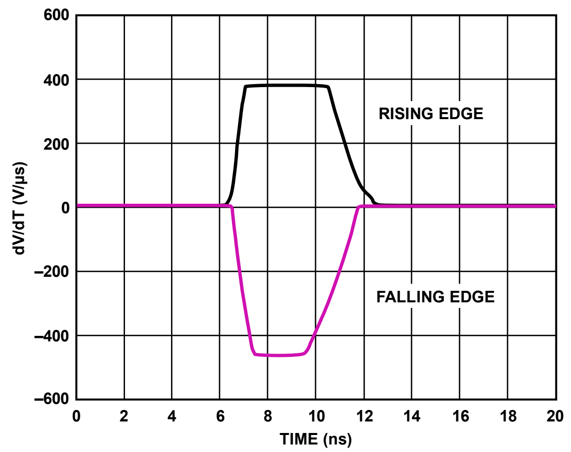

Figure 16. ADV3203 Slew Rate

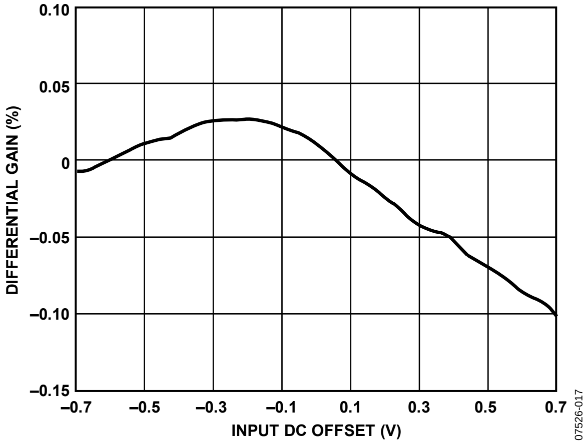

Figure 17. ADV3203 Differential Gain, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

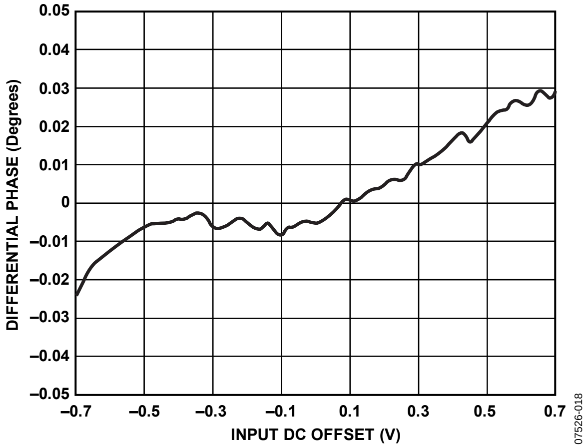

Figure 18. ADV3203 Differential Phase, Carrier Frequency = 3.58 MHz, Subcarrier Amplitude = 300 mV p-p

THEORY OF OPERATION

The ADV3202/ADV3203 are single-ended crosspoint arrays with 16 outputs, each of which can be connected to any one of 32 inputs.The 32 switchable input stages are connected to each output buffer to form 32-to-1 multiplexers. There are 16 of these multiplexers, each with its inputs wired in parallel, for a total array of 512 stages forming a multicast-capable crosspoint switch. In addition to connecting to any of the nominal inputs (INxx), each output can also be connected to an associated OSD input through an additional 2-to-1 multiplexer at each output. This 2-to-1 multiplexer switches between the output of the 32-to-1 multiplexer and the OSD input.

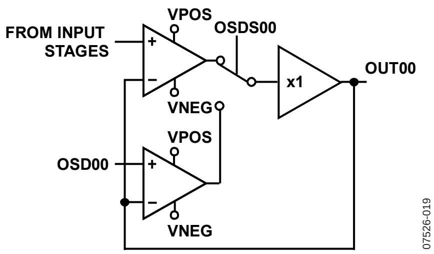

Figure 19. Conceptual Diagram of Single Output Channel, G = +1 (ADV3202)

Decoding logic for each output selects one (or none) of the input stages to drive the output stage. The enabled input stage drives the output stage, which is configured as a unity-gain amplifier in the ADV3202 (see Figure 19). In the ADV3203, an internal resistive feedback network and reference buffer provide for a total output stage gain of +2 (see Figure 20). The input voltage to the reference buffer is the VREF pin. This voltage is common for the entire chip and needs to be driven with a low impedance to avoid crosstalk.

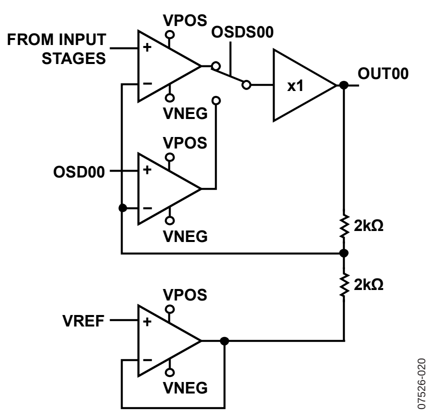

Figure 20. Conceptual Diagram of Single Output Channel, G = +2 (ADV3203)

Each input to the ADV3202/ADV3203 is buffered by a receiver. The purpose of this receiver is to provide overvoltage protection for the input stages by limiting signal swing. In the ADV3202, the output of the receiver is limited to ±1.2 V about VREF, while in the ADV3203, the signal swing is limited to ±1.2 V about midsupply. This receiver is configured as a voltage feedback unity-gain amplifier. Excess loop gain bandwidth product reduces the effect of the closed-loop gain on the bandwidth of the device. In addition to a receiver, each input also has a sync-tip clamp for use in ac-coupled applications. This clamp is either enabled or disabled according to the 193rd serial data bit. When enabled, the clamp forces the lowest video voltage to the voltage on the VCLAMP pin. The VCLAMP pin is common for the entire chip and needs to be driven with a low impedance to avoid crosstalk.

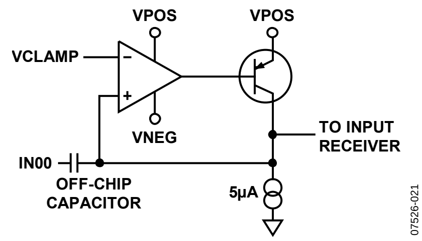

Figure 21. Conceptual Diagram of Sync-Tip Clamp in an AC-Coupled Application

The output stage of the ADV3202/ADV3203 is designed for low differential gain and phase error when driving composite video signals. It also provides slew current for fast pulse response when driving component video signals.

The outputs of the ADV3202/ADV3203 can be disabled to minimize on-chip power dissipation. When disabled, a series of internal amplifiers drive internal nodes such that a wideband high impedance is presented at the disabled output, even while the output bus is under large signal swings. (In the ADV3203, there is 4 kΩ of resistance terminated to the VREF voltage by the reference buffer). This high impedance allows multiple ICs to be bussed together without additional buffering. Care must be taken to reduce output capacitance, which results in more overshoot and frequency domain peaking. In addition, when the outputs are disabled and driven externally, the voltage applied to them should not exceed the valid output swing range for the ADV3202/ADV3203 to keep these internal amplifiers in their linear range of operation. Applying excess voltage to the disabled outputs can cause damage to the ADV3202/ADV3203 and should be avoided (see the Absolute Maximum Ratings section for guidelines).

The internal connection of the ADV3202/ADV3203 is controlled by a TTL-compatible logic interface. Serial loading into a first rank of latches preprograms each output. A global update signal moves the programming data into the second rank of latches, simultaneously updating all outputs. A serial out pin allows devices to be daisy chained together for single pin programming of multiple ICs. A power-on reset pin is available to prevent bus conflicts by disabling all outputs.

The ADV3202 can operate on a single +5 V supply, powering both the signal path (with the VPOS/VNEG supply pins) and the control logic interface (with the VDD/DGND supply pins). However, to easily interface to ground referenced video signals, split supply operation is possible with ±2.5 V. (The ADV3203 is intended to operate on ±3.3 V.) In the case of split supplies, a flexible logic interface allows the control logic supplies (VDD/DGND) to be run off +3.3 V/0 V to +5 V/0 V while the core remains on split supplies.

APPLICATIONS INFORMATION

PROGRAMMING

The ADV3202/ADV3203 are programmed serially through a 193-bit serial word that updates the matrix and the state of the sync-tip clamps each time the part is programmed.

Serial Programming Description

The serial programming mode uses the CLK, DATA IN, UPDATE, and CS device pins. The first step is to assert a low on CS to select the device for programming. The UPDATE signal should be high during the time that data is shifted into the serial port of the device. Although the data still shifts in when UPDATE is low, the transparent, asynchronous latches allow the shifting data to reach the matrix. This causes the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATA IN is clocked in at every rising edge of CLK. A total of 193 bits must be shifted in to complete the programming. For each of the 16 outputs, there are five bits (D0 to D4) that determine the source of its input followed by one bit (D5) that determines the enabled state of the output. If D5 is low (output disabled), the five associated bits (D0 to D4) do not matter because no input is switched to that output. These comprise the first 96 bits of DATA IN. The remaining 96 bits of DATA IN should be set to zero. If a string of 96 zeros is not suffixed to the first 96 bits of DATA IN, a certain test mode is employed that can cause the device to draw up to 30% more current. The last bit, Bit 193, is used to enable or disable the sync-tip clamps. If Bit 193 is low, the sync-tip clamps are disabled; otherwise, they are enabled.

The sync-tip clamp bit is shifted in first, followed by the most significant output address data (OUT15). The enable bit (D5) is shifted in first, followed by the input address (D4 to D0) entered sequentially with D4 first and D0 last. Each remaining output is programmed sequentially, until the least significant output address data is shifted in. At this point, UPDATE can be taken low, which causes the programming of the device according to the data that was just shifted in. The UPDATE latches are asynchronous and when UPDATE is low, they are transparent.

If more than one ADV3202/ADV3203 device is to be serially programmed in a system, the DATA OUT signal from one device can be connected to the DATA IN of the next device to form a serial chain. All of the CLK and UPDATE pins should be connected in parallel and operated as described previously. The serial data is input to the DATA IN pin of the first device of the chain, and it ripples through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence is 193 bits times the number of devices in the chain.

Reset

When powering up the ADV3200/ADV3201, it is often useful to have the outputs come up in the disabled state. The RESET pin, when taken low, causes all outputs to be disabled. After power-up, the UPDATE pin should be driven high prior to raising RESET.

Because the data in the shift register is random after power-up, it should not be used to program the matrix, or the matrix may enter unknown states. To prevent this, do not apply a logic low signal to UPDATE initially after power-up. The shift register should first be loaded with data and UPDATE then taken low to program the device.

The RESET pin has a 25 kΩ pull-up resistor to DVCC that can be used to create a simple power-on reset circuit. A capacitor from RESET to ground holds RESET low for some time while the rest of the device stabilizes. The low condition causes all the outputs to be disabled. The capacitor then charges through the pull-up resistor to the high state, thus allowing full programming capability of the device.

The CS pin has a 25 kΩ pull-down resistor to ground.

OUTLINE DIMENSIONS

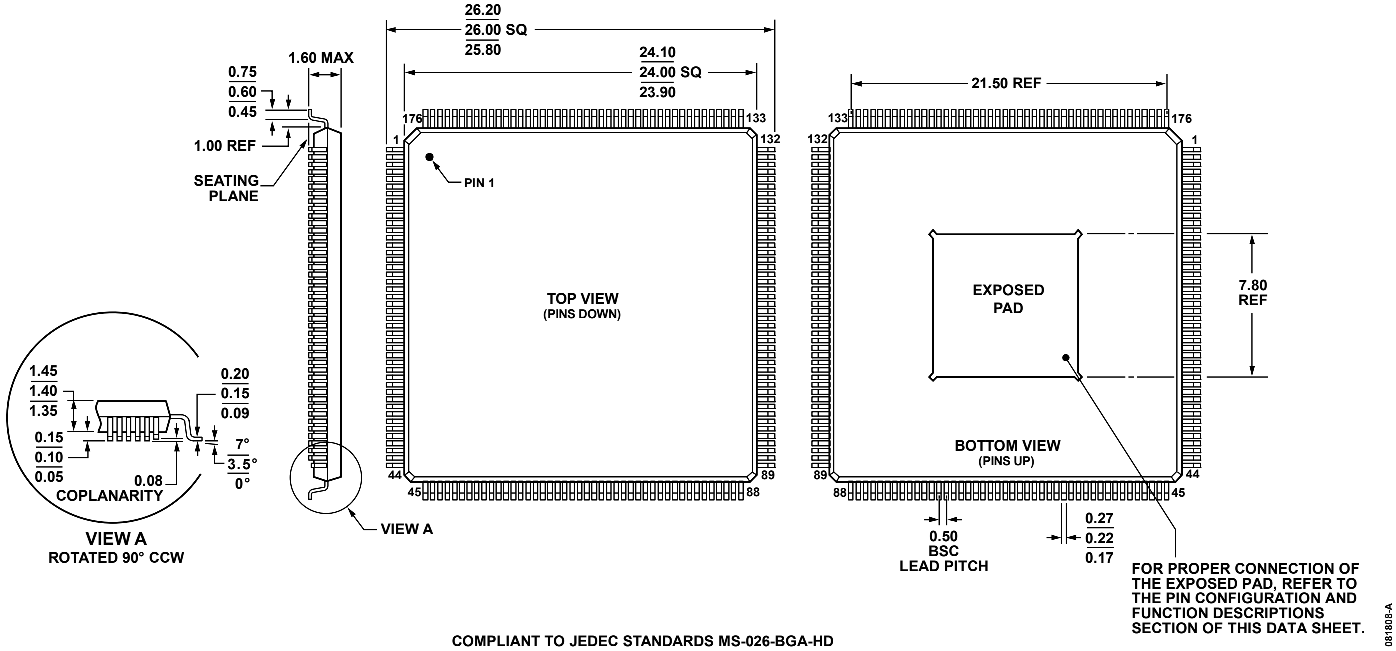

Figure 22. 176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-176-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV3202ASWZ[1]	−40°C to +85°C	176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]	SW-176-1
ADV3203ASWZ[1]	−40°C to +85°C	176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]	SW-176-1

[1] Z = RoHS Compliant Part.

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